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Wire Density Driven Global Routing for CMP Variation and Timing

Minsik Cho¹, Hua Xiang², Ruchir Puri², David Z. Pan¹

¹Department of ECE
University of Texas at Austin
Austin, TX 78712

²IBM Research Division
Thomas J. Watson Research Center
P.O. Box 218
Yorktown Heights, NY 10598



Research Division
Almaden - Austin - Beijing - Haifa - India - T. J. Watson - Tokyo - Zurich

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Minsik Cho*, Hua Xiang[†], Ruchir Puri[†] and David Z. Pan*

*Dept. of ECE, The University of Texas at Austin, Austin, TX 78712

[†]IBM T. J. Watson Research Center, Yorktown Heights, NY 10598

thyeros@cerc.utexas.edu, huaxiang@us.ibm.com, ruchir@us.ibm.com, dpan@ece.utexas.edu

Abstract—We propose the first wire density driven global routing that considers CMP variation and timing optimization. To enable CMP awareness during global routing, we propose a compact predictive CMP model with dummy insertion, and validate it with extensive industry data. While wire density has some correlation and similarity to the conventional congestion metric, they are indeed different in the global routing context. Therefore, wire density rather than congestion should be a unified metric to improve both CMP variation and timing. The proposed wire density driven global routing is implemented in a congestion-driven global router [1] for CMP and timing optimization. The new global router utilizes several novel techniques to reduce the wire density of CMP and timing hotspots. Our experimental results are very encouraging. The proposed algorithm improves CMP variation and timing by over 7% with negligible overhead in wirelength and even slightly better routability, compared to the pure congestion-driven global router [1].

I. INTRODUCTION

Aggressive technology scaling has led to much higher resistance and larger coupling capacitance on interconnect. According to ITRS roadmap [2], copper dishing/erosion after Chemical-Mechanical Polishing (CMP) and scattering effect may increase resistance significantly [3]–[5]. Also, coupling capacitance between wires becomes dominant over ground/fringing capacitance at $0.18\mu\text{m}$ technology (over 60% of the total capacitance), and increases rapidly with higher wire aspect ratio of the advanced technologies [6]–[8]. Therefore, interconnect delay will suffer from the increased resistance and coupling capacitance more seriously in the future.

Meanwhile, manufacturability and yield are becoming ever-serious concerns at 90nm node and below, and shown to be heavily affected by design patterns [9]. Especially, topography (thickness) variation after CMP is shown to be systematically determined by wire density distribution [4], [9], [10]. Even after CMP, intra-chip topography variation can still be on the order of 20–40% [9], [11]. Such topography variation leads to not only significant performance degradation due to increased wire resistance and capacitances, but also acute manufacturing issues like etching and printability [3], [9], [11], [12].

The main reason for the above problems is wire density distribution. Higher wire density usually leads to copper thickness reduction due to erosion after CMP [4], [10], making resistance worse. Also, the reduced copper thickness after CMP can

worsen the scattering effect, further increasing resistance [5]. Meanwhile, a region with higher wire density tends to have less spacing between wires, thus significantly increasing coupling capacitance between them. For a lower wire density region, dummy insertion is performed before CMP to make density distribution more uniform, expecting less topography variation after CMP. However, dummy insertion is usually applied in the post-design stage, and has limitations due to strict rules (such as fill size, pattern, spacing to other features) which intend to minimize the disturbance on the existing design. Thus, non-uniform distribution of density still exists even after the dummy insertion, creating topography variation which wastes the already minuscule depth of focus [13].

The global routing, as its name implies, is the routing stage that plans the approximate routing path of each net to reduce the complexity of routing task and guide the detailed router [14]. Thus, it has significant impact on wirelength, congestion/routability and wire density distribution, hence CMP variation and timing [3], [14]–[16]. The global routing should be an ideal stage for the first order to improve CMP variation as well as timing by optimizing wire density distribution [8], [17]. Even though there have been significant amount of work in global routing about crosstalk [17]–[23], timing [8], [15], [17], [24] and congestion/routability [1], [25], [26], none of them has worked on the optimization of wire density distribution for CMP variation and timing.

In this paper, we propose a new paradigm of wire density driven global routing to improve CMP variation and timing. To our best knowledge, this is the first work that takes wire density distribution into account to enhance both CMP variation and timing, while considering congestion and wirelength. Essentially, the proposed algorithm minimizes the wire density around timing critical nets to enhance timing, and the wire density of dense global routing cells to reduce topography variation after CMP. The major contributions of this paper include the following.

- We present a simple predictive CMP model verified with industrial cases for the first time. We also show that only few regions of a chip are responsible for most of topography variation after CMP. This means that selective optimization of wire density distribution can enhance the uniformity of topography.
- We use the wire density to guide global routing for CMP variation and timing. We show that wire density and con-

gestion are not linearly proportional to each other. This implies that just congestion-driven global routing cannot address the wire density issue efficiently. Furthermore, we observe that wire delay is near linearly proportional to wire density in global routing even with CMP effect (dishing/erosion and dummy insertion) [4], [11], [27] and scattering effect [5] taken into consideration.

- We propose several novel wire density driven routing techniques for CMP variation and timing optimizations, including minimum pin density routing, timing sensitivity map and CMP aware wire density distribution. Each technique helps global router to reduce the wire density around timing critical nets, while minimizing topography variation after CMP.

Our approach achieves better timing and less topography variation than the state-of-the-art academic congestion-driven router [1] with negligible overhead on wirelength, and even better congestion/routability.

The rest of the paper is organized as follows. In Section II, preliminaries are described. A predictive CMP model is presented, and timing impact with wire density distribution is analyzed in Section III. In Section IV, a wire density driven global routing is proposed. Experimental results are discussed in Section V. Section VI concludes this paper.

II. PRELIMINARIES

A. Global Routing Model

The global routing problem can be modelled as a grid graph $G(V, E)$, where each vertex v_i represents a rectangular region of the chip, so called a global routing cell (G-cell), and each edge e_{ij} represents the boundary between v_i and v_j with a given maximum routing resource r_{ij} . A global routing is to find paths that connect the pins inside the G-cells through $G(V, E)$ for each net.

B. Global Routing Metrics

The key task of global router is to maximize (minimize) the routability (congestion) for successful detailed routing [16]. In addition, timing, manufacturability, and wirelength are other important goals of global router.

TABLE I
THE NOTATIONS IN THIS PAPER.

v_i	vertex / global routing cell i
w_i	wire density of v_i
d_i	dummy density of v_i
m_i	metal density of v_i
t_i	copper thickness of v_i
l_i	width / height of v_i
n_i	number of signal wires in v_i
p_i	number of wide wires in v_i
s_i	average spacing between wires in v_i
ts_i	timing sensitivity of v_i
e_{ij}	edge between v_i and v_j
r_{ij}	maximum routing resource of e_{ij}
c_{ij}	available routing resource of e_{ij}
g_{ij}	congestion of e_{ij}

- **Routability** can be estimated by the number of *overflows* which indicates that routing demand locally exceeds the available routing capacity [16] [22]. Formal definition of overflow is in [22].
- **Timing** is a significant design objective, as interconnect performance which governs the overall system performance is mainly determined by global routing [8], [15].
- **Manufacturability** is no longer an optional objective in deep submicron region. In global routing, CMP variation which is a macro systematic variation due to wire density distribution can be optimized, as global router plans approximate routing path for each net [14].
- **Wirelength** is an important metric for placement as well as routing. But, it is less concern for global routing, as routing all wires with shortest path algorithms will result in minimum or near-minimum wirelength [16].

III. PREDICTIVE CMP MODEL AND TIMING IMPACT WITH WIRE DENSITY DISTRIBUTION

In this section, we propose a predictive CMP model for the first time. It is followed by the study of the timing impact of wire density under CMP (topography variation and dummy insertion) [3] and scattering effect [5]. Then, we show that congestion driven routing cannot replace wire density driven routing, even though they are closely related.

A. Wire density and Predictive CMP Model

Topography variation (thickness variation) after CMP is determined by underlying metal density which includes both wires and dummies. As dummy insertion in turn depends on wire density, the required dummy density and the expected copper thickness can be predicted from a given wire density.

In Fig. 1, normalized copper thickness change by metal density is shown based on three industrial designs. For a given G-cell v_i with a metal density m_i , we discover the copper thickness of v_i , t_i can be expressed as follows:

$$t_i = \alpha \left(1 - \frac{m_i^2}{\beta}\right) \quad (0.2 \leq m_i \leq 0.8) \quad (1)$$

where α and β are technology dependent constants. Eq. (1) requires the metal density m_i as an input which is essentially the summation of the wire density w_i and the dummy density d_i in a global routing cell v_i . Fig. 2 shows the required dummy density and the predicted copper thickness with respect to wire

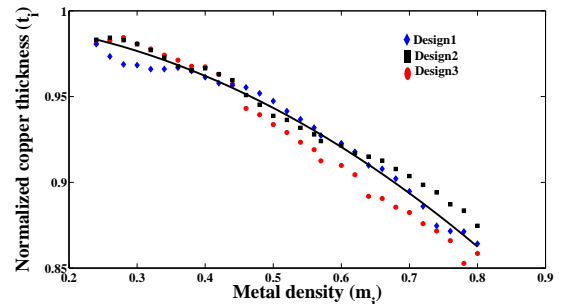


Fig. 1. Normalized copper thickness by metal density

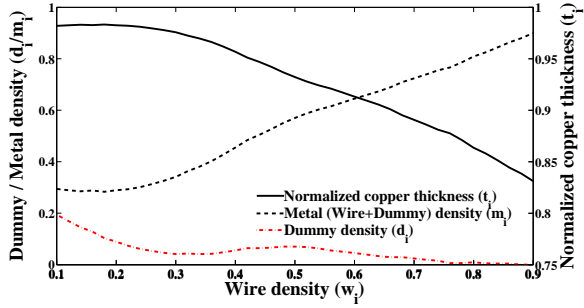


Fig. 2. Predictive CMP model

density. For a given v_i , d_i can be looked up with w_i using Fig. 2, and then m_i can be obtained by adding w_i and d_i . Finally, the calculated m_i can be fed into Eq. (1) to predict the copper thickness t_i . This predictive model is verified with a commercial CMP simulator [28] and industry test cases.

B. Wire density and Timing

For two adjacent wires, each has two capacitance components, coupling capacitance C_c between itself and the other wire, and ground capacitance C_g between itself and ground. Bakoglu [29] shows that wire delay on a distributed RC network contains the following delay component, D :

$$D \propto (R_d + r \cdot l)(C_g + C_c) = (R_d + \frac{\rho \cdot l}{w \cdot t}) \left(\frac{\epsilon \cdot l \cdot w}{h} + \frac{\epsilon \cdot l \cdot t}{s} \right) \quad (2)$$

where R_d is the driver resistance, ρ is the resistivity of the wire, ϵ is the insulator dielectric constant, w , t and h are the wire width, thickness and distance from the substrate, respectively. And, l and s are the length and spacing between two coupled wires, respectively.

In Eq. (2), h is a constant and w can be assumed to be a constant as well (we do not consider the width variation effect in this paper as it is relatively small for copper process). Without loss of generality, we just use the nominal wire width. For a given G-cell v_i , t_i is essentially a function of w_i (m_i depends on w_i as in Fig. 2), and can be denoted as $t_i(w_i)$. If even spacing between wires and square G-cell are assumed, spacing between wires s_i becomes a function of w_i :

$$s_i(w_i) = l_i \cdot \frac{1 - w_i}{n_i + p_i} \propto \frac{1}{w_i} - 1 \quad (0 < w_i \leq 1) \quad (3)$$

Also, we can obtain the increased total capacitance due to dummy insertion (dummy increases coupling capacitance) as a function of w_i based on [27]:

$$f(w_i) = 1 + \gamma \log\left(\frac{s_i(w_i)}{\delta}\right) \quad (4)$$

where γ and δ are technology dependent constants. Note that $f(w_i)$ is typically less than 1.1, and saturates quickly. Due to scattering effect under a given temperature, ρ is a function of t_i . Thus, it is also a function of w_i (see Eq. (1)), and can be denoted as $\rho(w_i)$ [5]. Finally, the component of the wire delay in v_i can be rewritten as a function of w_i based on Eq. (2):

$$R(w_i) = \frac{\rho(w_i) \cdot l_i}{t_i(w_i) \cdot W_{nom}} \quad (5)$$

$$C(w_i) = \epsilon \cdot f(w_i) \left(\frac{l_i \cdot W_{nom}}{h} + \frac{l_i \cdot t_i(w_i)}{s_i(w_i)} \right) \quad (6)$$

$$D(w_i) \propto (R_d + R(w_i))C(w_i) \propto w_i \quad (7)$$

We observe the following with 65nm technology node:

- Lower wire density shows less resistance (less erosion after CMP) as well as less capacitance (more spacing between wires).
- Resistance variation dependence on wire density (computed post dummy insertion and CMP estimation) is relatively smaller than capacitance variation.
- $D(w_i)$ is near linearly proportional to w_i in the region where most of wire densities exist (see Eq. (3) and (6)).

C. Wire Density and Congestion

While congestion/routability has been the main concern in global routing, wire density distribution is an emerging important objective due to CMP variation and timing as shown in Section III-A and III-B. Although wire density is closely related to congestion, congestion driven global routing cannot address wire density issues directly and effectively, because wire density is computed for the wires inside a global routing cell, while congestion is computed for the wires crossing the edges of a global routing cell.

For example, Fig. 3 shows a G-cell with edge A and B . When there is a wide wire such as power/ground as in Fig. 3 (a), density is not a half of congestion. Even though Fig. 3 (a) and (b) have the same density, Fig. 3 (b) is less congested. As wire density and congestion can be significantly different, wire density cannot be replaced with congestion; as a unified metric, wire density should be directly addressed in global routing for the optimization of CMP variation and timing.

IV. WIRE DENSITY DRIVEN GLOBAL ROUTING FOR CMP VARIATION AND TIMING

In this section, we propose our wire density driven global routing algorithm which essentially minimizes the delay of timing critical nets by decreasing the wire density around such nets, and improves the topography variation after CMP by decreasing the wire density of dense G-cells selectively. Our approach consists of four ideas which can be easily integrated with any existing global router [1], [22], [25], [26]; minimum pin density routing in Section IV-A, timing sensitivity map in Section IV-B, selective wire density optimization for CMP awareness in Section IV-C, and wire density driven maze routing in Section IV-D.

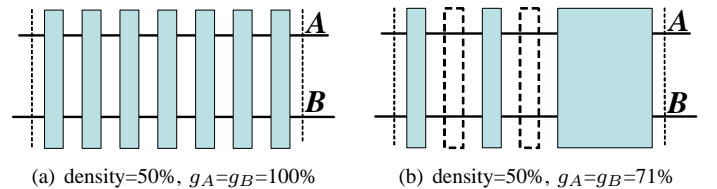


Fig. 3. Difference between congestion and density

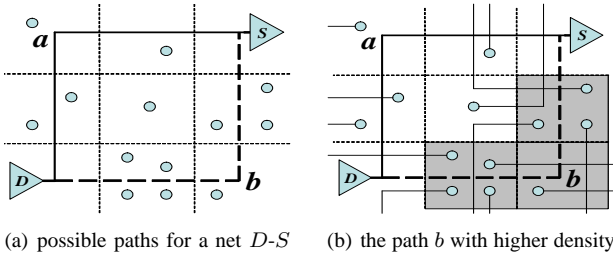


Fig. 4. Motivational example of the minimum pin density routing

A. Minimum Pin Density Routing

In practice, timing critical nets are commonly routed before other nets for the minimum length. As there can be multiple paths with the minimum length, a router can choose any of those based on its policy. However, we find that a path with the minimum pin density is better for the wire density distribution. In Fig. 4, a net D - S to be routed is shown with a pin distribution. If only L-shape routing is allowed, we can have two possible paths, a and b with the same length but different pin densities. As the existence of a pin means a connection to other pins, a path with higher pin density like b tends to have higher wire density eventually as in Fig. 4 (b), resulting in higher resistance and larger coupling capacitance.

More importantly, the path with higher pin density cannot get much benefit from the wire density optimization, as there is little room for improvement (it is destined to have high wire density from the beginning). Note only L/Z-shape routing is considered in the minimum pin density routing to minimize the number of vias in our implementation.

B. Timing Sensitivity Map Construction

As Elmore delay can be expressed as the summation of RC product where C is the downstream capacitance seen by R in the distributed RC network, a capacitance close to the sink has more impact on timing than one close to the driver. Also, the capacitance of a G-cell where more timing critical nets are passing has more impact on timing. Thus, we can compute the sensitivity of each G-cell to timing, and construct the timing sensitivity map. As resistance is relatively insensitive to wire density (see Section III-B), we consider only capacitance in constructing the timing sensitivity map. Fig. 5 illustrates how to construct timing sensitivity map. Given a net D_1 - S_1 - S_2 as in Fig. 5 (a), if nominal resistance R is assumed for each G-cell (see Section III-B), a part of Elmore delay from D_1 to S_1 can be written as follows:

$$\begin{aligned} \text{Delay} &\propto RC(w_a) + 2RC(w_b) + 4RC(w_f) \\ &+ 3\{RC(w_c) + RC(w_d) + RC(w_e)\} \end{aligned}$$

As mentioned in Section III-B, RC wire delay in a G-cell v_i is near linearly proportional to w_i . Thus, the above delay equation can be further simplified as follows:

$$\text{Delay} \propto w_a + 2w_b + 4w_f + 3\{w_c + w_d + w_e\}$$

It is clear that each wire segment (thus, each G-cell) has different impact on the timing due to its geometrical location (whether it is close to driver or not). For example, 10%

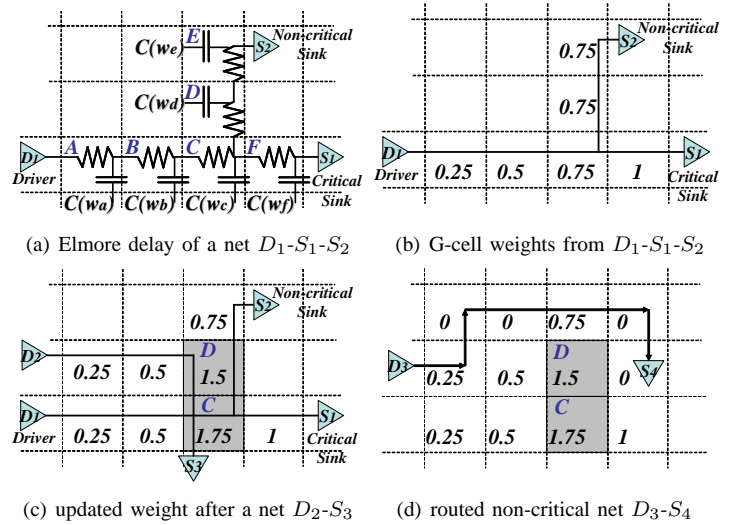


Fig. 5. Example of the timing sensitivity map construction

increase of w_f has the same impact as 40% increase of w_a on timing. Therefore, each G-cell can have its own time sensitivity to the density change as in Fig. 5 (b). We can apply the same idea to all the timing critical nets which are already routed by the minimum pin density routing, and sum up the timing sensitivity from each net to construct a timing sensitivity map. For example, in Fig. 5 (c), another timing critical net D_2 - S_3 is joining the net D_1 - S_1 - S_2 at the G-cell v_C and v_D . As v_C has already 0.75 as the timing sensitivity ts_C , after considering D_2 - S_3 , ts_C becomes 1.75 due to 1 from D_2 - S_3 . In the same manner, ts_D becomes 1.5 due to another 0.75 from D_2 - S_3 . With the timing sensitivity of each G-cell, we can make a non-timing critical net D_3 - S_4 detour to reduce the wire density of the highly timing sensitive G-cell like v_D as in Fig. 5 (d). This improves the overall timing by reducing the wire density of more timing sensitive G-cells, while minimizing the overhead in wirelength. Algorithm 1 shows how to construct the timing sensitivity map.

Algorithm 1 Timing Sensitivity Map Construction

Input: List of timing critical nets and G-cells

- 1: $ts_i = 0 \forall$ G-cell i
- 2: **for** each timing critical net N **do**
- 3: $P =$ Path from critical sink S to driver D
- 4: $L_s =$ Path length from S to D
- 5: **for** each G-cell $v_j \in P$ **do**
- 6: $L_j =$ Path length from v_j to D
- 7: $ts_j = ts_j + L_j/L_s$
- 8: **end for**
- 9: **for** each G-cell $v_j \notin P, \in N$ **do**
- 10: $v_x =$ G-cell closest to $v_x \in P$
- 11: $L_x =$ Path length from v_x to D
- 12: $ts_j = ts_j + L_x/L_s$
- 13: **end for**
- 14: **end for**

Output: Timing sensitivity map

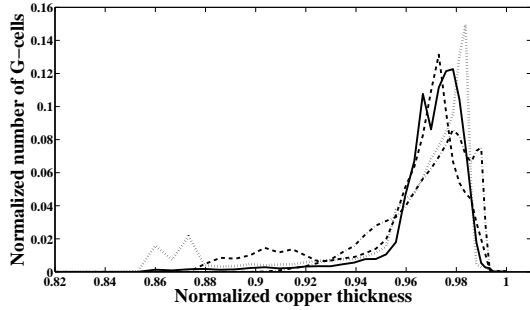


Fig. 6. Normalized copper thickness distributions of four industrial designs

C. CMP Aware Wire Density Distribution

To improve CMP variation, more uniform wire density distribution should be achieved by increasing density for less dense G-cells or decreasing density for more dense G-cells. We find that reducing wire density of the more dense G-cells can be more effective than the other way for two reasons. First, it requires to perturb smaller number of G-cells. Fig. 6 shows copper thickness distributions of four industrial cases after CMP. It shows only few G-cells have over 5% of copper loss, and are mainly responsible for topography variation. Thus, optimizing only such G-cells can make topography more uniform without disturbing other design objectives. Second, lowering wire density also helps congestion as they are correlated.

D. Wire Density Driven Maze Routing

As discussed so far, the wire density distribution governs both CMP variation and timing. The objective for timing requires lower density for the timing sensitive G-cell, and the objective for CMP variation requires lower density for the G-cells above the threshold of Section IV-C. The wire density driven maze routing is shown in Algorithm 2. Note that $Cost_o$ represents costs from other design objectives such as congestion, power and printability. Two parameters, P and Q are introduced to control the trade-off between objectives.

V. EXPERIMENTAL RESULTS

We implement the proposed algorithm in C++ by modifying BoxRouter [1], and compare the results with the original BoxRouter. All the experiments are performed on a 2.8 GHz Pentium-4 Linux machine. The ISPD98 IBM benchmarks are taken from [30], and we modify the horizontal and vertical capacity of each circuit as shown in Table II. Further, assuming up to 30% of routing capacity is assigned for wide wires

Algorithm 2 Wire Density Driven Maze Routing

Input: G-cell v_i and Parameter P, Q, T_d

- 1: Cost $C = Cost_o$ //from other optimization costs
- 2: **if** $ts_i > 0$ **then**
- 3: $C += P \cdot w_i \cdot (1 + ts_i)$ //timing sensitivity
- 4: **else if** $w_i > T_d$ **then**
- 5: $C += Q \cdot w_i$ //CMP awareness
- 6: **end if**

Output: C

like power/ground, we reduce the routing capacity to get enough number of overflows (to see the impact on congestion/routability), and make the horizontal and the vertical capacity same for easy wire density calculation. Since the original benchmarks do not have any timing information, we randomly pick less than 1% nets which are longer than $200\mu m$ as optimization targets. HSPICE simulation with $65nm$ technology is performed to estimate timing with CMP variation and scattering effect taken into account. Note that all the timing critical nets are pre-routed in the same minimum length and same topology in any experiment to eliminate the effect of different path lengths and topologies on timing.

Fig. 7 (a) shows total/max delay and wirelength change by the parameter P with $Q=0$. While the wirelength increases as P increases, the delay decreases until $P=1$, and then starts increasing after that. The reason is because too much increase in wirelength due to detouring around timing sensitive G-cells (with higher P value), finally makes overall congestion worse. This provokes the congestion driven objective to push wires back to the timing sensitive G-cells. All the following simulations use $P=1$, as it shows reasonable trade-off. Fig. 7 (b) shows total/max delay, wirelength and topography variation change by the parameter Q with $P=1$. While the total delay and max delay increase with larger Q , the topography variation decreases. Wirelength does not change noticeably, proving that our selective wire density optimization for CMP variation is friendly with other design objectives. Even though the topography variation can be improved by more than 10% with quite large Q , all the following simulations use $Q=1.3$ for the minimal impact on timing.

Table II shows the experimental results and comparison of the proposed algorithm (the modified BoxRouter) with the original BoxRouter. The experiment sets $P=1$, $Q=1.3$ and $T_d=0.33$ of Algorithm 2 to evaluate the optimization for CMP variation and timing together. The average of total delay and max delay are slightly reduced to 7.0% and 8.0% respectively, while topography variation after CMP is improved by 7.5% on average and up to 10.1%. The overhead in CPU time is still only 41% on average. Also routability is improved, as the number of G-cells with high wire density (which tend to be congested) is reduced by CMP aware wire density distribution. As already shown in Fig. 7 (b), wirelength overhead is quite small, and the improved routability further suppresses the increase in wirelength (less detouring) as well.

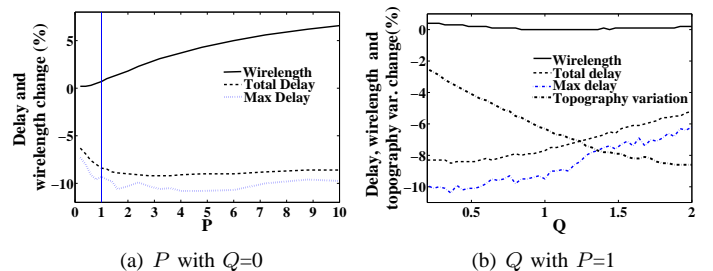


Fig. 7. Effectiveness of parameter P and Q in Algorithm. 2

TABLE II
COMPARISON WITH BOXROUTER FOR ISPD98 BENCHMARKS.

circuit			BoxRouter							Wire Density Driven BoxRouter						Change (%)							
name	hz. cap	vt. cap	t.del ^a (ns)	m.del ^b (ps)	wlen ^c	ovfl ^d	dum ^e	t.v ^f (%)	cpu (sec)	t.del (ns)	m.del (ps)	wlen	ovfl	dum	t.v (%)	cpu (sec)	t.del	m.del	wlen	ovfl	dum	t.v	cpu
ibm01	18	18	0.57	30.1	61374	4	372	1.34	7.1	0.53	26.3	61512	5	366	1.31	8.7	-6.7	-12.5	0.2	25.0	-1.6	-2.2	22.5
ibm02	36	36	1.85	67.6	180816	25	357	1.94	34.8	1.74	66.3	180399	26	358	1.90	44.7	-6.0	-2.0	-0.2	4.0	0.3	-2.1	28.4
ibm03	31	31	1.91	75.7	148530	5	389	1.73	16.0	1.77	69.4	150274	6	389	1.75	23.7	-7.0	-8.4	1.2	20.0	0.0	1.2	48.1
ibm04	26	26	1.61	61.4	167557	99	441	1.75	20.0	1.47	58.2	168307	100	437	1.75	26.4	-8.4	-5.2	0.4	1.0	-0.9	0.0	32.0
ibm05	45	45	3.75	252.2	426547	100	542	1.78	51.1	3.41	219.3	432529	85	539	1.84	77.7	-9.1	-13.0	1.4	-15.0	-0.6	3.4	52.1
ibm06	35	35	2.10	243.8	283836	11	540	1.42	33.1	1.93	228.0	286783	8	541	1.46	49.7	-8.3	-6.5	1.0	-27.3	0.2	2.8	50.2
ibm07	34	34	1.77	100.7	372268	18	867	1.67	46.5	1.62	93.1	374954	17	871	1.68	63.1	-8.3	-7.5	0.7	-5.6	0.5	0.6	35.7
ibm08	31	31	2.62	191.8	420609	72	770	1.72	94.2	2.36	162.4	423634	62	770	1.74	121.7	-10.0	-15.3	0.7	-13.9	0.0	1.2	29.2
ibm09	25	25	2.32	192.8	432120	75	1091	1.59	68.8	2.13	170.4	435230	70	1088	1.58	88.1	-8.3	-11.6	0.7	-6.7	-0.3	-0.6	28.1
ibm10	43	43	3.21	799.0	584100	33	1183	1.48	90.5	2.85	711.4	589234	32	1166	1.48	122.3	-11.4	-11.0	0.9	-3.0	-1.4	0.0	35.1
average																	-7.0	-8.0	0.0	-28.6	-2.2	-7.5	40.9

(a) total delay (b) max delay (c) wirelength (d) overflow (e) the amount of dummy (f) topography variation after dummy insertion(std/avg)

VI. CONCLUSION

In nanometer design, wire density should be a key metric for manufacturability and performance optimization. We present the first wire density driven global routing to improve CMP variation as well as timing based on the predictive CMP model and several novel techniques. Experimental results are highly encouraging, showing that the proposed algorithm outperforms the state-of-the-art congestion driven global router in terms of CMP variation and timing with negligible overhead in wirelength, and even slightly better routability.

REFERENCES

- [1] M. Cho and D. Z. Pan, "BoxRouter: A New Global Router Based on Box Expansion and Progressive ILP," in *Proc. Design Automation Conf.*, July 2006.
- [2] International Technology Roadmap for Semiconductors (ITRS), 2005.
- [3] T. E. Gbondo-Tugbawa, "Chip-Scale Modeling of Pattern Dependencies in Copper Chemical Mechanical Polishing Process," in *Ph.D. Thesis, Massachusetts Institute of Technology*, 2002.
- [4] P. Zarkesh-Ha, S. Lakshminarayann, K. Doniger, W. Loh, and P. Wright, "Impact of Interconnect Pattern Density Information on a 90nm Technology ASIC Design Flow," in *Proc. Int. Symp. on Quality Electronic Design*, Nov 2003.
- [5] S. Im, N. Srivastava, K. Banerjee, and K. E. Goodson, "Scaling Analysis of Multilevel Interconnect Temperatures for High-Performance ICs," *IEEE Trans. on Electron Devices*, vol. 52, Dec 2005.
- [6] R. Arunachaiam, K. rajagopal, and L. T. Pileggi, "TACO: Timing Analysis with COupling," in *Proc. Design Automation Conf.*, June 2000.
- [7] D. Wu, J. Hu, M. Zhao, and R. Mahapatra, "Timing Driven Track Routing Considering Coupling Capacitance," in *Proc. Asia and South Pacific Design Automation Conf.*, Jan 2005.
- [8] D. Wu, J. Hu, and R. Mahapatra, "Coupling Aware Timing Optimization and Antenna Avoidance in Layer Assignment," in *Proc. Int. Symp. on Physical Design*, April 2005.
- [9] X. Qi, A. Gyure, Y. Luo, S. C. Lo, M. Shahram, and K. Singhal, "Emerging technologies: Measurement and characterization of pattern dependent process variations of interconnect resistance, capacitance and inductance in nanometer technologies," in *ACM Great Lakes symposium on VLSI*, April 2006.
- [10] S. Lakshminarayanan, P. J. Wright, and J. Pallinti, "Electrical characterization of the copper CMP process and derivation of metal layout rules," *IEEE Trans. on Semiconductor Manufacturing*, vol. 16, Nov 2003.
- [11] L. He, A. B. Kahng, K. Tam, and J. Xiong, "Design of IC Interconnects with Accurate Modeling of CMP," in *Int. Society for Optical Engineering (SPIE) Symp. on Microlithography*, Mar 2005.
- [12] R. Tian, D. F. Wong, and R. Boone, "Model-Based Dummy Feature Placement for Oxide Chemical-Mechanical Polishing Manufacturability," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 20, 2001.
- [13] S. J. Fang, T. H. Smith, G. B. Shinn, J. A. Stefani, and D. S. Boning, "Advanced Process Control in Dielectric Chemical Mechanical Polishing (CMP)," in *Chemical Mechanical Polish for ULSI Multilevel Interconnection Conference*, Feb 1999.
- [14] J. Hu and S. Sapatnekar, "A Survey On Multi-net Global Routing for Integrated Circuits," *Integration, the VLSI Journal*, vol. 31, 2002.
- [15] —, "A Timing-Constrained Algorithm for Simultaneous Global Routing of Multiple Nets," in *Proc. Int. Conf. on Computer Aided Design*, 2000.
- [16] J. Westra, P. Groeneveld, T. Yan, and P. H. Madden, "Global Routing: Metrics, Benchmarks, and Tools," in *IEEE DATC Electronic Design Process*, April 2005.
- [17] M. R. Beecer, D. Blaauw, R. Panda, and I. N. Hajj, "Early Probabilistic Noise Estimation for Capacitively Coupled Interconnects," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 22, March 2003.
- [18] T.-Y. Ho, Y.-W. Change, S.-J. Chen, and D. T. Lee, "A Fast Crosstalk and Performance-Driven Multilevel Routing System," in *Proc. Int. Conf. on Computer Aided Design*, Nov 2003.
- [19] D. A. Kirkpatrick and A. L. Sangiovanni-Vincentelli, "Techniques For Crosstalk Avoidance In The Physical Design Of High-performance Digital Systems," in *Proc. Int. Conf. on Computer Aided Design*, 1994.
- [20] A. Vittal and M. Marek-Sadowska, "Crosstalk reduction for VLSI," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 16, March 1997.
- [21] H. Zhou and D. F. Wong, "Global routing with crosstalk constraints," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 18, Nov 1998.
- [22] R. Kastner, E. Bozorgzadeh, and M. Sarrafzadeh, "Pattern Routing: Use and Theory for Increasing Predictability and Avoiding Coupling," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 21, July 2002.
- [23] P. Saxena and S. Gupta, "On Integrating Power and Signal Routing for Shield Count Minimization in Congested Regions," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 22, April 2003.
- [24] J. Xu, X. Hong, T. Jing, Y. Cai, and J. Gu, "A Novel Timing-Driven Global Routing Algorithm Considering Coupling Effects for High Performance Circuit Design," in *Proc. Asia and South Pacific Design Automation Conf.*, Jan 2003.
- [25] C. Albrecht, "Global Routing by New Approximation Algorithms for Multicommodity Flow," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 20, May 2001.
- [26] R. T. Hadsell and P. H. Madden, "Improved Global Routing through Congestion Estimation," in *Proc. Design Automation Conf.*, June 2003.
- [27] W.-S. Lee, K.-H. Lee, J.-K. Park, T.-K. Kim, and Y.-K. Park, "Investigation of the capacitance deviation due to metal-fills and the effective interconnect geometry modeling," in *Proc. Int. Symp. on Quality Electronic Design*, Nov 2003.
- [28] <http://www.praesagus.com/>.
- [29] H. B. Bakoglu, "Circuits, Interconnections, and Packaging for vlsi," in *Addison-Wesley Publishing Company*, 1990.
- [30] <http://www.ece.ucsb.edu/~kastner/labyrinth/>.