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Germanium-on-SOI Infrared Detectors for Integrated Photonic Applications

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Abstract

An overview of recent results on high-speed Ge-on-silicon-on-insulator (Ge-on-SOI) photodetectors and their prospects for integrated optical interconnect applications are presented. The optical properties of Ge and SiGe alloys are described and a review of previous research on Si-on-insulator (SOI) and SiGe detectors is provided as a motivation for the Ge-on-SOI detector approach. The photodetector design is described, which consists of lateral alternating p- and n-type surface contacts on an epitaxial Ge absorbing layer grown on an ultra-thin-SOI substrate. When operated at a bias voltage of -0.5 V, 10 x 10 μm^2 devices have dark current, I_{dark}, of only ~ 10 nA, a value that is nearly independent of finger spacing, S, down to S = 0.3 μm. Detectors with S = 1.3 μm have external quantum efficiencies, η, of 52% (38%) at λ = 895 nm (850 nm) with corresponding responsivities of 0.38 A/W (0.26 A/W). The wavelength-dependence of η agrees fairly well with expectations, except at longer wavelengths, where Si up-diffusion into the Ge absorbing layer reduces the efficiency. Detectors with 10 x 10 μm^2 area and S = 0.6 μm have -3 dB bandwidths as high as 29 GHz, and can simultaneously achieve a bandwidth of 27 GHz, with I_{dark} = 24 nA, at a bias of only -1 V, while maintaining high efficiency of η = 46% (33%), at λ = 895 nm (850 nm). Analysis of the finger-spacing and area dependence of the device speed indicates that the performance at large finger spacing is transit-time limited, while at small finger spacing, RC delays limit the bandwidth. Methods to improve the device performance are presented, and it is shown that significant improvement in the speed and efficiency both at λ = 850 nm and 1300 nm can be expected by optimizing the layer structure design.

Index terms**:** Germanium, photodetectors, optoelectronic devices, silicon on insulator technology

I. INTRODUCTION

As bandwidth requirements for high-performance servers continue to increase, a greater push is being made to incorporate optical components to replace conventional copper interconnects for local I/O functions [1]. The reason is that traditional copper links cannot transmit longer than a few meters once data rates increase beyond several Gbit/sec per channel. Furthermore, the edge connector density is restricted using copper interconnects, placing an upper limit on overall system performance. Not only would highly-parallel optical data links offer superior performance in terms of bandwidth-length product, but, as data rates scale, these links should also increase overall interconnect density, reduce power dissipation and improve synchronization. The transition to optical interconnects is expected to occur first at the rack-to-rack level. However, as bandwidth requirements continue to increase, optical solutions will also be needed for board-to-board and eventually chip-to-chip interconnects [2].

Conventional high-speed fiber-optic components mainly utilize compound semiconductors (mostly III-Vs) due to their excellent light-emission and absorption properties, as well as the wide range of alloys and heterostructures that can be used to precisely optimize device performance in a given system application. Unfortunately, compound-semiconductor devices are generally too costly for utilization in server-based optical interconnects, due to the overhead associated with manufacturing optical components in a separate facility, as well as the costs associated with packaging and assembling the hybrid III-V / CMOS interconnect subsystem. When combined with CMOS electronics, III-V-based systems also tend to suffer performance degradation due to packaging parasitics and crosstalk associated with wire-bond leads.

For these reasons, there has been ongoing interest in utilizing Si-based optical components to realize a fully monolithic solution for high-performance optical interconnects [3]. A potential advantage of monolithic integration is reduced cost, which results from the lower starting material costs, as well as the ability to leverage the volume manufacturing infrastructure of Si processing. Integrated optical interconnects could also have improved performance by eliminating the parasitics and noise associated with hybrid packaging technology and may eventually allow higher interconnect densities to be realized.

Unfortunately, the poor optical properties of Si have so far precluded the development of several key components needed for integrated optical interconnects. In particular, for receivers, weak absorption in the infrared makes it difficult to realize high-performance photodetectors in Si. For example, at a wavelength, λ, of 850 nm, the most promising platform for near-term optical interconnects due to the low cost of multi-mode fiber and availability of relatively inexpensive GaAs VCSEL emitters, Si has a very low absorption coefficient of 600 cm^{-1} [4] as shown in Fig. 1. The corresponding absorption depth, α^{-1}, of 17 μm makes it difficult to overcome the fundamental speed / responsivity trade-offs associated with photodetector devices. Furthermore, Si is transparent at λ = 1300 nm and 1550 nm, wavelength platforms that are standard for long-distance fiber-optic communications, but which could also be useful for future high-performance short-distance interconnects.

In recent years, $Si_{1-x}Ge_x$ has emerged as a mainstream technology with tremendous benefits for both bipolar and CMOS transistor-based technologies [5]. However, $Si_{1-x}Ge_x$ has a number of benefits for photonic applications as well, not the least of which is an

increased absorption coefficient and absorption edge at longer wavelengths compared to Si [6]. Unfortunately, as shown in Fig. 1, the absorption advantages gained by $Si_{1-x}Ge_x$ do not become significant until rather high Ge concentrations are reached, and that the strongest absorption occurs in pure Ge layers [7]. To illustrate this point more clearly, Fig. 2(a) shows the $Si_{1-x}Ge_x$ absorption depth plotted as a function of Ge concentration, x, for three different wavelengths important for fiber-optic links. The plot shows that, at λ = 850 nm, α^{-1} is improved by only a factor of 1.5 in $Si_{0.8}Ge_{0.2}$ alloys compared to Si, and even for $Si_{0.5}Ge_{0.5}$, the absorption depth is still ~ 4 μm, roughly only a factor of 4 smaller than Si. Similarly, at λ = 1300 nm, the absorption depth is over 100 μm at $x = 0.7$. In contrast, pure Ge has an absorption depth less than 300 nm at λ = 850 nm, a factor of over 50 times shorter than Si at the same wavelength. At λ = 1300 nm, α^{-1} is about 1 μm in Ge, close to the same as GaAs at λ = 850 nm. Pure Ge even absorbs at λ = 1550 nm, though the absorption depth (α^{-1} ~ 10 μm) is only slightly less than Si at λ = 850 nm.

The Ge-concentration dependence of the absorption properties can be understood by an examination of Fig. 2(b), which plots the calculated energy gaps associated with various valence-to-conduction band transitions in $Si_{1-x}Ge_x$ as a function of x [8]. The plot shows that while the energy associated with the Δ-point transition has a very weak Ge-concentration dependence, the indirect L-point and direct Γ-point transition energies decrease rapidly at high Ge concentrations. This dependence explains why, at low x, the absorption coefficient at λ = 850 nm is a very weak function of x, but increases more rapidly at higher x as L- and Γ-point absorption take effect. At λ = 1300 nm, even higher Ge concentrations are needed for the upper conduction-band transitions to take effect, with L- and Γ-point transitions not allowed until $x \gtrsim 0.8$ and 0.9, respectively.

From the above discussion, it is clear that the high absorption coefficient in Ge makes it an extremely attractive material for use in high-performance infrared detectors. In addition to its absorption advantage, Ge also has improved mobility compared to Si, with intrinsic bulk electron and hole mobilities of 3900 and 1900 cm^2/Vs, respectively. The mobility advantage should not only improve the device speed compared to Si, but also allow operation at low voltages, a key priority for integrated detector applications.

Despite the advantages described above, Ge can be a challenging material to integrate into a CMOS in manufacturing environment. The main difficulty is the 4.2% lattice mismatch between Si and Ge, which can cause rough growth and lead to high defect densities in epitaxial films grown on Si [9]. The process temperatures for Ge and Si devices could also be incompatible since Ge melts at 934 ^oC, and dopant diffusion is generally much faster in Ge than in Si. Finally, for detector applications, excess dark current is a major concern, not only due to the low band gap of Ge (0.66 eV at room temperature), but also due to the previously-mentioned defects, and the known surface passivation difficulties of Ge [10]. In recent years, many of the above-mentioned difficulties have been overcome to varying extents, and the status of Ge-on-Si technology, as well as the remaining challenges, will be discussed in later sections.

In this paper, we describe our approach to realizing an optimized Ge photodetector that can allow high-performance operation suitable for integrated optical interconnect applications. The approach, based upon Ge-on-silicon-on-insulator (Ge-on-SOI) technology, allows the demonstration of photodetectors that provide nearly all of the characteristics desirable for integrated optoelectronic receiver applications, and could be practical for near-term 10 Gbit/sec and 40 Gbit/sec optical interconnects applications.

The detectors also have good potential for extendibility to higher speeds and operation at longer wavelengths.

In the following sections, we first discuss the performance requirements for integrated photodetectors, and review recent developments in Si- and Ge-based high-performance photodetectors. Then we describe the design and fabrication strategy of our Ge-on-SOI detectors approach. The dc and high-frequency properties of these devices are described next, followed by an assessment of the overall performance figures of merit. Finally, we discuss possible methods of improving the device design to allow even higher performance in the future.

II. BACKGROUND

2.1. Performance requirements for integrated detectors

As a preface to describing previous work on Si and Ge photodetectors, it is useful to review the performance requirements of photodetectors to be used for integrated receiver applications. First, it is important that the devices be capable of high-speed operation, particularly in order to accommodate the anticipated bit rates of future optical interconnect applications. Considering that optoelectronic interconnects utilizing hybrid detectors have already been demonstrated [2], it is essential that integrated devices operate at 10 Gbit/sec with a foreseeable path to at least 40 Gbit/sec operation in the future. Together with high-speed operation, the devices must have reasonable responsivity in order to maintain acceptable signal-to-noise ratio and ease performance and noise constraints on amplifier circuitry. For datacom applications, to achieve adequate receiver sensitivity, photodiode responsivities must be $\gtrsim$ 0.1 A/W [11],

corresponding to external quantum efficiencies, η, of 15%, 10% and 8% at λ = 850 nm, 1300 nm and 1550 nm, respectively. Dark current in integrated photodetectors is an important issue, since the shot noise associated with this leakage current can increase the bit-error rate. In typical detectors, dark currents less than 1 μA are desirable, though a precise value of the required dark current depends upon the speed of operation and the amplifier design. An often-overlooked requirement of integrated detectors is low voltage operation. It would be desirable for the detector and CMOS circuitry to operate on single power supply. This requirement essentially restricts the bias voltage to < 5 V, and for advanced CMOS generations, to biases as low as 1 V.

2.2. Bulk Si detectors

A number of bulk Si photodetector geometries have been reported in the literature [11]-[14]. A good example of the performance of bulk Si detectors designed for integrated receiver applications is described in [11]. In that work, a lateral p-i-n photodetector was fabricated on a high-resistivity bulk Si substrate. Those detectors had a high external quantum efficiency of η = 85% at λ = 850 nm. However, even at a bias of -10 V (-30 V), -3 dB bandwidths of only 124 MHz (234 MHz) were obtained. This is a direct result of the long absorption depth in Si, where a majority of the electron-hole pairs are generated deep within the substrate, far from the high-field drift region generated by the surface electrodes. A novel approach to improving bulk detectors was described by Yang *et al*. [14], who demonstrated a lateral trench detector (LTD) which consisted of a lateral p-i-n detector with 7 μm-deep trench electrodes designed to maintain a uniform electric field deep within the absorbing region. These detectors were able to simultaneously show high efficiency (η = 68%) and high-speed operation

(3 GHz) at $\lambda = 670$ nm. However, at longer wavelengths of $\lambda = 850$ nm, the devices still suffered from degraded bandwidth due to carrier generation and collection below the electrodes.

2.3. SOI detectors

The use of Si-on-insulator (SOI) substrates has been investigated extensively to improve the performance of Si-based photodetectors [11],[15]-[22]. This technique is particularly attractive given the widespread acceptance of SOI technology as a platform for high-performance CMOS [23]. The main benefit gained by using SOI is the fact that the buried insulator can be used to prevent carriers generated in the substrate (below the oxide) from reaching the surface electrodes above the oxide. The index contrast offered by the buried oxide has the additional advantage that it can reflect a portion of the incident light back into the absorbing layer, thus improving efficiency.

Perhaps the best example of the speed improvements that can be gained using SOI photodetectors is the work of Liu *et al.* [15], who demonstrated metal-semiconductor-metal (MSM) detectors on thin SOI substrates with bandwidth as high as 140 GHz. However, those results also reveal a fundamental difficulty with the SOI approach, which is low responsivity due to the thin absorbing region. The devices in [15], which used an absorbing layer of 200 nm, had external quantum efficiencies of only 2.0% and 0.87%, at wavelengths of $\lambda = 650$ nm and 780 nm, respectively. SOI detectors with thicker absorbing layers have been reported in [22]. Predictably, the thicker absorbing layer improved the efficiency (to 24% at $\lambda = 840$ nm), but also resulted in reduced bandwidth of 3.4 GHz.

One approach to improving the bandwidth-efficiency product in Si photodetectors is to utilize novel detector geometries to decouple the transport and absorption lengths in the detector. The LTD geometry described above is one such technique, and when fabricated on SOI wafers, circular LTD detectors with 75-μm diameter [19] have produced values of η = 51% and 2 GHz bandwidth at λ = 850 nm, and bandwidths over 10 GHz, with comparable efficiency, have been realized in smaller-area (14 x 17 μm^2) detectors [20]. The waveguide detector geometry is another approach (commonly-used for integrated photonics in III-V materials) to decouple the transport distance from the absorption length in a low-capacitance configuration with thin absorbing layers. Recent demonstrations of these devices on SOI [17] have produced bandwidths of 15 GHz and 8 GHz in geometries producing external efficiencies of η = 2% and 12%, respectively.

The resonant cavity detector design [24] is another technique that can be applied to Si detectors [25]-[27] to improve efficiency while maintaining a thin absorbing layer. Schaub *et al*. reported an example of such detectors that utilized Si laterally grown over a Si/SiO_2 Bragg reflecting mirror stack [27]. These devices produced a -3 dB bandwidth of 34 GHz, while displaying high quantum efficiency (up to η = 42%) at wavelengths corresponding to sharp resonance peaks in the responsivity. However, in off-resonance conditions, the efficiency dropped by over an order of magnitude, suggesting that devices based upon the resonant cavity design could be very sensitive to process-induced variations. Detectors with roughened [28] or grating [18] backside reflectors can accomplish much of the same effect as resonant cavity structures, and 84-GHz-bandwidth devices with η = 19 % at λ = 850 nm have been demonstrated using the latter technique [18].

2.4. *SiGe and Ge detectors*

A second method of improving the bandwidth-efficiency product is to utilize an alternative material with increased absorption coefficient compared to Si. As described in the previous section, SiGe, and ideally, pure Ge absorbing layers are very promising materials to achieve enhanced absorption at $\lambda = 850$ nm, while having the additional benefit of extending the absorption edge to wavelengths beyond $\lambda = 1550$ nm.

Much of the early work on photodetectors utilizing SiGe involved the use of quantum well or strained-layer superlattice absorbing regions [29]-[35] because these structures can be grown pseudomorphically on Si substrates. Strained $Si_{1-x}Ge_x$ structures are useful because the strain reduces the band gap, allowing absorption at longer wavelengths for a given Ge concentration. However, for operation at $\lambda = 1300$ nm, these layers tend to have very low absorption, and typically require the use of a waveguide geometry in order to achieve high responsivity [34].

The concept of using relaxed Ge on Si as an absorbing layer for a photodetector was first proposed and demonstrated in the pioneering work of Luryi, *et al.* [36]. However, not until recently has the Ge-on-Si concept been resurrected to study its potential for high-performance fiber-optic applications. Several approaches to Ge-on-Si detector design have been investigated. In order to overcome the lattice-mismatch problem described in the previous section, a number of demonstrations of Ge detectors grown on graded buffer layers have been made, since these structures can greatly reduce the density of threading dislocations penetrating into the top layer [37]. Samavedam, *et al*. [38] demonstrated vertical p-i-n devices with excellent dark current density of only 2 pA/μm^2 on graded buffer detectors, while lateral p-i-n geometries on graded buffers

with η = 49% and 3.8 GHz bandwidth were demonstrated by Oh, *et al*. [39]. However, devices on thick graded buffer layers could suffer from integration difficulties due to non-planarity with CMOS devices. Furthermore, though low defect density are needed for VLSI CMOS applications, it is not clear whether elaborate defect reduction techniques are needed for photodetectors.

For this reason, more recent work on Ge-on-Si detectors has focused on the use of thin buffer layers, or even direct growth of Ge on Si. Such structures are beneficial for integration due to the thinner layers used, and it has been found that reasonable defect densities (~ 10^7 cm^{-2}) can still be achieved in such structures when the layers are subjected to post-growth annealing, or grown in limited-area structures [40]. Initial demonstrations of direct-grown Ge-on-Si detectors were made by Colace *et al.* [41] and Masini *et al.* [42], as well as in [43], where lateral MSM devices were demonstrated with similar speed, responsivity and dark current to devices grown on graded buffer layers. Vertical p-i-n photodiodes utilizing Ge on thin SiGe buffers were also demonstrated by Huang *et al*. [44] who reported devices with η = 61% and 8.1 GHz bandwidth using back-side illumination at λ = 1300 nm.

Our previous work in this area was performed using Ge-on-bulk Si lateral p-i-n photodiodes with Ge layers of only ~ 400 nm [45]. Because of the thin absorbing layer, and the transparency of Si at λ > 1100 nm, these devices were able to achieve bandwidths in excess of 15 GHz at λ = 1300 nm, and operated at extremely low voltage of ~ 1 V, but had low quantum efficiency of only 2.5%. For operation at λ = 850 nm, the efficiency improved to η = 30%, but similar to the bulk Si devices described previously, the bandwidth was degraded due to absorption in the underlying Si. More details of these

device results will be described in the following section. Very recently, the ultra-thin Ge-on-Si approach was demonstrated in a vertical p-i-n photodiode by Jutzi *et al*. [46]. These devices had 39 GHz bandwidth and efficiency values of $\eta = 16\%$ at $\lambda = 1298$ nm, and $\eta = 2.8\%$ at $\lambda = 1552$ nm.

2.5. Summary of previous work

The results from the previous work described above clearly demonstrate that tremendous improvement in the performance of Si-based photodetectors can be achieved both from a device design perspective by using SOI technology, and from a materials perspective by using Ge absorbing layers. In the next section, we describe our approach to combine the two technologies to produce Ge-on-SOI detectors that can simultaneous achieve nearly all of the performance requirements needed for integrated detector applications on Si, and provide an extendable platform that could lead to further performance enhancements in the future.

III. GE-ON-SOI PHOTODETECTORS

3.1. Device description

The basic Ge-on-SOI photodetector device design used in the present work is shown in Fig. 3. The device structure consists of a Ge absorbing layer directly on a thin SOI wafer. In this design, the high absorption coefficient of the Ge layer allows the absorbing region to be kept very thin, while the buried oxide serves to prevent any carriers generated in the underlying Si from reaching the top electrodes. The SOI layer is also kept as thin as possible, not only to maintain maximum efficiency in the absorbing region, but also to minimize the amount of Si available for diffusion into the Ge layer with subsequent annealing. This is an important feature of this design, since dilution of

the Ge layer with even a small amount of Si can reduced the detector efficiency, especially at longer wavelengths. The device utilizes a lateral p-i-n geometry, which is favored over a vertical detector design for several reasons. First of all, the lateral design results in a planar contact scheme that is simpler to integrate than a vertical structure. The top-side contacts also minimize the impact of defects that form at the lower Si-Ge interface as a result of the lattice mismatch between Si and Ge. The lateral p-i-n structure is also preferred over an MSM design to ensure that the dark current is kept as low as possible. Finally, the device has interdigitated metal fingers overlaying the implanted electrodes. The metal fingers, while blocking a portion of the incident light, considerably reduce the series resistance of the device, which is crucial for high-speed operation.

3.2. Fabrication

The fabrication of the photodetectors has already been described in detail in [47]. Briefly, the layer structure was grown by ultra-high vacuum chemical vapor deposition (UHV-CVD) directly on an ultra-thin (15 nm) SOI substrate with buried oxide thickness of 140 nm. The epitaxial layer structure consisted of a 30 nm Si buffer layer, followed by a thick Ge layer. SEM inspection indicated that the combined thickness of the Si and Ge layers was ~ 400 nm. After growth, the layer structure was subjected to thermal cyclic annealing to reduce the density of threading dislocations [40]. In all, during this step, the accumulated thermal budget was 900 °C for 1 hour, and the threading dislocation density was reduced from ~ 1×10^9 cm^{-2} before annealing to ~ 1×10^8 cm^{-2} after annealing. In addition to reducing the dislocation density, the annealing also improved the mobility. Hall measurements on the as-grown sample indicated p-type conduction with hole

mobility of 710 cm^2/Vs, while after annealing, the mobility improved to 1140 cm^2/Vs [48].

The devices were fabricated by first defining square mesas with areas, A, of 10 x 10 μm^2, 20 x 20 μm^2 and 30 x 30 μm^2. Oxide was then deposited on the sidewalls in a self-aligned manner (as shown in Fig. 3) to prevent leakage arising from the metal fingers overlapping the edges of the devices. The device fabrication was completed by formation of the n- and p-type implants, activation, and patterning of Ti/Al (30 / 150 nm) contact metal. No anti-reflection coating was used. For the devices described in this paper, the following device dimensions have been utilized. The electrode spacing, S, defined as the distance between the edges of adjacent n- and p-type implants, ranges from 0.3 μm to 1.3 μm. The implanted region width, W_i, and the metal finger width, W_m, have both been kept fixed at values of 0.3 μm and 0.2 μm, respectively. The metal fingers are nominally centered within the boundaries of the implanted regions. An SEM micrograph of a completed 20 x 20 μm^2 device with S = 0.3 μm is shown in Fig. 4.

3.3. DC characteristics

Fig. 5 shows a plot of the dark current, I_{dark}, vs. bias voltage, V_b, for 10 x 10 μm^2 detectors with finger spacing, S, ranging from 0.3 μm to 1.0 μm. All devices show diode-like behavior, with rectifying current-voltage characteristics and very similar current at forward bias. The reverse leakage current has a strong bias dependence that scales roughly with finger spacing, particularly in the range of S = 0.3 to 0.5 μm. The dark current increases with decreasing S at $|V_b| \gtrsim 0.5$ V, but at sufficiently low bias, I_{dark} is relatively independent of S. The photocurrent for the different devices is also shown in the figure. For these measurements, the devices have been overfilled with 822-nm light

using a lensed, 50-μm core multimode fiber. The total power exiting the fiber was 125 μW. As shown in the figure, the photocurrent is nearly independent of bias, and decreases slightly for smaller finger spacing due to the greater shadowing from the metal fingers, an effect that will be described in more detail later.

In order to highlight the significance of the bias dependence of the dark current, Fig. 6 shows the photocurrent and dark current plotted vs. S at different values of V_b. The plot shows that at V_b = -2 V, I_{dark} increases significantly with decreasing finger spacing, becoming comparable to the photocurrent at S = 0.3 μm. However, at V_b = -0.5 V, I_{dark} is considerably lower, and essentially independent of S. Even for detectors with S = 0.3 μm, a dark current of only 8.8 nA is obtained at V_b = -0.5 V. This current value is over 3 orders of magnitude lower than the photocurrent at 125 μW incident power. The ability to reduce the dark current at low bias voltages is important, since, as will be shown later, devices with S = 0.4 μm, can achieve nearly the same bandwidth at V_b = -0.5 V as they can at -2 V. It is this ability to operate at low bias voltages, while still maintaining high speed, that is a key benefit of the Ge-on-SOI detector scheme.

Fig. 7 shows the measured external quantum efficiency plotted vs. wavelength for a 30 x 30 μm^2 device with S = 1.3 μm, as well as calculated responses for the detectors with and without an anti-reflection coating (ARC). The quantum efficiency was measured using a tungsten-halogen light source and a monochrometer. In this setup, the light was focused onto the active area of the device using free-space optics, where a calibrated commercial germanium photodetector was used to measure the incident optical power at each wavelength. The calculated quantum efficiency values have been obtained using a transfer matrix method, assuming the layer stack shown in Fig. 8. For these

calculations, the buried oxide thickness is 140 nm, while a Ge absorbing layer thickness of 392 nm has been utilized, a value that provides the best possible fit to the measured data. For the model utilizing an ARC, the SiN_x layer has a thickness of 120 nm, and a refractive index of 2.0, while for the model with no ARC, the SiN_x layer thickness is zero. The refractive index and absorption values for Ge have been taken from [7], and in all cases, the calculated quantum efficiency values have been scaled by a factor of 0.87 to account for the shadowing from the metal fingers. For simplicity, the calculations do not take into account the thin Si part of the absorbing region.

Fig. 7 shows that, as expected, due to the buried oxide, the quantum efficiency is an oscillatory function of wavelength, with a peak external efficiency of 52% occurring at λ = 895nm, while at λ = 850 nm, the devices have η = 38%. These values correspond to responsivities of 0.38 A/W and 0.26 A/W, respectively. The devices maintain efficiencies greater than 20% up to λ = 1200 nm, before the efficiency (responsivity) drops sharply to η = 3.4% (0.036 A/W) at λ = 1300 nm. The magnitude of the resonance effects observed for the Ge-on-SOI devices are considerably less than occur in resonant-cavity Si detectors [27]. Our calculation results for detectors using a 120 nm SiN_x ARC show that the resonances can be nearly eliminated, while at the same time improving the quantum efficiency to η = 78%. This value is very close to the maximum theoretical value of η = 87%, which is limited by the shadowing factor of the metal fingers. The calculations also indicate that improved absorption can be obtained at longer wavelengths, with a quantum efficiency of η = 22% predicted for λ = 1300 nm, a value that corresponds to a responsivity of 0.23 A/W. This latter result is encouraging for the extendibility of these detectors to longer wavelengths as well as to optimize the layer structure to achieve

higher speeds at shorter wavelengths. Further details of the device design optimization are provided in the next section.

For wavelengths in the range of 600 nm < λ < 1200 nm, reasonably good agreement between the model and experiment are obtained. However, for λ > 1200 nm, the measured quantum efficiencies become much lower than the values predicted by the model. For instance, at λ = 1300 nm, η is only 3.4%, compared to a value of η = 9.3% predicted by the model. To understand the origin of the discrepancy at long wavelengths, the results from Fig. 7 have been expanded and plotted on a log scale in Fig. 9. The plot shows that the deviation between the simulated and measured responses gets larger with increasing wavelength, up to λ ~ 1400 nm, beyond which the device responsivity can no longer be measured. However, the model predicts that this cutoff should not occur until λ > 1600 nm. In our earlier studies, we postulated that this discrepancy occurs due to Si diffusion into the Ge absorbing region as a result of the high-temperature cyclic annealing utilized to reduce the defect density [47]. Despite the fact that the degree of up-diffusion has not been measured directly, if we assume that the absorption is primarily dominated by the Γ-point transition in Ge, then the change in the cutoff wavelength can be used to estimate the amount of Si in the Ge absorbing region. The plot in Fig. 9 shows that the cutoff wavelength corresponds to a 0.14 eV higher Γ-point transition energy, $E_{G(\Gamma)}$, than predicted for pure Ge. Since Fig. 2(b) predicts that $E_{G(\Gamma)}$ increases by 25 meV for every 1% mole fraction of Si added to Ge, then the atomic percentage of Si calculated to have diffused into the Ge layer from thermal annealing is 6%.

For high-speed applications, it is important that high efficiency can be maintained in devices with smaller finger spacings. However, the efficiency is expected to drop as *S*

decreases, due to the increased shadowing from the metal fingers. Therefore, the quantum efficiency was measured for devices with smaller finger spacing, and the results are shown in Fig. 10. Here, η, is plotted vs. finger spacing for 30 x 30 μm^2 detectors at a single incident wavelength of λ = 822 nm. (It should be noted that this wavelength corresponds to a minimum in the η vs. λ curve shown in Fig. 7).

The results show that the quantum efficiency ranges between a minimum value of η = 23% at S = 0.3 μm, and a maximum value of η = 31% at S = 1.1 μm. To understand the finger-spacing dependence better, the results have been modeled according to two functions. Model 1 assumes that shadowing only occurs under the metal fingers, while Model 2 assumes that the carriers generated within the exposed n- and p-type implanted regions on either side of the metal fingers also do not contribute to the photocurrent. Mathematically, Model 1 can be described by $\eta \propto (S + W_\mathrm{i} - W_m)/(S + W_\mathrm{i})$, while the formula for Model 2 is $\eta \propto S/(S + W_\mathrm{i})$. The results have then been fitted to the experimental data and plotted in Fig. 10. The fits clearly show that Model 1 matches the data more closely than Model 2, indicating that the exposed part of the implanted regions do not effect the quantum efficiency. This result is encouraging as it suggests that, in optimized geometries, even smaller electrode spacing may be possible before the onset of excessive shadowing limits the ability to obtain acceptable responsivities.

3.4. Pulse response characteristics

The high-frequency properties of the devices have been characterized extensively using impulse response measurements. A diagram of the setup used for these measurements is shown in Fig. 11. The devices were illuminated using a 850-nm mode-locked Ti-sapphire laser, with pulse width of 1-2 psec, pulse repetition rate of 13 nsec,

and a steady-state optical power of ~ 3 μW. The devices were contacted using a microwave probe, and the resulting photocurrent was measured using a high-speed oscilloscope with a 70 GHz sampling head. The data have been analyzed by performing a Fourier transform of the impulse response in order to determine the frequency domain response. For the transformed frequency-dependent characteristics, the frequency response of the bias tee, the electrical probe and 12" cable resulted in a combined attenuation of just over 0.1 dB/GHz. Therefore, in order to make an accurate determination of the detector bandwidth, the responses of these components were deembedded from the frequency-dependent data reported in this paper.

The impulse response for a 10 x 10 μm^2 detector with S = 0.4 μm at V_b = -1 V is shown in Fig. 12, where the voltage developed by the transient photocurrent across the 50-Ω input of the high-speed oscilloscope is plotted vs. time. The response consists of a single sharp peak with full-width half-maximum (FWHM) of only 14.8 psec. This result is in contrast to our previous results for Ge-on-bulk-Si detectors [45], where the main peak is accompanied by a longer-time-scale response, associated with electron-hole pair generation in the Si substrate and subsequent slow diffusion of the deep carriers to the surface contacts. The pulse response for that device, which had similar dimensions (A = 10 x 10 μm^2 and S = 0.34 μm) to the Ge-on-SOI device, is shown in the inset of Fig. 12.

In order to extract the bandwidth of the devices, the Fourier transform of the impulse response has been calculated and the response of the bias tee, probe and cable deembedded as described above. The resulting frequency response is shown in Fig. 13, where the curve has been normalized to equal 0 dB at a frequency of 10 MHz. Also shown in the figure is the (un-deembedded) transform of the pulse response of the Ge-on-

bulk-Si detector that produced the pulse response shown in the inset of Fig. 12. In order to provide a consistent comparison, the un-deembedded response of the Ge-on-SOI detector has also been included in the figure.

The deembedded frequency response of the Ge-on-SOI device indicates a -3 dB bandwidth of 29 GHz, and -6 dB bandwidth of 36 GHz at V_b = -1 V. The response shows very little attenuation at low frequencies, with only ~ 1 dB of attenuation at 20 GHz. On the other hand, due to the carrier generation in the underlying Si layer, the Ge-on-bulk-Si device shows significant attenuation at low frequencies, having -3 dB and -6 dB bandwidths of 1 GHz and 6 GHz, respectively. The fact that the Ge-on-SOI device eliminates this low-frequency tail, and maintains a flat response over a broad frequency range, underscores the advantage of the Ge-on-SOI device design for high-speed operation at λ = 850 nm.

Fig. 14 shows the frequency response for 10 x 10 μm^2 Ge-on-SOI detectors with finger spacing of S = 0.4 μm at V_b = 0, -0.5 and -2.0 V. The plot shows that the bandwidth saturates at very low bias voltages. At V_b = -0.5 V, the bandwidth is 27 GHz, which is nearly the same as the 29 GHz bandwidth obtained at V_b = -2.0 V. Even at V_b = 0, a bandwidth of 25 GHz is determined for these devices. Given the dark current data shown in Fig. 6, these results are very significant, as they indicate that our devices can maintain high speed while operating in a regime of low dark current. The excellent zero-bias operation also suggests that the detectors may be suitable for use in differential amplifier circuit configurations, which can reduce the noise and improve bit error rates for sensitive receiver applications [49].

Impulse response measurements have also been performed on 10 x 10 μm^2 detectors with different finger spacing. The results of these measurements for devices with S = 0.4 μm to 1.0 μm at V_b = -1 V are shown in Fig. 15(a). The plot shows that the FWHM increases with increasing finger spacing, from a value of 14.8 psec at S = 0.4 μm, to values of 16.2, 16.7 and 19.3 psec for devices with S = 0.6, 0.8 and 1.0 μm, respectively. The normalized frequency responses for the same devices are shown in Fig. 15(b). As expected from the pulse response measurements, detectors with the smallest finger spacing have the highest bandwidths. The -3 dB bandwidths extracted from the data in Fig. 15(b) are 29, 27, 22 and 16 GHz, for devices with S = 0.4, 0.6, 0.8 and 1.0 μm, respectively.

Pulse response measurements for detectors with different areas are shown in Fig. 16. Fig. 16(a) shows the impulse response for detectors with A = 10 x 10 μm^2, 20 x 20 μm^2 and 30 x 30 μm^2, for a fixed finger spacing of S = 0.6 μm at V_b = -1 V. The plot in Fig. 16(a) indicates that the device performance slows considerably with larger detector size, with the FWHM increasing from 16.2 psec at A = 10 x 10 μm^2, to 22.3 psec and 30.1 psec for 20 x 20 μm^2 and 30 x 30 μm^2 detectors, respectively. Once again, the transform of the pulse response is shown in Fig. 16(b), where -3 dB bandwidths of 27, 19 and 11 GHz are extracted for devices with respective areas of 10 x 10 μm^2, 20 x 20 μm^2 and 30 x 30 μm^2.

Insight into the speed-limiting mechanisms of the detectors can be gained by an investigation of the finger-spacing dependence of the bandwidth for different device areas. The results of this analysis are shown in Fig. 17 which shows log-log plots of the -3 dB bandwidth vs. finger spacing for the three detector sizes at zero bias and high bias

($|V_b| > 2$ V). The results confirm the performance improvement with decreasing area, as at every finger spacing, the bandwidth increases as the area decreases. However, the devices also show an interesting trend; with decreasing S, the bandwidth tends to increase, then reaches a maximum value, and subsequently starts to decrease again. Furthermore, the finger spacing at which the maximum occurs is different for each detector area. At zero bias, for $A = 10 \times 10$ μm^2, the maximum bandwidth, BW_{max}, occurs for $S = 0.4$ μm, while at $A = 20 \times 20$ μm^2 and 30×30 μm^2, BW_{max} is achieved at $S = 0.6$ μm and $S = 0.7$ μm, respectively. At high bias, BW_{max} occurs at a larger finger spacing ($S = 0.4$, 0.7 and 0.8 μm, respectively) than at $V_b = 0$, and the bandwidth has a less-pronounced finger-spacing dependence at high bias.

The results of Fig. 17 can be understood by modeling the speed-limiting mechanism as being affected by two factors, transit-time delay and RC delay. At zero bias, the transit time delay, τ_t, can be estimated as follows:

$$\tau_t = 0.5 \cdot (W_d^2/V_{bi}) \cdot (1/\mu_e + 1/\mu_h), \qquad (1)$$

where μ_e and μ_h are the respective electron and hole mobilities, W_d is the depletion width, and V_{bi} is the built-in voltage. In a lateral p-i-n geometry, W_d depends not only on S, but on the absorbing layer thickness, t_{Ge}, as well. However, in the limit of $S \gg t_{Ge}$, W_d approaches S, and so (1) can approximated by

$$\tau_t \approx 0.5 \cdot (S^2/V_{bi}) \cdot (1/\mu_e + 1/\mu_h). \qquad (2)$$

The relation in (2) assumes that transport is not limited by velocity saturation, a reasonable assumption at zero bias and large finger spacing. For high bias operation, the device operation approaches the opposite limit, where the transport is expected to be

dominated by velocity saturation. Once again, assuming $W_d \rightarrow S$ for large S, the velocity-saturated transit time delay can be calculated as

$$\tau_t \approx 0.5 \cdot S \cdot (1/v_{sat(e)} + 1/v_{sat(h)}), \qquad (3)$$

where $v_{sat(e)}$ and $v_{sat(h)}$ are the saturated velocities for electrons and holes, respectively. Assuming that the transit-time-limited -3 dB bandwidth, BW_t, equals $(2\pi\tau_t)^{-1}$, then the relations (2) and (3) indicate that, at zero bias, $BW_t \propto 1/S^2$, and at high bias, $BW_t \propto 1/S$. As shown in Fig. 17, the trends predicted by (2) and (3) appear to match the experimental data very well, with bandwidth vs. S characteristics asymptotically approaching the expected power-law behavior in the limit of large S, both at high bias and zero bias.

For small finger spacings, the measured bandwidths deviate from the transit-time limited behavior described above. This deviation is believed to be due, in large part, to the onset of RC-limited performance. This conclusion is supported by the area-dependent results in Fig. 17, where larger-area devices deviate from transit-time limited performance at higher values of S than smaller-area devices. In order to confirm this trend, admittance measurements were performed at 1 MHz on the devices to determine the capacitance as a function of finger spacing at different bias voltages. The results are shown in Fig. 18(a), which plots the capacitance vs. finger spacing at V_b = 0 and -1 V. In this figure, the capacitance of an open-circuit probe pad geometry have been subtracted in order to determine the intrinsic device capacitance. The figure shows that the capacitance scales with increasing device area and also increases with decreasing S. As expected, the zero-bias capacitance is also consistently higher than the capacitance at V_b = -1 V.

From the capacitance measurements, a rough calculation of the RC-limited bandwidth, BW_{RC}, can be determined by assuming $BW_{RC} = (2\pi\tau_{RC})^{-1}$, where τ_{RC}, $= R \cdot C$. For these calculations, we assume that C is equal to the capacitance values in Fig. 18(a), and $R = 50\ \Omega$, which is simply the resistance of the terminating load. The value of BW_{RC} calculated in this manner is only an estimate, due to additional series resistance components that may be present, and uncertainty as to the effect of the probe pads on the admittance at microwave frequencies. Nevertheless, Fig. 18(b) plots BW_{RC} vs. S for the three different device areas at $V_b = 0$ and -1 V. The plot shows that the values of BW_{RC} extracted from the 20 x 20 μm^2 and 30 x 30 μm^2 detectors agree quite well with the experimental data for the same detector areas shown in Fig. 17, both at $V_b = 0$ and -1 V, suggesting that the performance of the large-area detectors is indeed RC-limited at small S. For the 10 x 10 μm^2 devices, the extracted BW_{RC} values are much higher than the measured bandwidths. This discrepancy is likely due to the effect of the probe-pad capacitance, which is neglected in our calculation. This result suggests that the RC-limited performance of the 10 x 10 μm^2 detectors could be improved further by reducing parasitics associated with the probe-pad geometry. Clearly, additional microwave s-parameter measurements are needed to clarify the impact of the probe pads on the RC-limited performance and more accurately determine the intrinsic bandwidth limitations of these devices.

IV. DISCUSSION

4.1. Overall performance assessment

As discussed at the start of section II, the properties needed for integrated photodetectors are high speed, high responsivity, low dark current, and low operating voltage. Since it is important that these all of these figures of merit are achieved at the same time, we have made an attempt to assess the ability of our Ge-on-SOI detectors to simultaneously provide these performance requirements. To do this, we have first identified the device dimensions and operating conditions that provide the optimum performance. The results of this analysis are shown in Fig. 19, where the bandwidth-efficiency product of the 10 x 10 μm^2 detectors is plotted as a function of finger spacing for bias voltages ranging from V_b = 0 to -2 V. In this analysis, the data of Figs. 7 and 10 have been utilized to calculate the maximum efficiency as a function finger spacing corresponding to the responsivity maximum at λ = 895 nm.

The plot in Fig. 19 shows that the highest bandwidth-efficiency is achieved at S = 0.4 μm for V_b = 0, but at $|V_b| \geq 0.5$ V, the maximum shifts to S = 0.6 μm. This shift occurs due to the fact that the devices with S = 0.4 μm have lower efficiency as a result of the increased shadowing factor of the metal fingers as described in Fig. 10. At zero bias, the devices with S = 0.4 μm have higher bandwidth than at S = 0.6 μm, which compensates for the lower efficiency. However at higher bias, the devices tend to have similar bandwidths, giving the device with S = 0.6 μm the overall bandwidth-efficiency advantage. At V_b = 0 and -0.5 V, bandwidth-efficiency products of 10.4 GHz and 11.6 GHz are obtained for S = 0.4 μm, while at V_b = -0.5 V and -1.0 V, the S = 0.6 μm device produces bandwidth-efficiency values of 12.3 GHz and 12.4 GHz, respectively.

Further increasing the bias up to -4 V enables bandwidth-efficiency products as high as 13.2 GHz [48], but as will be described next, the slight improvement in the performance is offset by the much higher dark current that occurs at these voltages.

Finally, the results can be combined with the dark current data to determine the optimum operating voltage. The devices with $S = 0.6$ μm have a low I_{dark} value of 7 nA at $V_b = -0.5$ V, but a bandwidth of only 25 GHz. At $V_b = -1$ V, the bandwidth increases to 27 GHz, with only a slight increase in I_{dark} to 24 nA. For $|V_b| > 1$ V, the bandwidth increases only marginally, going up to 29 GHz at $V_b = -4$ V. However at $V_b = -4$ V, the dark current exceeds 9 μA, making it impractical to operate the devices at such a high bias. The optimum performance metrics for the 10 x 10 μm^2 detectors with $S = 0.4$ μm and 0.6 μm are summarized in Table 1. The results clearly show that the Ge-on-SOI detectors, in their current state, can meet the simultaneous performance requirements needed for integrated optical interconnect applications at 10 Gbit/sec and higher. Recently, these predictions have been confirmed by measurements of Ge-on-SOI detectors integrated with CMOS receiver circuits that display sensitivities of -11.0 dBm 12.5 Gbit/sec [50] and operate error-free to data rates as high as 19 Gbit/sec [51].

4.2. Outlook for improved performance

Despite the excellent performance of the current detector technology, it is important that a pathway exists to improve the device performance even further for future applications. In this section we describe how the performance can be optimized, not only for operation at λ = 850 nm, but at longer wavelengths as well.

The simplest and most obvious method of improving the performance is through the use of an ARC. The simulations shown in Fig. 7 indicate that with no other modification

to the structure, a properly designed SiN_x ARC could improve the external quantum efficiency by a factor of 1.3x (2.0x) at λ =895 nm (850 nm). This improvement alone could increase the bandwidth-efficiency product to over 20 GHz, though the possible adverse effects of the SiN_x ARC on the parasitic capacitance of the device would need to be evaluated.

The efficiency of the devices, particularly at longer wavelengths, could also be improved dramatically by optimizing the layer structure design and post-growth annealing process. As described previously, substantial up-diffusion of Si into the Ge likely occurs due to the aggressive cyclic annealing utilized to reduce the defect density. Therefore, reduction of the underlying SOI layer thickness could help to limit the amount of Si available for diffusion during this process. Furthermore, recent results have shown that such aggressive annealing may not be necessary and that reduced defect density can be achieved by the use of lower-temperature annealing, as well as selective-area growth. As shown in Fig. 7, an optimized process with minimal Si/Ge mixing could result in values of $\eta > 20\%$ at $\lambda = 1300$ nm.

Much greater improvements in the device efficiency can be achieved by a complete optimization of the entire layer stack. We have performed such an optimization using transfer matrix calculations on the idealized layer structure shown in Fig. 8. The results of this study are shown in Fig. 20 where the maximum quantum efficiency is plotted vs. Ge thickness, where at each x-axis value, the thicknesses of the SiN_x and SiO_2 layers have been tuned for maximum absorption in the Ge layer. This plot indicates that not only can much higher efficiencies be achieved utilizing the current absorbing-layer thickness (~ 400 nm), but that with proper tuning, much thinner Ge layers can be utilized

to achieve the same responsivity as the current detectors. For instance, Fig. 20 shows that quantum efficiencies of 50% (not including shadowing) can be achieved for Ge thickness of only 100 nm. If the finger spacing were correspondingly reduced to S = 100 nm, it is conceivable that tremendous improvements in the bandwidth could also be achieved. Performance improvement at such smaller finger spacings would, however, require reduction of the intrinsic junction capacitance, or a significant reduction in the metallization resistance. At least some improvement in these parameters should be possible due to the non-optimized fabrication process utilized for the current devices. Finally, the results in Fig. 20 also show that, with proper optimization of the absorbing layer thickness, the prospects for efficient detector operation at λ = 1300 nm can be greatly improved. For instance, the results of Fig. 20 predict that quantum efficiencies as high as 40% can be expected at λ = 1300 nm for Ge absorbing layer thicknesses of only for 310 nm.

It is important to remember that the optimization study assumes that the Si layer beneath the Ge absorbing region can be reduced to arbitrarily thin layers. Though some promise for creating "pure" Ge-on-insulator exists, either through wafer bonding [52] or novel epitaxial techniques [53], using the current direct Ge growth process, a minimum SOI layer thickness of ~ 10 nm would probably need to be maintained. Also, in order to realize speed improvements by correspondingly reducing the finger spacing and Ge layer thickness, the RC-limited delay time would have to be reduced. Such improvement may be possible in thin Ge layers due to the reduced fringing capacitance associated with the deep n- and p-type contacts. The device area can be reduced as well, though further reduction of the device size could make the use of lensed fibers or integrated lenses

necessary to allow efficient optical coupling into the detector, and may lead to alignment difficulties with the optical fiber as well.

Finally, although our single-buried-oxide Ge-on-SOI design is advantageous due to its compatibility with current CMOS technology, the results in Fig. 20 show that this structure has little prospect for achieving efficiencies much greater than 10% at λ = 1550 nm. Despite the fact that our model does not include strain effects that can improve absorption at longer wavelengths [54], alternative geometries may still have to be utilized for optimal operation at 1550 nm. Recently very promising results have been obtained by Dosunmu, *et al*. [55], who demonstrated Ge-on-SOI Schottky detectors with η = 59 %, at λ = 1550 nm, and bandwidths as high as 12 GHz. The resonant-cavity photodetector concept can also be applied to Ge-on-SOI detectors, and promising results using Ge on double-buried oxide structures have recently been demonstrated [56]. Finally, another possible alternative to achieving efficient absorption at λ = 1550 nm in Ge is the use of a waveguide geometry similar to those utilized for Si and strained SiGe detectors [17], [29]-[32], [34]-[35]. The use of Ge in a waveguide fashion is very advantageous due to the relatively-short absorption length of 10 μm at λ = 1550 nm, which could allow low-capacitance geometries to be realized. This structure is also compatible with other SOI-based optical devices such as modulators and switches that have been intensely studied in recent years due to their promise for realizing fully integrated optical systems on Si substrates [57].

V. CONCLUSIONS

In conclusion, we have demonstrated the feasibility of high-performance infrared detectors based upon Ge-on-SOI technology that are suitable for integrated optical interconnect applications in high-performance servers. For operation at $\lambda = 850$ nm, the devices meet all of the requirements of integrated detector operation, including high speed, high efficiency, low operating bias, and low dark current. The Ge-on-SOI detector design has potential for integration with standard CMOS, and should be extendable to even higher speeds, and operation at longer wavelengths. Continued investigation into these devices is needed however, particularly to develop integration strategies with CMOS, as well as to understand and improve yield and reliability issues for Ge-based devices in a manufacturing environment. Nevertheless, the approach we have developed has tremendous potential not only for integrated optical interconnects but also to serve as a basic high-speed detector platform for a wide range of novel Si-based optoelectronic applications.

BIOGRAPHIES

Steven Koester was born in Defiance, Ohio in 1966. He joined IBM in 1995, and has over 15 years of experience in the field of semiconductor device research. Since 1997, he has performed research on group-IV heterostructure materials and devices, with an emphasis on strained-layer field-effect transistors and photodetectors. Prior to 1997, Dr. Koester worked as a postdoctoral researcher on the fabrication and characterization of nanostructured devices in Si/SiGe strained-layer materials. Before joining IBM, Dr. Koester was a research fellow at the University of California, Santa Barbara. There he performed research involving the fabrication of quantum devices in the InAs/AlSb heterostructure system. He also received M.S.E.E and B.S.E.E. degrees from the University of Notre Dame in 1991 and 1989, respectively. Dr. Koester has authored or co-authored over 80 technical publications and conference presentations. He also holds 9 United States patents.

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Gabriel Dehlinger graduated magna cum laude from the University of Tübingen in 1997. He received the Ph.D. degree in 2001 from the Swiss Federal Institute of Technology Zürich, in the solid state group of Prof. Ensslin. His thesis research was performed in the Laboratory of Micro- and Nanotechnology at the Paul-Scherrer-Institute, on the subject of vertical transport and intersubband emission in SiGe resonant tunneling diodes and quantum cascade structures. In 2001, he joined IBM Research, working on direct growth of Ge on Si using UHV-CVD, and on the processing and measurement of Ge high-speed photodetectors. He joined Infineon in 2003, where he is currently a staff engineer in Villach, Austria, working on high-power bipolar transistor technology development.

Jack Chu is a Research Staff Member at the IBM T. J. Watson Research Center. He received the B.S. degree in chemistry from Princeton University in 1978, and M.S. and Ph.D. degrees in chemistry from Columbia University in 1980 and 1984, respectively. Dr. Chu joined IBM at the Thomas J. Watson Research Center, Yorktown Heights, New York, as a Postdoctoral Fellow in 1986 where his early work was in the field of chemical dynamics investigating the gas-phase reactivity of transient species such as SiH_2 relevant to the silicon CVD growth process. While at IBM, he has been involved in the development and application of the Ultrahigh Vacuum/Chemical Vapor Deposition (UHV/CVD) technique to fabricate various type of metastable silicon alloys (Si:Ge, Si:B, SiGe:B, SiGe:P, Si:C, and SiGe:C) and strained Si/SiGe/Ge structures with applications to high performance bipolar and field effect devices. He has authored and co-authored over 160 publications, including one book chapter in the microelectronics field and holds over 45 U.S. patents. He has received an IBM Research Division Award for his work on understanding silylene gas phase dynamics, and is a recipient of an IBM Outstanding Technical Achievement Award for high mobility electron and hole transports in SiGe structures. Recently, he earned the distinction as a 2005 Master Inventor at the T. J. Watson Research Center.

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Finger spacing (μm)	Bias (V)	Ext. QE at 850 nm (%)	Ext. QE at 895 nm (%)	Responsivity at 850 nm (A/W)	Responsivity at 895 nm (A/W)	BW (GHz)	I_{dark} (nA)	Area (μm^2)
0.4	-0.5	30	42	0.21	0.30	27	8	10 x 10
“	-1.0	“	“	“	“	29	85	“
0.6	-0.5	33	46	0.23	0.33	25	7	10 x 10
“	-1.0	“	“	“	“	27	24	“

Table 1. Performance metrics for Ge-on-SOI detectors indicating simultaneous achievement of high bandwidth, high efficiency / responsivity, low dark current and low operating bias.

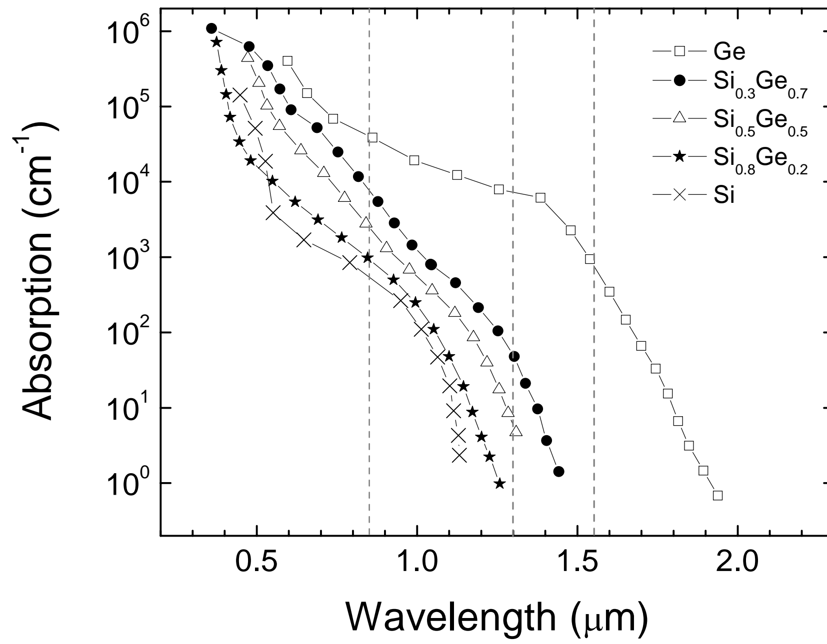

Fig. 1. Plot of absorption coefficient vs. wavelength for relaxed SiGe layers, with Ge concentration ranging from 0% (Si) to 100% (Ge) [4],[6]-[7].

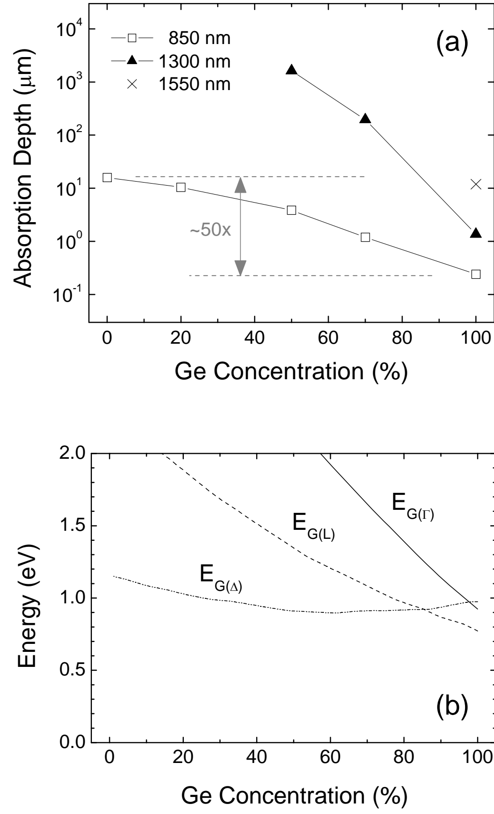

Fig. 2. (a) Plot of absorption depth vs. Ge concentration for SiGe alloys at three different wavelengths. (b) Calculated energy gaps in SiGe as a function Ge concentration between the valence-band aximum and the L-, Δ, and Γ-point conduction band local minima [8].

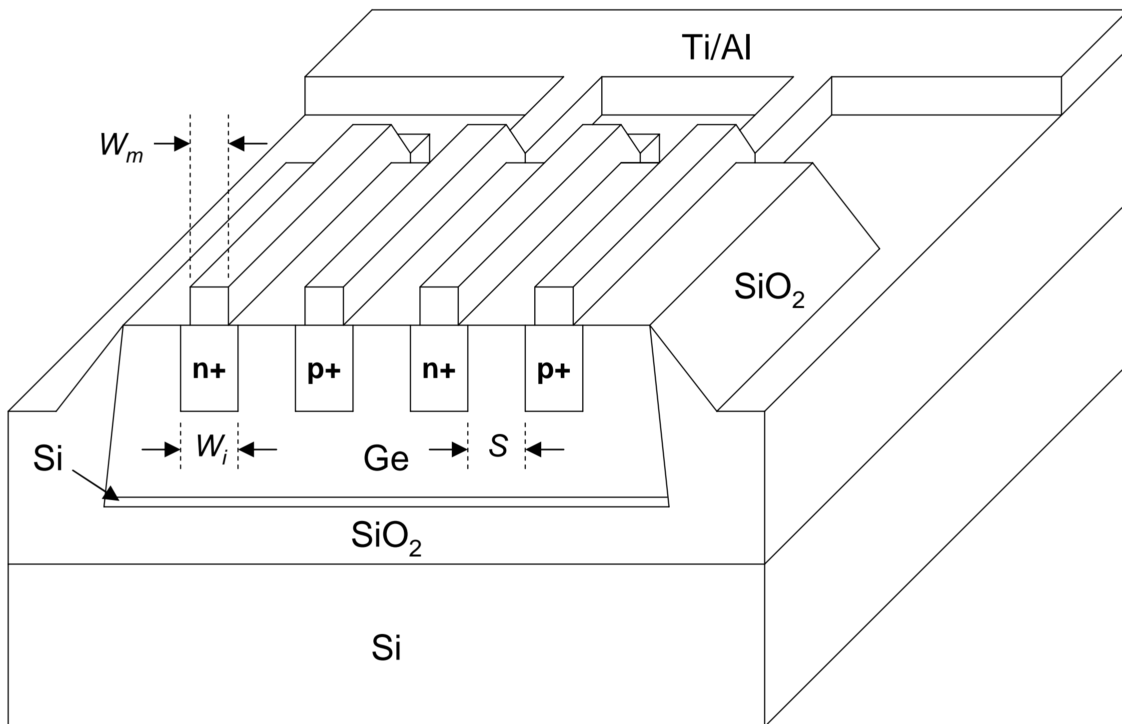

Fig. 3. Schematic diagram of Ge-on-silicon-on-insulator (Ge-on-SOI) photodetector structure. The figure is not drawn to scale.

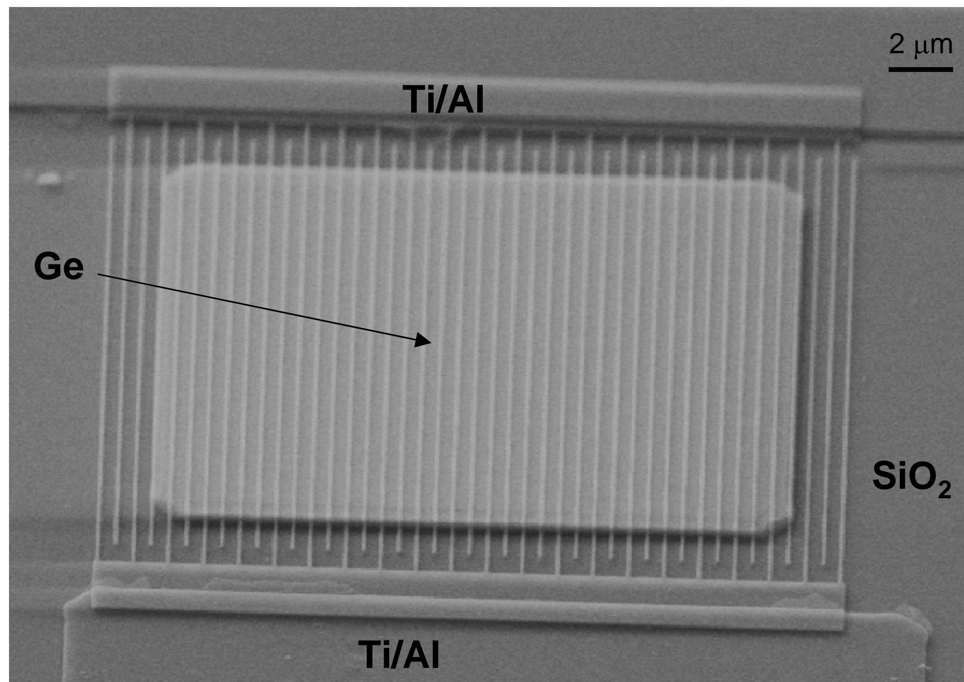

Fig. 4. Tilted-view SEM micrograph of completed Ge-on-SOI photodetector with mesa area of 20 x 20 μm^2 and implant spacing of 0.3 μm. The width of the metal fingers is 0.2 μm.

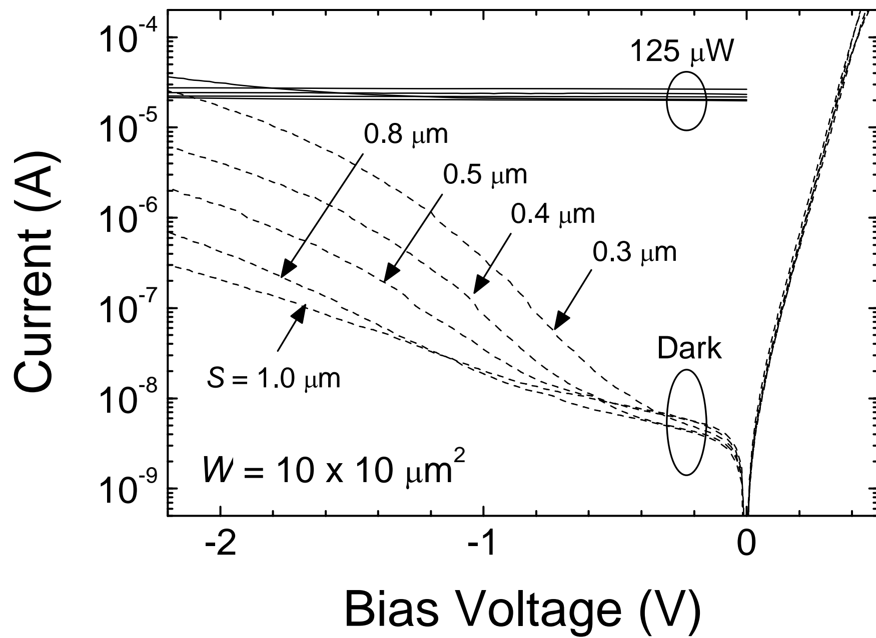

Fig. 5. Current-voltage characteristics of 10 x 10 μm^2 photodiodes with finger spacings, *S*, ranging from 0.3 to 1.0 μm. The plot shows both the dark current and photocurrent from a 822-nm source, using the illumination scheme described in the text.

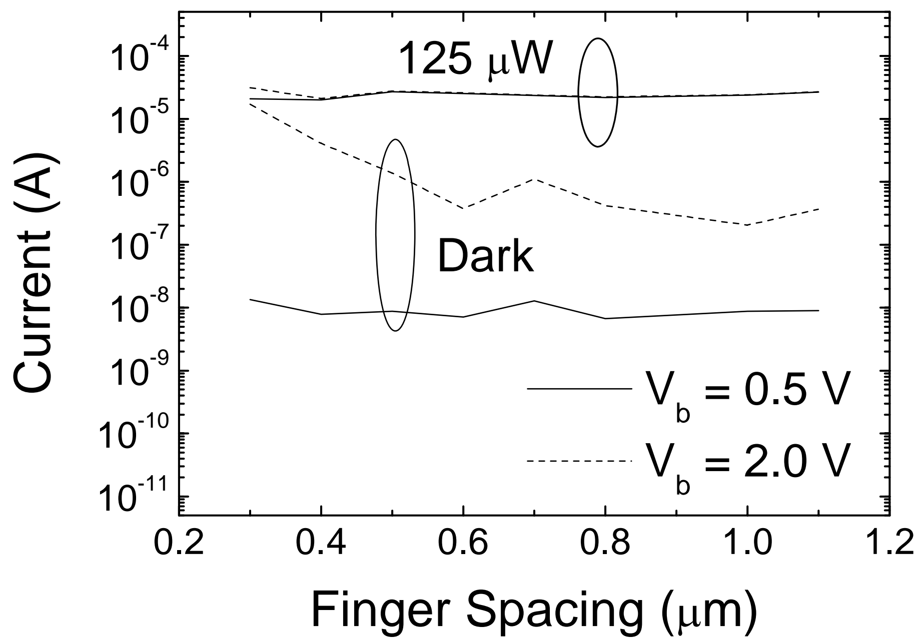

Fig. 6. Plot of dark current and photocurrent as a function of finger spacing for two different applied bias voltages, V_b. The dark current is essentially independent of finger spacing at V_b = -0.5 V.

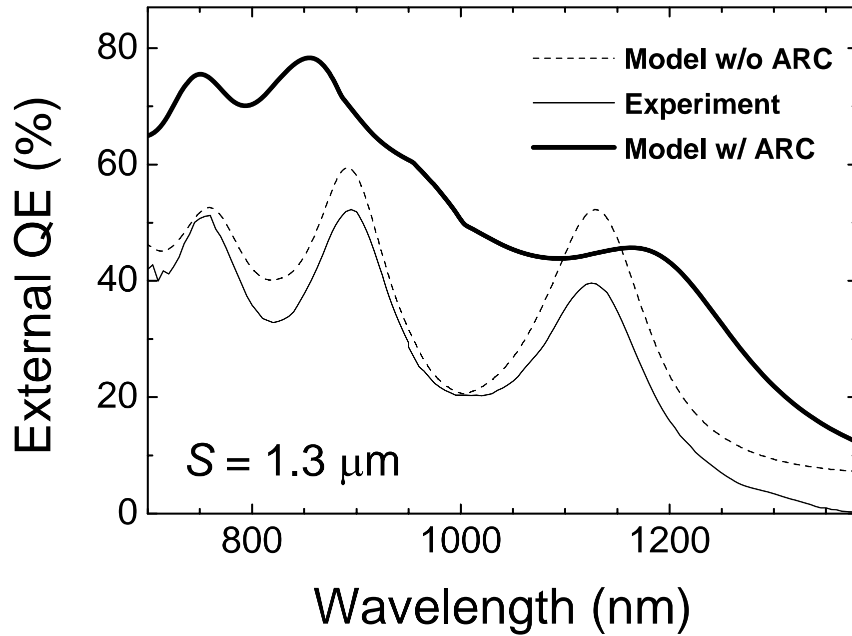

Fig. 7. Measured external quantum efficiency for a Ge-on-SOI detector with 30 x 30 μm^2 area and finger spacing, *S*, of 1.3 μm. Also shown is the calculated efficiency with and without a SiN_x (n = 2) anti-reflection coating. The calculated results have been scaled by a factor of 0.87 to account for the shadowing from the metal fingers.

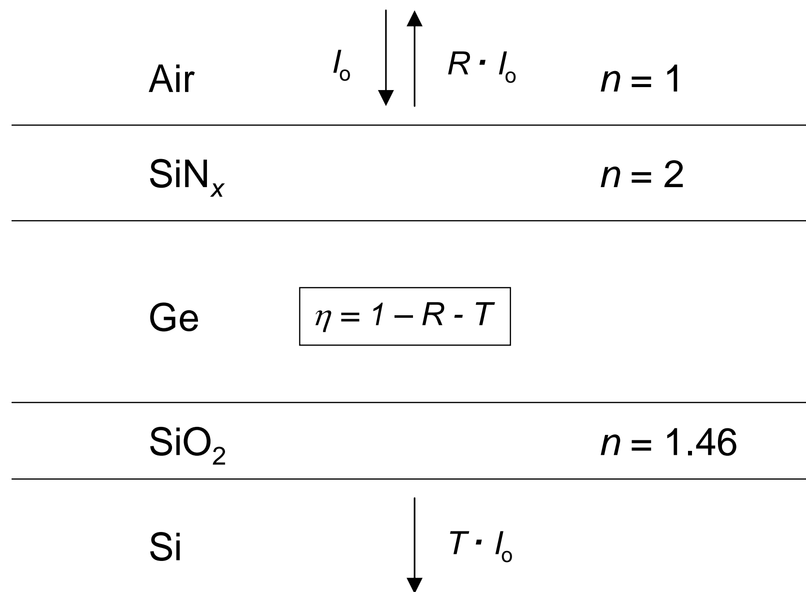

Fig. 8. Diagram of layer stack utilized for transmission matrix calculations of the detector quantum efficiency shown in Fig. 7.

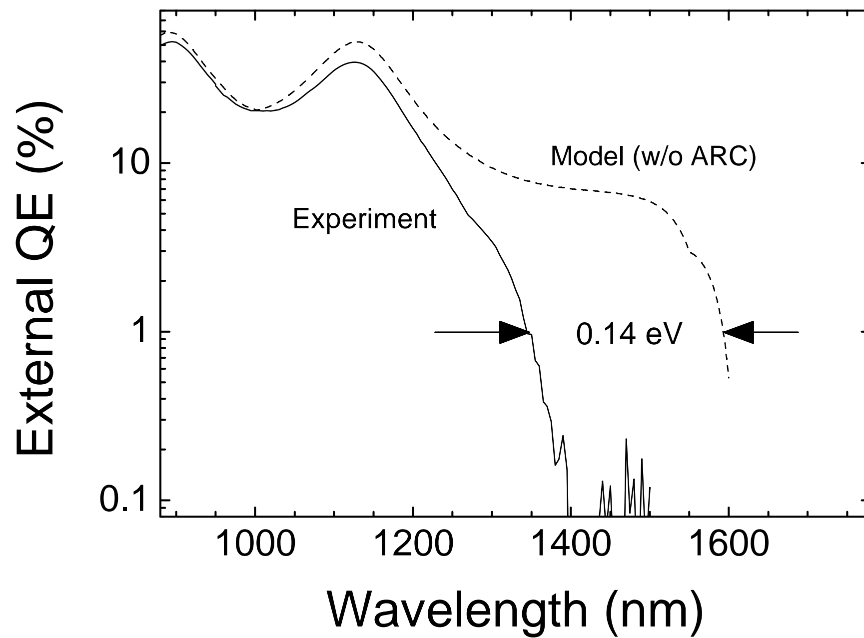

Fig. 9. Semi-log plot of measured and calculated external quantum efficiency for a 30 x 30 μm^2 Ge-on-SOI detector with finger spacing, *S*, of 1.3 μm. The difference between the measured and expected cutoff wavelength corresponds to an energy difference of 0.14 eV.

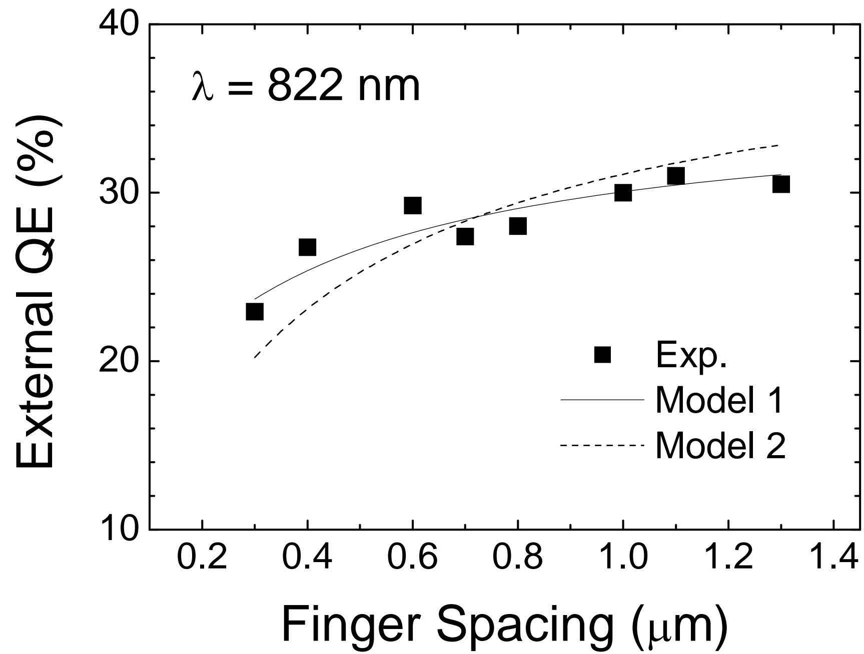

Fig. 10. Plot of external quantum efficiency for Ge-on-SOI photodetectors as a function of finger spacing at $\lambda = 822$ nm, along with two different electrode shadowing models described in the text. The wavelength corresponds to a minimum in the efficiency as shown in Fig. 7.

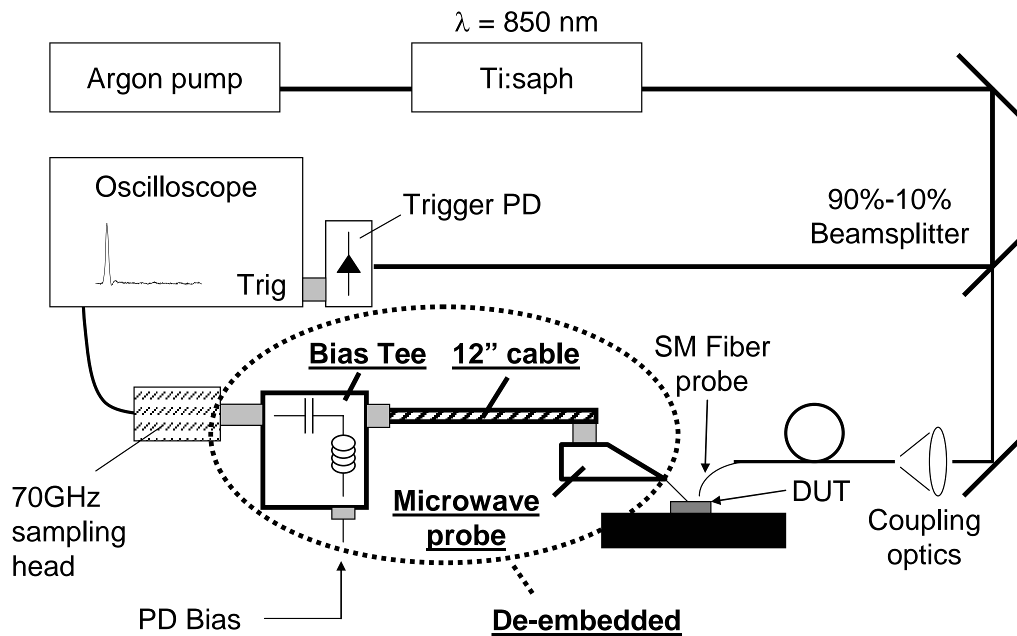

Fig. 11. Diagram of test setup used for the impulse response measurements. The responses of the items indicated in bold have been deembedded from the transformed frequency response characteristics.

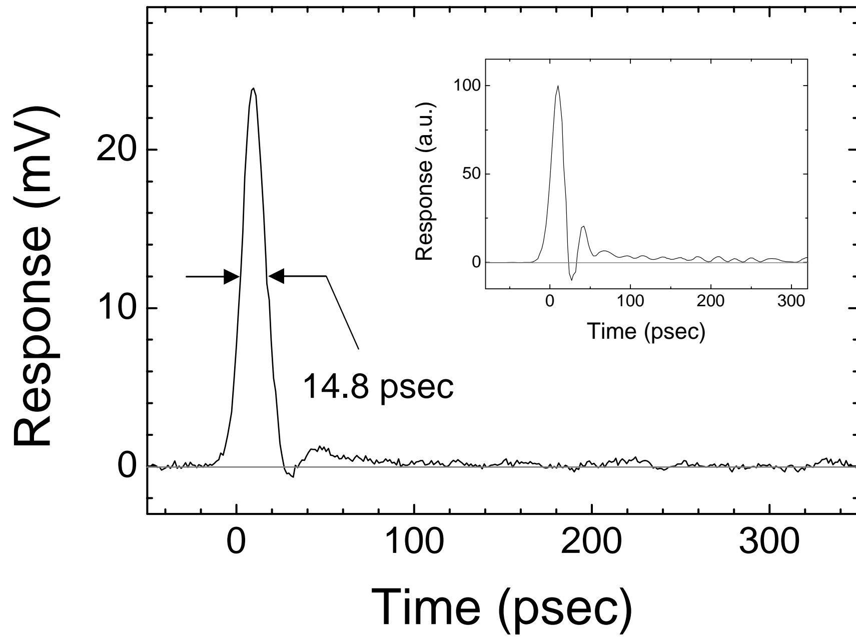

Fig. 12. Impulse response of a 10 x 10 μm^2 Ge-on-SOI detector with finger spacing, *S*, of 0.4 μm at a bias of -1 V and wavelength of λ = 850 nm. Inset: Impulse response for a similar 10 x 10 μm^2 Ge-on-bulk-Si detector with *S* = 0.34 μm.

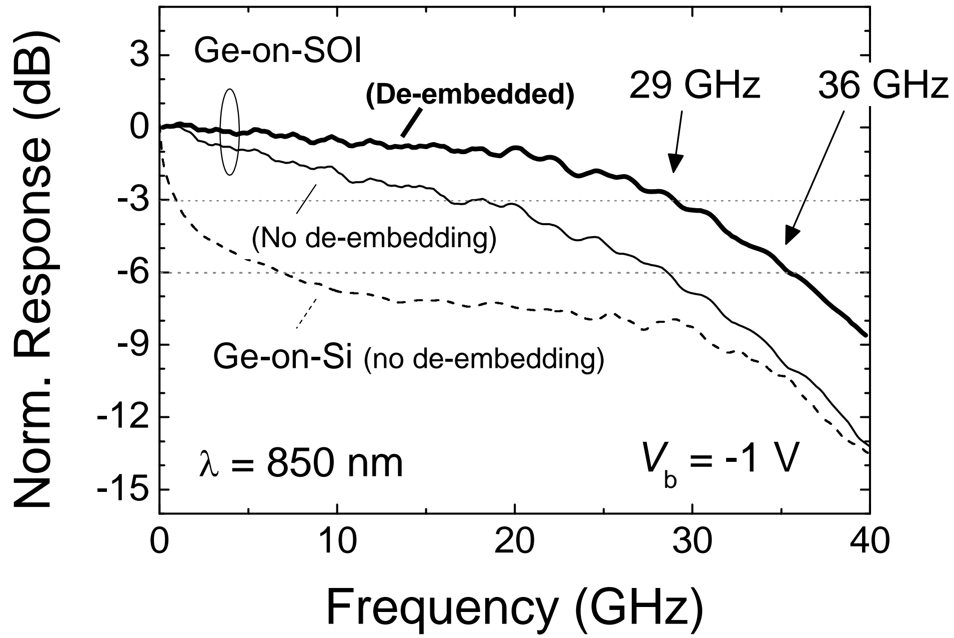

Fig. 13. Normalized Fourier transforms of the impulse responses from the Ge-on-SOI and Ge-on-bulk-Si photodetectors shown in Fig. 12. The curve for the Ge-on-bulk-Si device has not been de-embedded, while the transforms both with and without de-embedding are shown for the Ge-on-SOI device.

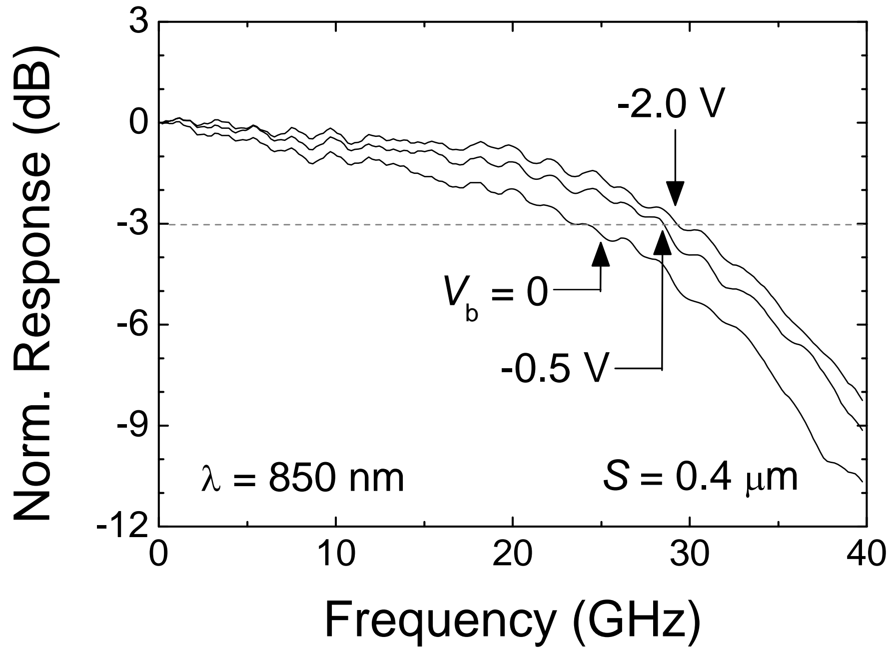

Fig. 14. Normalized frequency response for a 10 x 10 μm^2 Ge-on-SOI detector with S = 0.4 μm at bias voltages of 0, -0.5 and -2.0 V, showing -3 dB bandwidths of 25, 27 and 29 GHz, respectively.

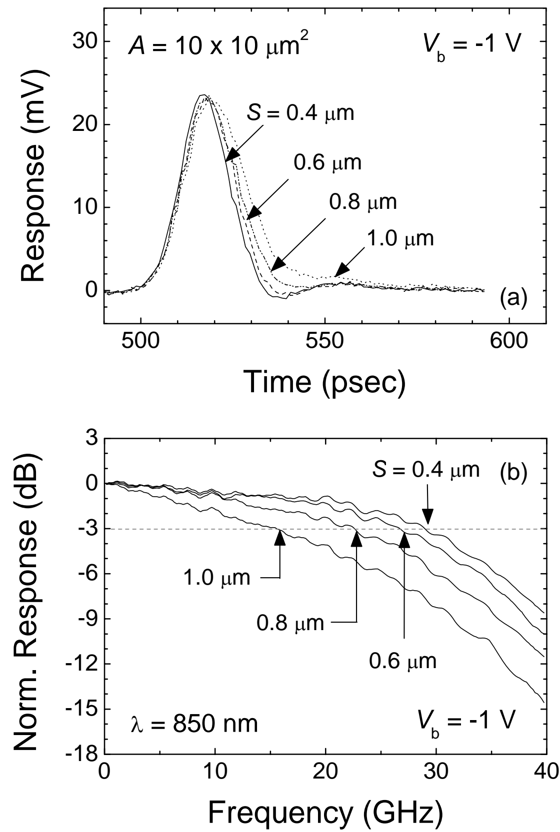

Fig. 15. (a) Impulse response, and (b) corresponding normalized frequency response of 10 x 10 μm^2 Ge-on-SOI detectors with finger spacings, S, ranging from 0.4 μm to 1.0 μm, at V_b = -1 V and λ = 850 nm.

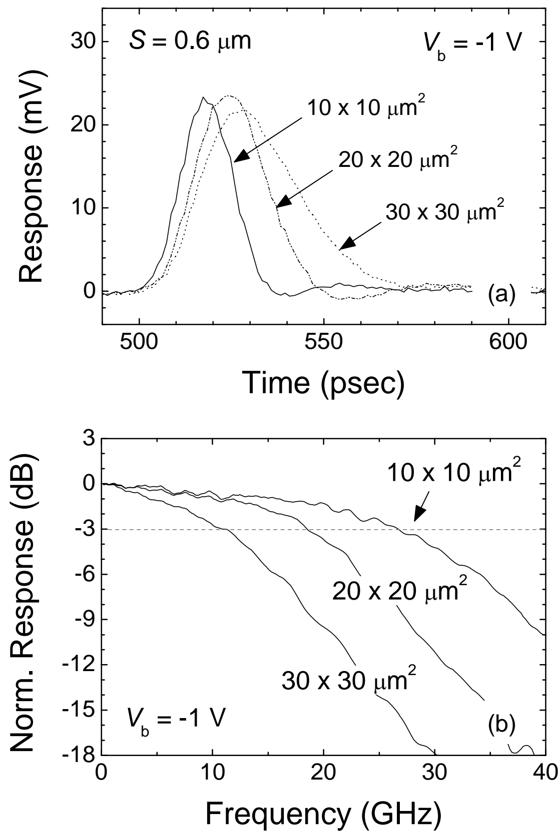

Fig. 16. (a) Impulse response, and (b) corresponding normalized frequency response of Ge-on-SOI detectors with S = 0.6 μm, and device areas ranging from 10 x 10 μm^2 to 30 x 30 μm^2 at V_b = -1 V and λ = 850 nm.

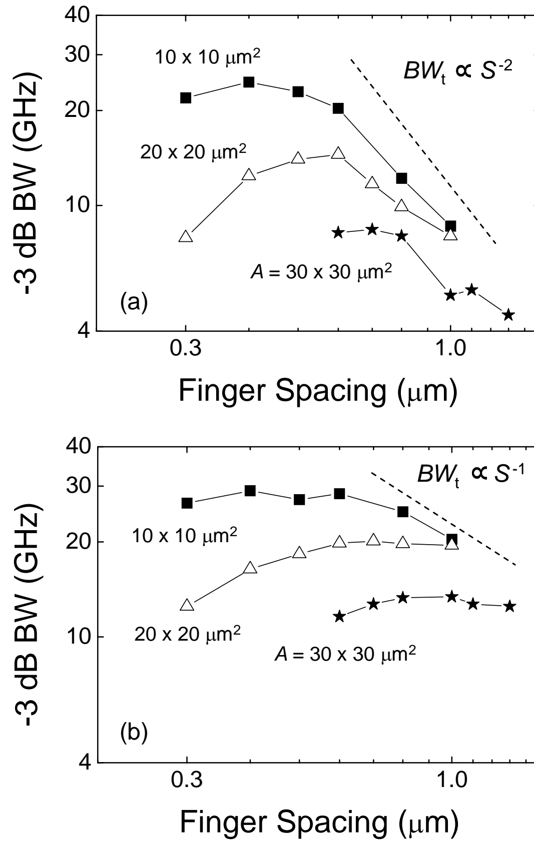

Fig. 17. Log-log plot of -3 dB bandwidth vs. finger spacing for detectors with different areas at (a) zero bias and (b) high bias ($|V_b| > 2$ V).

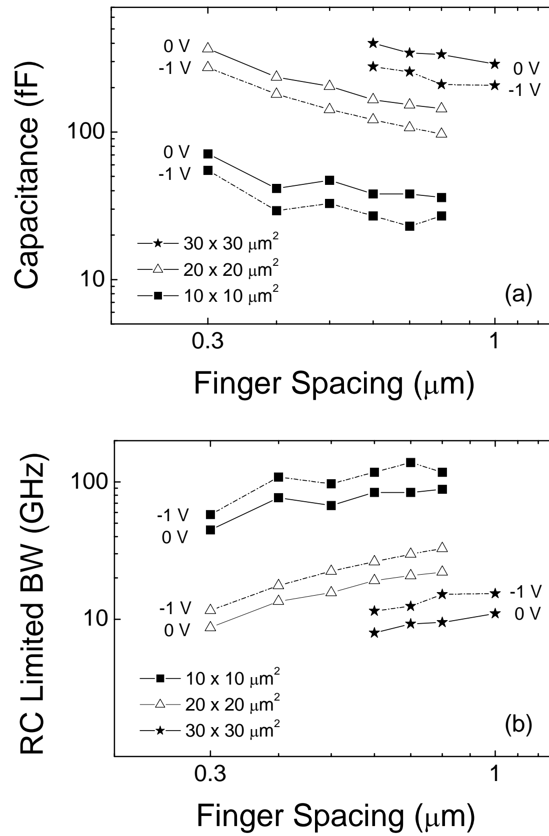

Fig. 18. (a) Device capacitance and (b) RC-limited bandwidth plotted vs. finger spacing at $V_b = 0$ and -1 V for devices with areas ranging from 10 x 10 μm^2 to 30 x 30 μm^2.

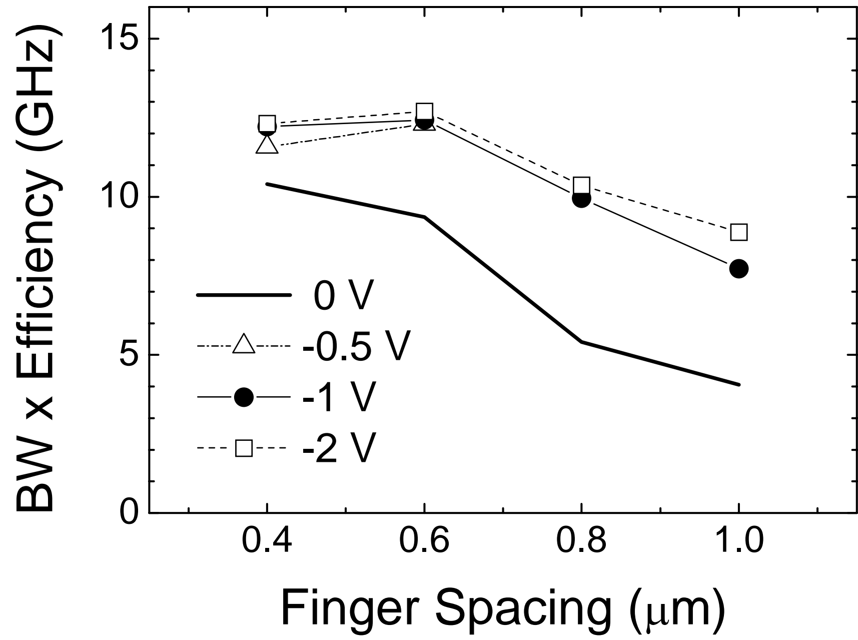

Fig. 19. Maximum bandwidth-efficiency product (at λ = 895 nm) plotted vs. finger spacing for 10 x 10 μm^2 Ge-on-SOI detectors at various bias voltages.

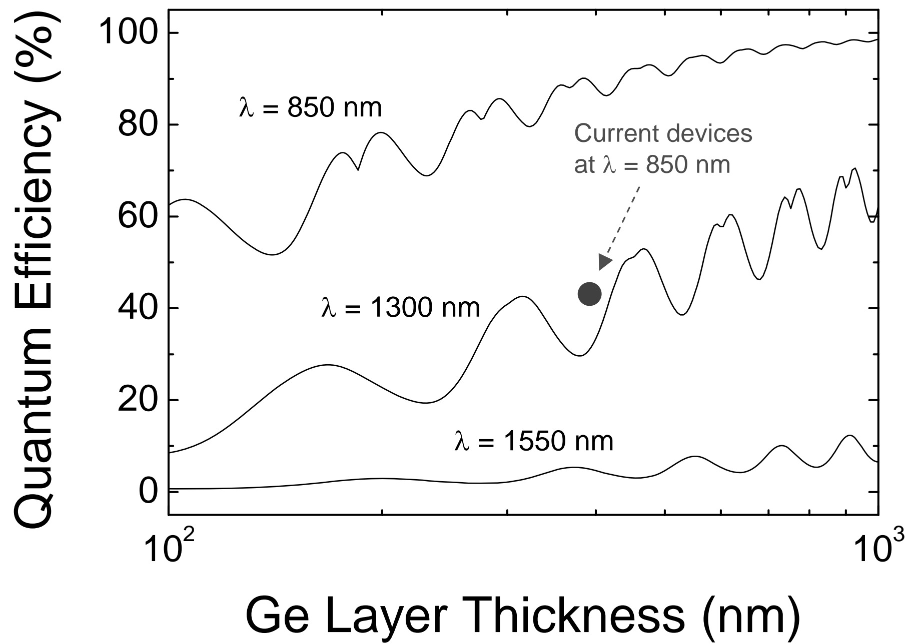

Fig. 20. Plot of calculated optimum quantum efficiency as a function of Ge thickness at λ = 850 nm, 1300 and 1550 nm, using the model layer structure in Fig. 8. No shadowing from the metal fingers has been assumed for these calculations.