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Fabrication of Silicon-on-Insulator (SOI) and Strain-Silicon-on-Insulator (sSOI) Wafers Using Ion Implantation

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CMOS devices fabricated on silicon-on-insulator (SOI) substrates are the key drivers for increased chip speed, lower voltage operation and increased resistance to cosmic ray induced 'soft error" events. Further device performance is achieved when a SOI layer is strained either locally or globally in tensile or compressive state. The most economical method to form SOI and sSOI of less than 200 nm for commercial applications, rely on oxygen implantation at elevated temperatures followed by > 1300^{o} C anneal. This method is known as SIMOX (Separation by IMplantation of Oxygen). Other methods to form SOI and sSOI wafers typically use a "layer transfer" process, where high dose implants of light ions are used, either alone or in combination with other processes, to form a weakened layer which is split off from a "donor" wafer. The "donated" layer of Si or strained-Si, is typically combined with an insulator layer, is bonded to a "handle" Si wafer, forming the final SOI or sSOI wafer. This chapter will describe these implantation methods and some of the applications of SOI and sSOI for advanced electronic and photonic devices.

Contents

1.0 Introduction: SOI transistors

Silicon-on-insulator (SOI) devices were first developed for early satellite and man-in-space exploration systems in the 1960's. The main advantage of SOI devices was their resistance to ionization from solar wind radiation and voltage isolation of the chips. Although most of the early SOI devices were made with Silicon-on-Sapphire (SOS) wafers, a process for making SOI wafers by direct ion implantation of high-dose oxygen, SIMOX (Separation by IMplantation of Oxygen), was developed in the later 1970's [Izumi78].

Today, SOI is used for CMOS microprocessors (IBM's PowerPC family, AMD's Opteron, memories (SRAM) and logic circuits including highly advanced game chips (Microsoft's Xbox and Sony's play station) to achieve high performance and reduced standby power. Compared to similar circuits on bulk Si, SOI CMOS can run at 20 % or higher switching speed and with nearly x 2 lower power requirements.

The structure of a SOI CMOS is shown in Figure 1-1. The MOS transistor is fabricated in a thin layer of crystalline Si that is isolated from the main bulk of the Si wafer by a dielectric (insulating) layer, which is usually SiO_2 [Fig.1-2].

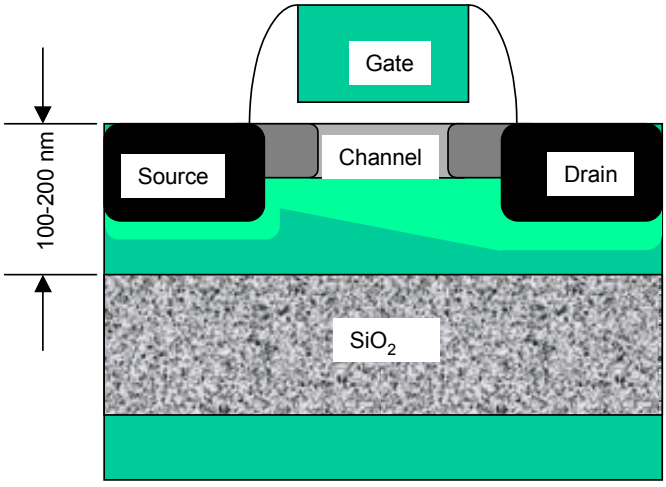


***Figure 1-1. Schematic diagram of a "partially-depleted" SOI-MOS transist*or.**

The thickness of the Si-device and buried oxide layers for SOI wafers vary over several orders of magnitude, depending on the applications [Fig. 1-2]. "Thick" SOI wafers (with Si layers thicker than 1 um) are used for a wide variety of power switching devices, high-speed bipolar circuits and MEMS (Micro-Electro-Mechanical-Systems). CMOS devices are built on SOI wafers with Si layer thickness ranging from "thin" 50 to 300 nm, to "ultra-thin", 10 to 50 nm, down to "thin-body" devices in "nano-SOI" with Si layers thinner than 10 nm.

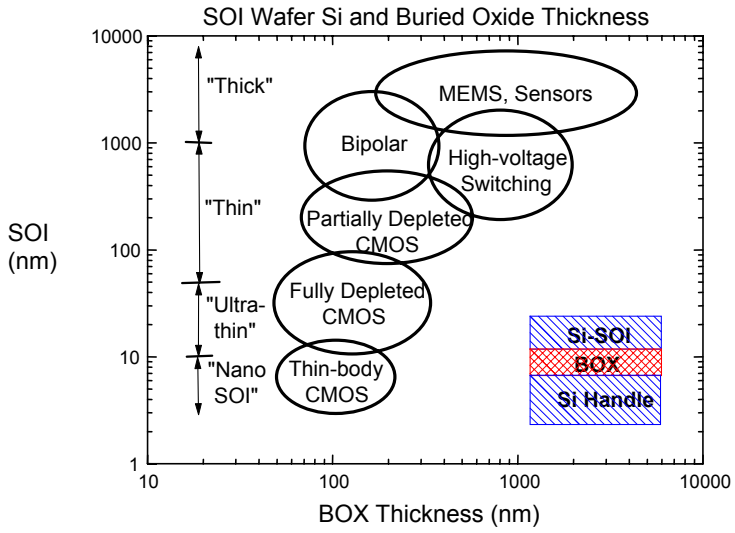


Figure 1-2. Si device layer and buried oxide layer thickness for various types of SOI wafers.

An increasing important advantage of SOI devices is the relatively low probability of "soft error" signal upsets compared to devices on bulk Si. A soft error can occur when an energetic secondary particle, generated in the upper atmosphere by a collision of a gas nucleus with a cosmic ray, collides

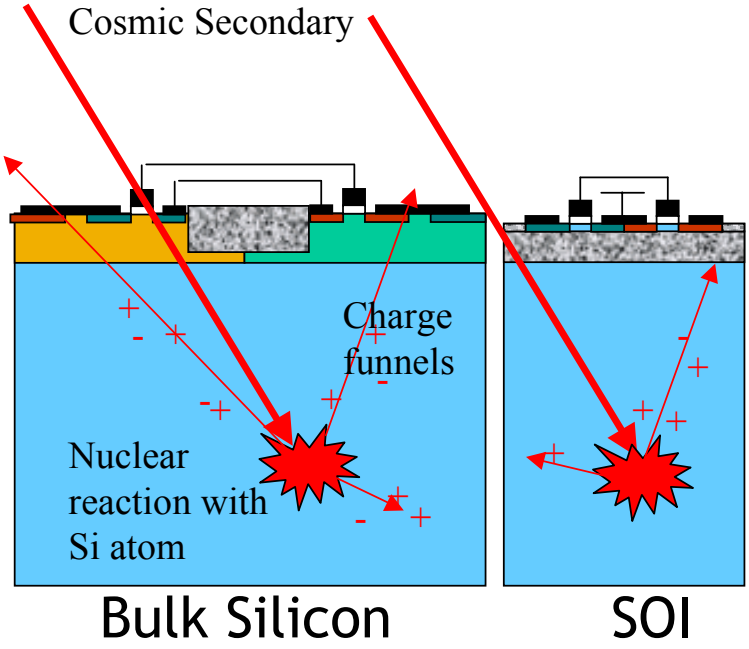


Figure 1-3. Schematic of "soft error" effects for CMOS devices in bulk Si and SOI wafers.

with a Si atom in a chip [Fig. 1-3]. If a nuclear reaction occurs, a large number of reaction products are produced by the disintegration of the Si nucleus. These reaction products generate ionization trails in the Si die which, if they reach the transistor and memory storage layer, can alter the charges in the IC

device leading to an unanticipated change in the signal state. This has long been a major issue for large data systems [Ziegler96] and is a concern for high-data rate transmission networks as well. The probability of a soft error failure is to first order proportional to the volume of Si which is in electrical contact with the device region. Since the thickness of a typical Si-SOI layer is ~ 0.1um and a 200 mm wafer is ~ 725 um thick the volume of Si which is above the buried oxide layer is ~2.5% of that under a device in a bulk Si chip. SOI devices can be influenced by other radiation-related effects, but the large relative resistance to soft-errors is a significant advantage over bulk Si circuits [Liu99].

SOI CMOS transistors are classified by the thickness of the SOI layer relative to the depths of the junctions and depletion layers in the power-up device [Fig. 1-4]. "Partially-depleted" CMOS transistors are formed in SOI layers which are thicker than the depth of the depletion region of the channel [Shahidi99]. For a "fully-depleted" SOI MOS transistor, the channel depth is equal to the thickness of the Si-SOI layer. A special case of the fully-depleted SOI MOS transistor is the "thin-body" transistor, where the channel region is thinned to less than 10 nm.

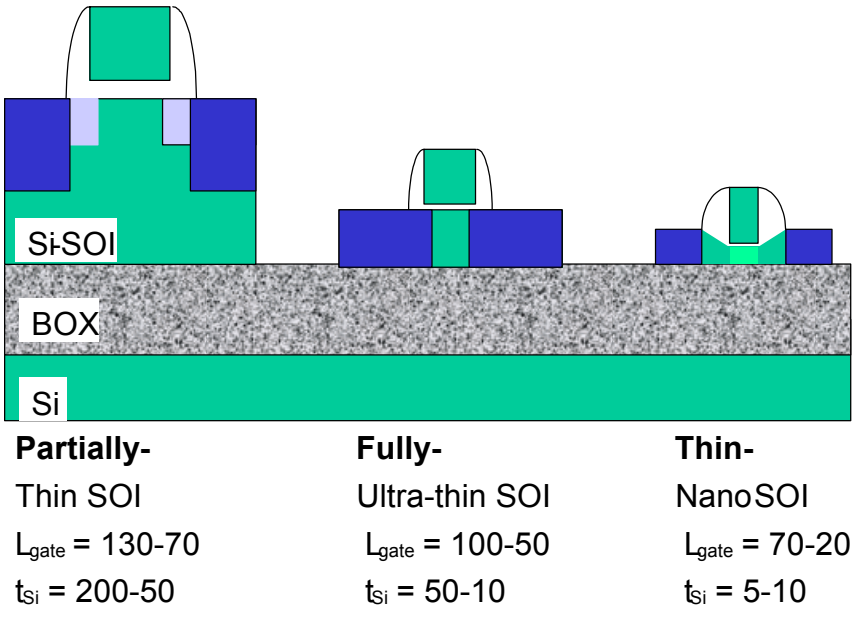


Figure 1-4. Schematics of partially-, fully-depleted and "thin-body" SOI MOS transistors.

SOI devices also provide a pathway beyond the multitude of difficulties that are anticipated for scaling of 45 nm CMOS node and beyond. Many of the process integration challenges for CMOS transistors in bulk-Silicon are either relaxed or removed when SOI wafers are used. A good example is the control of shallow source/drain junction depths. In bulk-Si, obtaining shallow junctions requires careful control of thermal budgets, with the use of rapid thermal annealing "spikes" or laser annealing, to limit both vertical and lateral dopant diffusion while obtaining high dopant activation and adequate defect annealing. With fully-depleted, thin-SOI, where the source/drain junction depth is determined by the SOI layer thickness, the process challenges shift to controlling lateral diffusion and obtaining abrupt lateral junction interfaces. The other key challenge for bulk-Si integration includes the "canyon effect" which is significantly relaxed in SOI. As opening for implants become smaller and smaller with scaling, shadowing during implant reduces the depth of doping as well as the doping volume to the extent that it no longer scales for bulk-Si devices and resuls in higher source/drain and extension resistance.

There is an increasing demand for SOI with ultra thin Si (<30 nm) on 300 mm SOI wafers to improve CMOS performance. Extensive strain engineering is being applied to MOSFET channels to boost CMOS performance on bulk-Si, partially depleted or fully depleted SOI in conjunction with scaling and advanced lithographic techniques (high numerical aperture (NA) immersion lithography). CMOS channels in 90 and 65 nm technology nodes have been strained uniaxially by selectively embedding pseudomorphic SiGe (compressive) and Si-C (tensile) layers in the source drain regions of pFETs, and an nFETs, respectively [Fritze00, Ghani03,Ang04]. The magnitude of the channel strain has been boosted further by depositing tensile and compressive stress liners on nFETs and pFETs, respectively. Scaling of future CMOS (32 nm and beyond) is expected to combine strain enhancement processes with high-k dieletrics, and metal gates.

Development of globally or bi-axially strain in Si is still justified even though locally strain techniques are quite efficient and manufacturable presently. There are two reasons for the development: (i) strains are additive, i.e., local strain will add to the globally strained channel, (ii) the magnitude of local strain is expected to decline in deeply scaled CMOS because there will be less and less volume available for embedding SiGe and SiC with successive CMOS generations. The strain decline can be compensated by the globally strained channel. Methods for fabricating globally strained Si (tensile) based on the SIMOX process will be described in Section 2.1.5. sSOI can be formed in two ways: (i) by creating a strain-Si directly on insulator, and (ii) by creating a relaxed SiGe template on insulator (SGOI) upon which strain-Si is grown.

Application of ultra-thin, 300 mm SOI, SGOI or sSOI for future CMOS technology nodes is being studied carefullly. Thin-body CMOS has been modeled and investigated with 20-25 nm gates [Choi99, Ernst99] [Fig. 1-5]. In terms of the scaling trends, a channel and extension thickness of ≈5 nm would be consistent with a gate size of ≅10 nm, which is 5 times smaller than the perceived "end of the roadmap" for CMOS transistors built on bulk-Si wafers.

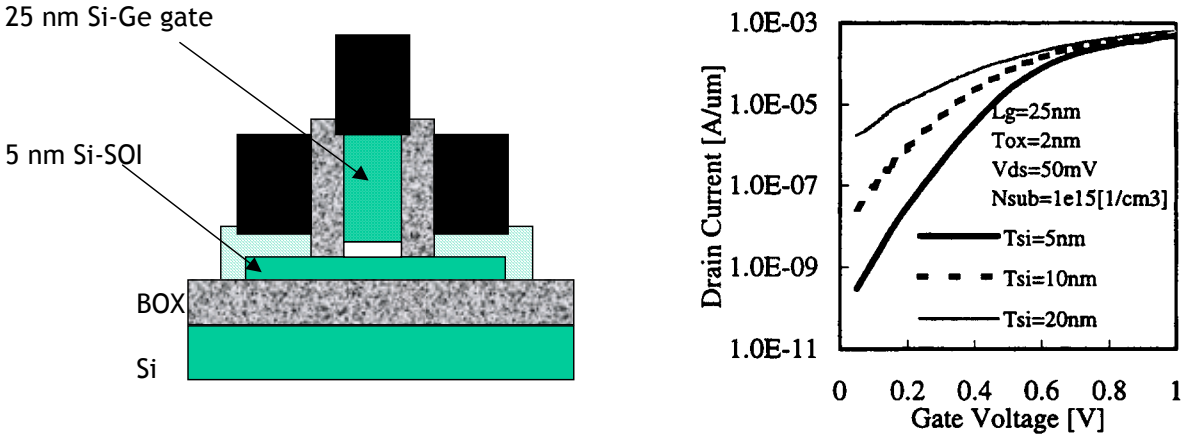


Figure 1-5. Schematic of a thin-body SOI MOS transistor and modeled current characteristics [Choi99].

Future application space for layer transfer techniques beyond SOI consists of both substrate engineering, such as, GeOI, III-VOI, and system level integration, such as forming three dimensional ICs with three dimensional memory stacks, "laminated electronics" for integrated electrical and photonic signal processing [Fig. 1-6] etc. In Fig 1-6, the basic components are (1) fully-depleted SOI CMOS with provisions for dual gates and high-mobility channel layers, (2) thin (<20 nm) Si layers for growth of high-quality optical layers (GaAs, GaN, InP, etc.) by "compliant substrate [Zang98] techniques and (3) optical couplers and signal routers [Wada00].

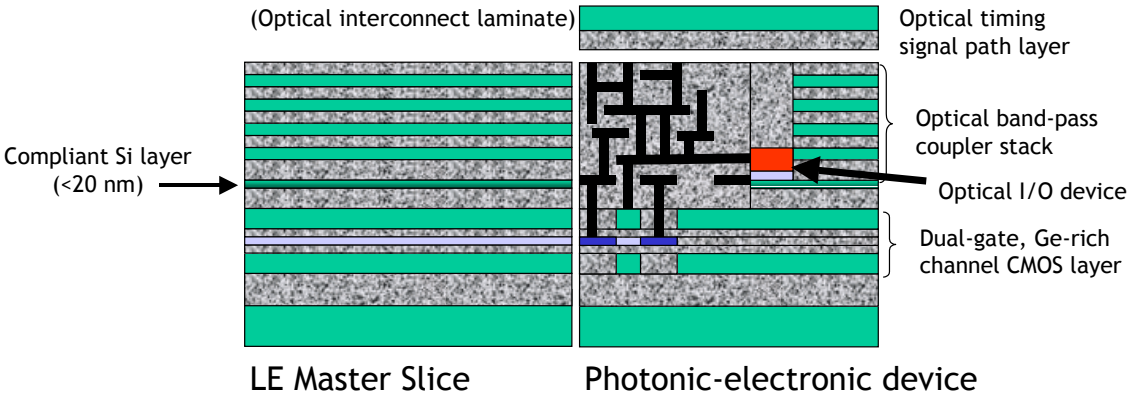


Figure 1-6. Schematic of a "laminated electronics" "Master Slice" wafer and device layers combining fully-depleted SOI CMOS transistors, optical input/output devices and layers for optical signal coupling and routing.

2.1 SIMOX

2.1.1 Products & Scalability

State-of-the-art SIMOX is predominantly made with the Modified Low Dose (MLD) process. Both the SOI and BOX thicknesses can be varied according to the product need. For example, SOI thickness has been varied from 550-1450 A during last three CMOS generations (180, 130, and 90 nm) while the BOX thickness has been kept constant at ~ 1450A (Table 2.1.1). 300 mm MLD SIMOX with excellent thickness and thickness uniformity control has been supplied in commercial quantities to IC manufactures. Current MLD SIMOX meets all highly demanding specifications for 65 and 45 nm CMOS SOI substrates.

There are two key reasons why SIMOX is an attractive process for SOI substrates. First, it is quite manufacturable as it involves only two main process steps, implantation and annealing, both of which have been practiced by the Si IC industry for many years. Second, it is a very scalable process both in terms of implantation dose and beam current. There is a straightforward relationship between the implant dose and cost, i.e., lower the implantation dose, lower the SIMOX cost. Alternatively, higher the beam current for a given dose, lower the cost assuming the equipment cost is not significantly impacted by higher beam current. There are challenges, however. If O^+ dose is lowered so much so that the peak concentration of oxygen falls below (< 1/2) that is required for stoichiometric SiO_2, BOX formation is adversely affected. New implant and/or annealing concepts have to be applied to enhance coalescence of oxide precipitates to form a continuous BOX. The MLD SIMOX process was invented to form a high integrity, continuous BOX at oxygen doses well below that required for stoichiometric SiO_2. Sections below describe SIMOX processes of both the past (standard dose) and present (MLD).

2.1.2 High Temperature Implantation

Since the SIMOX process requires extremely high fluences of oxygen (10^{17}- 10^{18} cm^{-2}), the Si substrate temperature is raised to a few hundred degrees (typically above 500°C) to enhance dynamic annealing of implantation induced damage [Reeson88, Li92]. In earlier generations of commercial oxygen implanters high power generated by high ion beam currents (40-60 mA) was used to achieve wafer temperatures > 500° C. However, this approach greatly limited the range of implant energies and beam currents under which SIMOX process could be practiced. For example, beam energies had to be greater than 150 keV and beam current had to be greater than 40 mA to achieve the required wafer temperature. Consequently, early SIMOX work in the sub 100 keV regime was limited to research laboratories where high implant temperatures could be achieved independently of the beam power by using conventional resistively heated wafer holders. This latter work clearly demonstrated dose regimes where a continuous BOX could be formed at low energies. Modern SIMOX implanters, however, provide independent control of wafer heating via halogen lamps thus enhancing the SIMOX process window down to energies lower than 100 keV.

2.1.3 SIMOX: As-Implanted Microstructure vs Oxygen Dose at > 500 C

The microstructure of as-implanted SIMOX depends on the implant conditions. For example, in the case of standard-dose SIMOX where the dose is 1.8-2.0x10^{18} cm^{-2} at 200 keV, a buried oxide layer has already formed in the implanted region [Fig 2.1-1]. Highly damaged and irregular structure is present on either side of this buried oxide layer. On the other hand, in the case of low-dose SIMOX with a dose of 4x10^{17} cm^{-2} and below at > 150 keV only a buried band of damage clusters intermixed with oxide precipitates in present in the implanted region. The density of SiO_x precipitates submerged in the damage band increases with dose until a semi-continuous but thin oxide region forms at a dose of 5-6x$10^{17}$$cm^{-2}$ (Fig 2.1-2). The thickness and continuity of the oxide region increases with dose. There appears to be a correlation between increased oxide precipitation in the damage band in the as-implanted material and an increase in the density of Si inclusions in the annealed wafers [Bagchi96]. The Si inclusion density begins to decline at doses which are significantly higher than those theoretically needed to achieve stoichiometric SiO_2. Excess implanted oxygen consumes the disordered Si and oxide precipitates or other nucleation sites by internal oxidation [Current96].

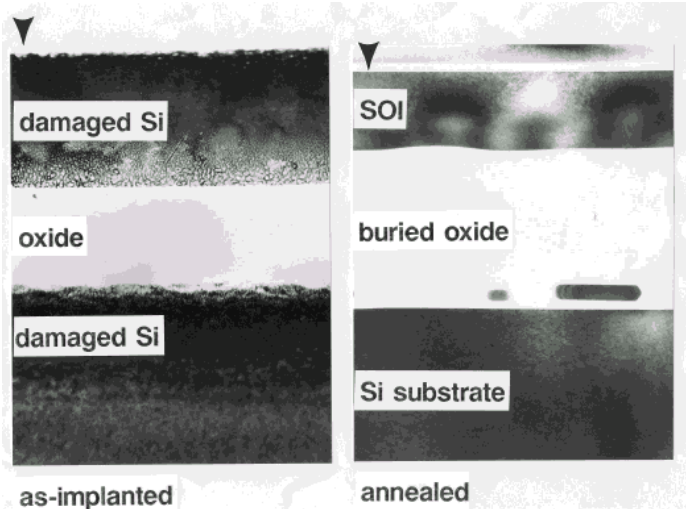


Figure 2.1-1. Cross-section TEM micrographs of standard-dose SIMOX before and after anneal. Note the formation of a buried oxide layer in the as-implanted sample (a). The surface region in (a) is crystalline albeit highly defective.

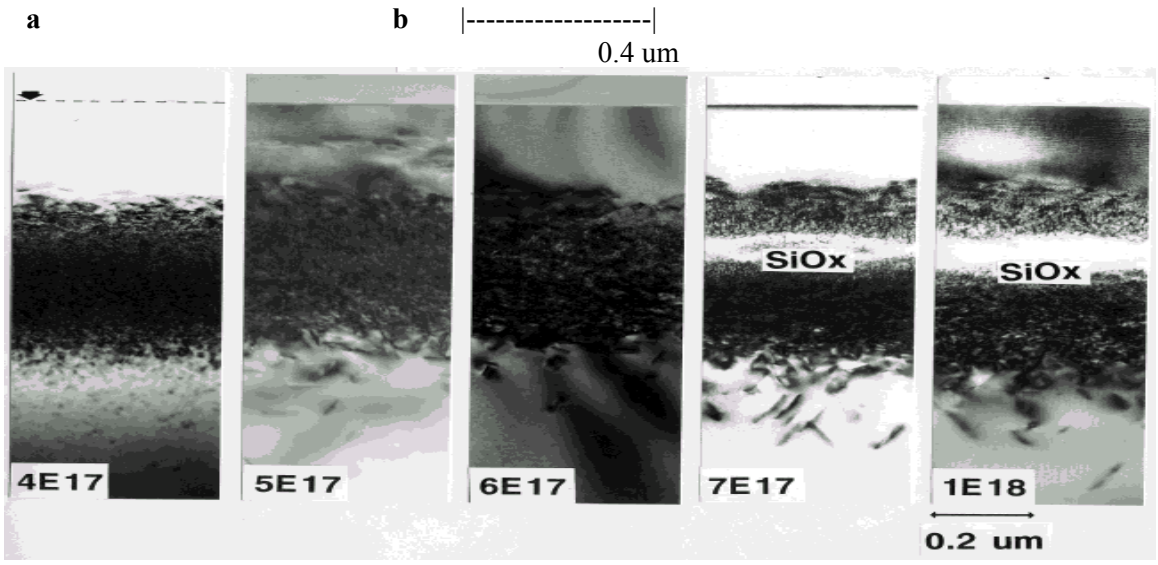


Fig. 2.1-2. Cross-section TEM micrographs showing damage distribution in as-implanted SIMOX as a function of the oxygen dose. Note the formation of an oxide layer at > $6x10^{17}$ cm^{-2}. The surface region in all samples is crystalline due to dynamic annealing during the implant.

2.1.4 SIMOX: Annealed

a. Standard Dose

Annealing kinetics of standard dose SIMOX is vastly different than that of the low-dose SIMOX because of their vastly different oxygen concentrations and damage structures in the implanted region [Figs2.1-1a and 2.1-2a-2.1-2e]. Typical annealing for standard dose SIMOX is carried out at temperatures > 1300^oC for 4-8 hours in Ar or N_2 ambient with low concentrations of O_2 (0.5-2%) [Celler86, Margail92]. Formation of the BOX in standard dose SIMOX involves a complex mechanism which probably occurs in two stages: (i) growth of oxide precipitates above the BOX during the early stages of annealing (e.g., during ramp up), and (ii) dissolution of the precipitates during prolonged anneal at 1300^o C. The oxygen released by the oxide precipitates is absorbed by the upper Si/BOX interface increasing the overall thickness of the BOX. Simultaneously, annihilation of voids and other defects at the surface takes place via interaction with Si interstitial, vacancies and their complexes. The end result is a SOI material with a dislocation density in the range 10^5 - 10^7 cm^{-2} with an SOI thickness of < $2000A^o$, and BOX thickness of ~ $4000A^o$. The density of dislocation depends on the implant dose, temperature, and the resultant stresses in the as-implanted material.

Early development of SIMOX from 1970s to early 1990s was dominated by the standard dose process. The oxygen dose window was defined by the stoichiometry requirements of SiO_2 in Si. Despite its initial success in demonstrating high yielding 22 nm CMOS product (IStar), the process is no longer used for CMOS applications because of low throughput and high cost. The process is quite time consuming and is unattractive for high volume production. A typical modern SIMOX implanter even with a nominal beam current of 100 mA is estimated to produce ~25 wafers of 300 mm diameter per day with around the clock operation. Because of its thicker BOX, standard dose SIMOX has limited application for optical waveguides.

b. Low Dose

A focused effort has been underway since early 90s to develop a high throughput, low-dose SIMOX process for Si IC applications. The BOX thickness cannot be reduced indefinitely because it has be to thick enough to avoid capacitive coupling of devices and circuits formed in the SOI with the underlying Si substrate. Work performed under a DARPA funded Low Power Electronics program at IBM during 1995-99 indicates that a BOX thickness of ~ 1000 A^o is sufficient to avoid capacitive coupling. SOI circuits formed on such a BOX maintain the same performance advantage over the bulk-Si technology as that achieved with a 4000 A^o BOX. This BOX thickness reduction corresponds to a decrease of x4 or more in the oxygen dose compared to that used to form the standard dose SIMOX.

Low dose SIMOX effort in the last decade has been focused in the dose regime of $2x10^{17}$ $4x10^{17}$ at energies of > 150 keV to create a product that meets the partially-depleted device design for high volume CMOS products. Furthermore, from the material development point of view, the use of thicker SOI can be extended to fully depleted SOI by simply thinning the SOI layer by thermal oxidation. It is also possible to develop a reverse process whereby fully depleted SOI is converted into partially depleted SOI by growing an epitaxial-Si layer on thin SOI. However, such an option is undesirable for two reasons (a) additional tooling and process cost, and (b) reduced thickness control of the SOI layer as the epi-Si layer may introduce additional thickness non-uniformity of 1-2% over and above that in SOI.

When the standard dose annealing is applied to low-dose SIMOX, a discontinuous BOX is typically created. The oxygen implanted region often consists of two discrcete layers of broken oxide precipitates corresponding to the peak regions of the damage and implanted oxygen. Formation of a continuous and high quality BOX in low-dose SIMOX was accomplished in the early 1990s by modifying annealing cycles and varying oxygen concentration in the anneal ambient. It was also discovered that internal thermal oxidation (ITOX) occurred during annealing of SIMOX. The extent of ITOX depended on the oxygen concentration in the anneal ambient and anneal temperature (see details below).

I. Non-ITOX: This process is an extension of that used for standard dose SIMOX. Wafers are typically implanted in the dose range $4\text{-}10x10^{17}cm^{-2}$ either in single or multiple steps followed by annealing at > 1300^oC in single or multiple steps in inert atmosphere mixed with low concentration (<5%) of oxygen. The thickness of the BOX corresponds closely to that expected from the implanted dose. For example, a dose of $4x10^{17}cm^{-2}$ corresponds to a BOX thickness of ~ $1000A^o$ [Fig 2.1-3] [Kilner93].

a b

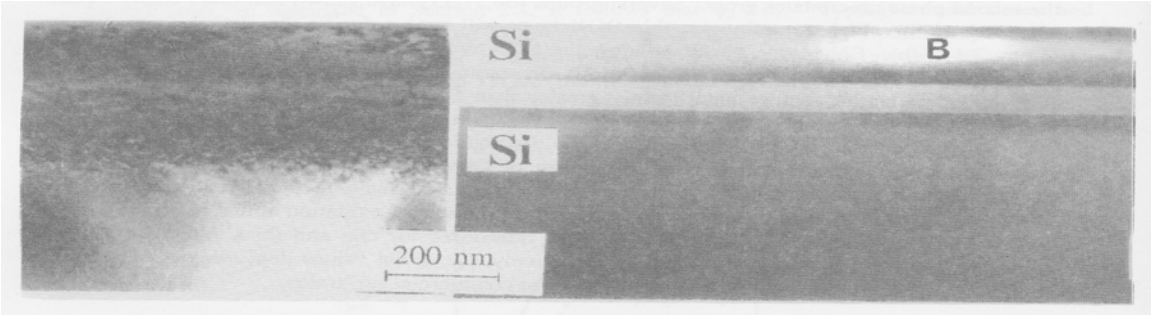


Fig. 2.1-3. Cross-sectional TEM micrographs of 70 keV SIMOX before and after high temperature annealing. Dose: 3.3e17 cm^{-2}, Imp Temp: 680^oC. Note the BOX thickness of approximately $700A^o$ (Fig. 2.1-3b) corresponds closely in value to what is expected from implant dose.[Kilner9].

II. **ITOX:** This annealing process was found to be very effective in improving the BOX quality when the implanted oxygen dose was around $4x10^{17}cm^{-2}$ (so called Izumi window). The annealing was conducted at > 1300C in an ambient that consists of inert gas (typically Ar) mixed with high concentrations of oxygen, typically in the range 30-60% [Nakashima93,94]. Under such annealing conditions, not only does oxygen reacts with the Si surface to form the surface oxide but it also diffuses into the Si in significant amounts. The upper-Si/BOX interface acts as a sink for the diffusing oxygen and additional thermal oxide-like BOX is formed on top of the implanted BOX. Figure 2.1-4 shows the relationship between the ITOX induced oxide growth and the thermal oxide growth on the surface during annealing at 1350°C. The electrical quality of this BOX (as determined by its breakdown field) is superior to that of the BOX formed without the ITOX [Fig 2.1-7]. The BOX thickness can be increased in a predictable manner for a given anneal temperature and oxygen concentration. The BOX thickness therefore has two components, the implanted dose component which forms the lower part of the BOX, and the thermal oxide component which forms the upper part of the BOX.. Figure 2.1-5 shows the relationship between the ITOX induced oxide and the reciprocal of annealing temperature [Nakashima93,94]. Typically, ITOX induced BOX thickness is 8-10% of the surface oxide. Under practical implant conditions, however, ITOX induced BOX thickness is limited to < 800A° for previous generation of implanters which run at a maximum beam energy of 210 keV. The maximum Si thickness that is available to form the surface oxide for a 210 keV O+ implant is limited to ~ 3500A° which limits the maximum surface oxide growth to < 7500A°, and hence the maximum ITOX thickness to < 800A. Fig 2.1-4 shows ITOX data from 180 keV oxygen implants where the maximum Si thickness available is ~ 2500A, and the maximum ITOX is < 600A.XTEM micrographs of Figure 2.1-6 compare the BOX in non-ITOX and ITOX wafers, and confirm the oxide growth data in

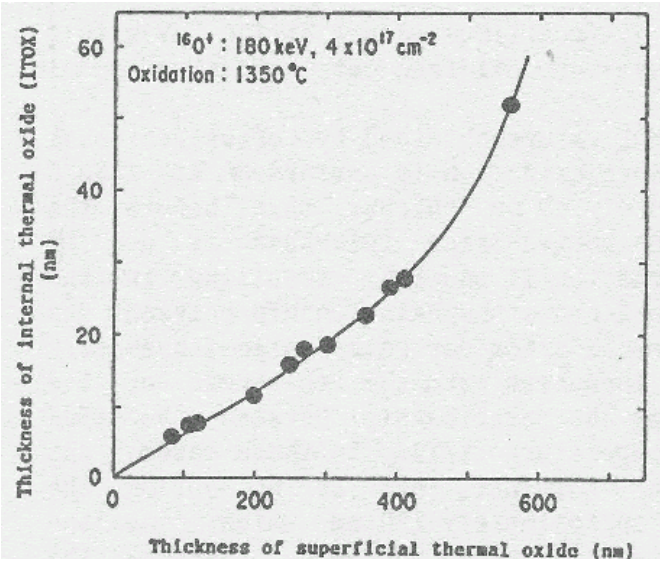


Fig. 2.1-4. Internal thermal oxidation induced buried oxide thickness vs the oxide grown on the surface of the SIMOX during annealing at 1350°C. (Nakashima94).

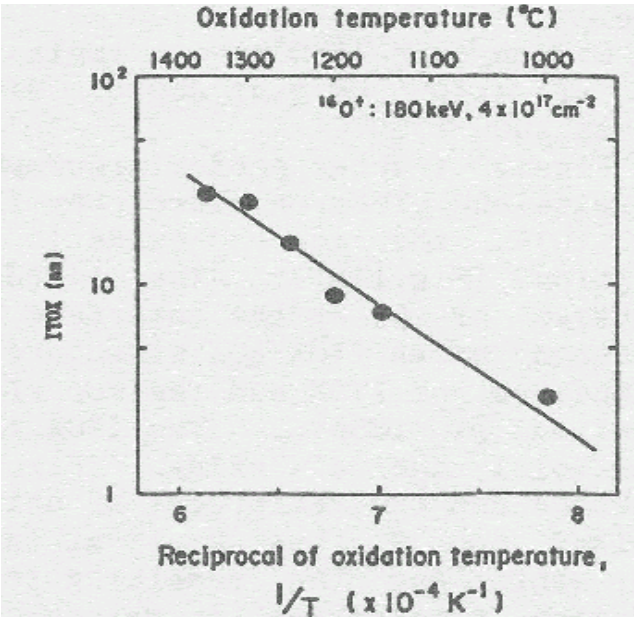
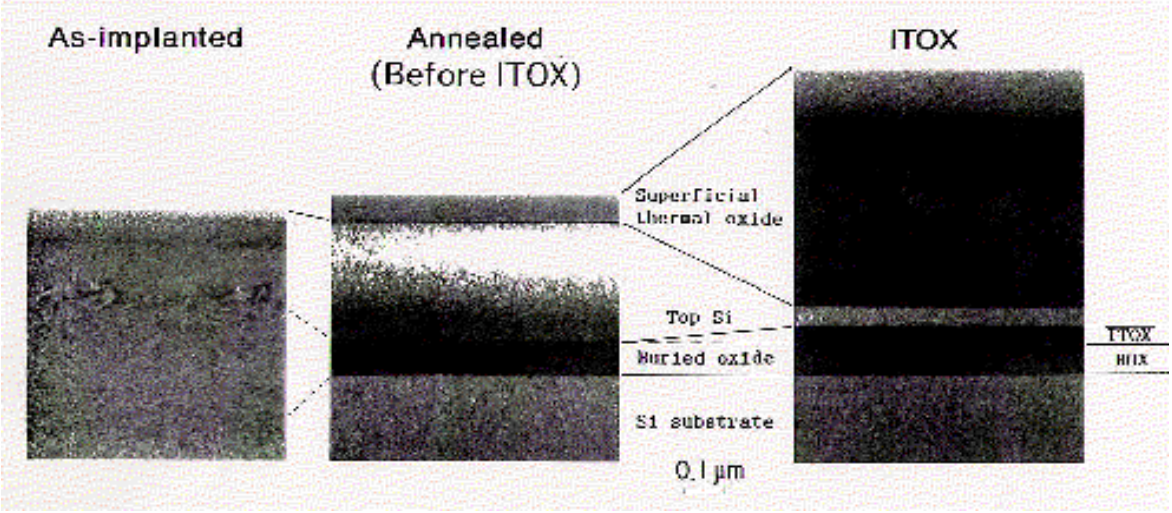


Fig. 2.1-5. Internal thermal oxidation induced oxide thickness vs reciprocal of annealing temperature (1/T). The surface oxide thickness was ~ 400nm and was kept constant for all temperature. [Nakashima1994]

Figs 2.1-4 and 2.1-5. Since top region of the BOX in ITOX wafers is thermal oxide, the BOX properties, such as breakdown voltage and short density show marked improvement as shown in Figure 2.1-.7 [Nakashima00].



a **b** **c**

Fig. 2.1-6. Cross-sectional TEM micrographs showing the BOX formation: (a) with, and (b) without ITOX. (b. Implant conditions: 180 keV, $4x10^{17}$ cm^{-2}. Anneal Temp: 1350°C [Nakashima94, Nakashima, 00]

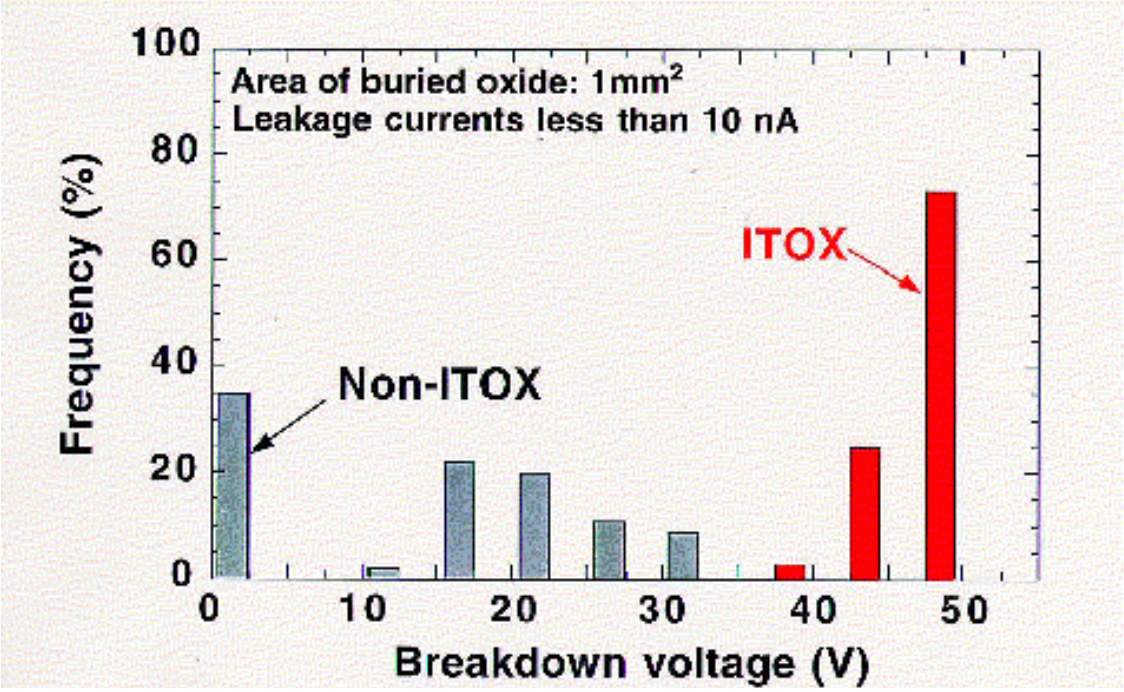


Fig. 2.1-7. Improvement in the electrical quality of the BOX by ITOX. Both the breakdown field and short density improve by ITOX [Nakashima00]

III Modified Low Dose (MLD) SIMOX : The MLD SIMOX process has two main attributes: (i) enhanced ITOX (> x 2 compared to the original ITOX process) which allows the BOX electrical quality to be at par with that of a thermal oxide, and (ii) a continuous range of BOX thicknesses that can be achieved by simply varying the base dose of oxygen. Furthermore, the minimum dose at which a continuous BOX can be formed is reduced to < $2x10^{17}$ cm^{-2} well below that was achieved previously by Izumi. MLD SIMOX can therefore provide a SOI product with a BOX in the thickness range of 500 – 2500A. The thickness of the Si can be tailored to any value down to 50A by adjusting SIMOX anneal parameters.

The MLD process utilizes the following three major steps: (i) implantation of the main $^{16}O^{+}$ dose (> $1.5x10^{17}$ cm^{-2}) into a hot (> 200C) Si substrate at an energy of > 100 keV, (ii) cooling down the substrate to nominal room temperature and amorphizing the upper part of the implanted region created after step (i) by another O^{+} implant at a dose of < $1x10^{16}$ cm^{-2} (touch up implant) [Holland96], and (iii) subsequently annealing the composite structure at > 1300C under conditions which enhance internal thermal oxidation at the implanted region [Sadana97]. Like its predecessor low-dose SIMOX process described in Section II above, thermal oxide grows at the upper BOX interface in MLD SIMOX due to ITOX. However, the stable damage created by the touch up RT implant not only enhances ITOX by almost *x* 2 or more compared to process II (Fig 2.1.8) but also reduces the O^{+} dose requirements (< $2.0x10^{17}$ cm^{-2}) for a continuous BOX.

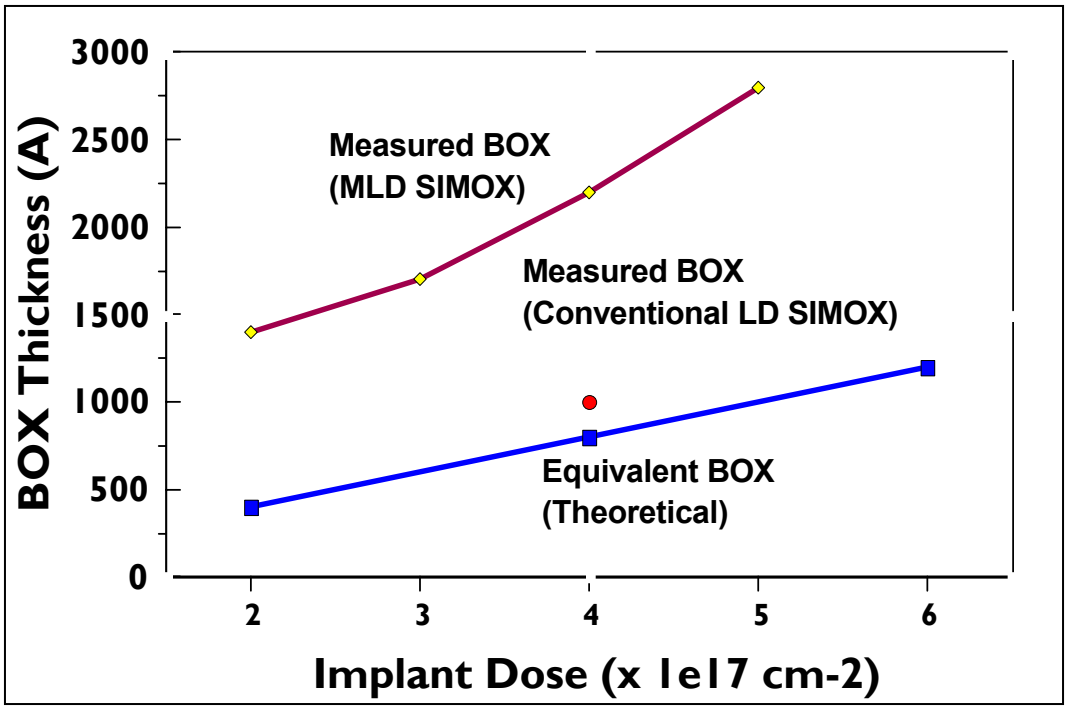


Fig 2.1-8. Modified low dose showing (i) enhanced ITOX (see calculated vs experimental curves), (ii) formation of a continuous BOX at doses (all the way down to ~ 2E17 cm-2) well below Izumi dose window, and (iii) a continuum of doses where a continuous BOX can be formed.

In the latest 300 mm commercial MLD SIMOX product the BOX consists of > 70% of thermal oxide created by ITOX. Typical intrinsic breakdown field of full BOX in such SIMOX (with 550A or 700A SOI) is ~ 8 MV/cm which is the same value as that obtained for a thermal oxide. The BOX short density is well below < 0.1 cm^{-2}. Figure 2.1-9 shows an XTEM micrograph of the 550A MLD SIMOX being used for IBM's 90 nm CMOS products.

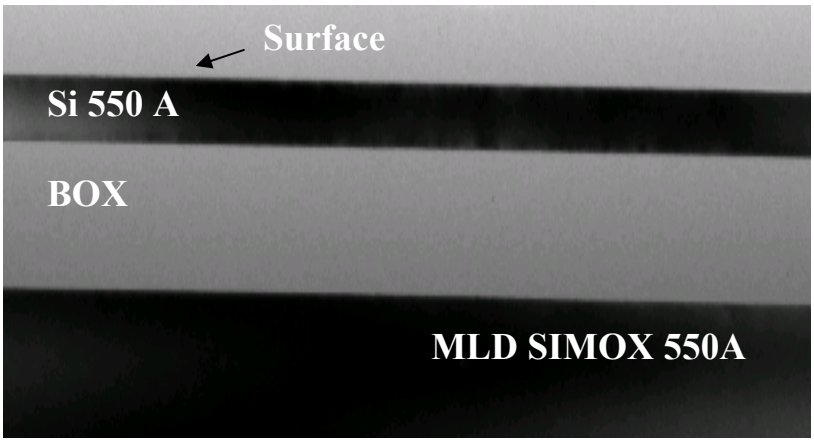


Fig 2.1-9. A XTEM micrograph showing state-of-the-art MLD 550 A SIMOX (Based on patent by Sadana97).

Figure 2.1-10 highlights the scalability of the SIMOX process as SOI applications move towards 90 nm beyond CMOS technology generations. The intrinsic electrical quality of the BOX improves dramatically as the base dose of O^+ decreases. This phenomenon occurs because the ITOX fraction of the BOX increases with respect to the implanted fraction of the BOX as the O^+ dose. From manufacturing point of view, one produces better SIMOX at a lower cost!

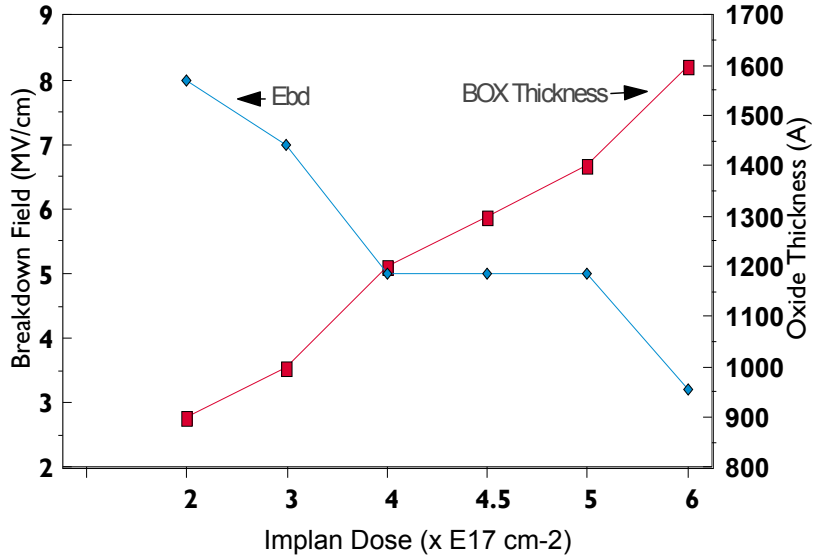


Figure 2.1-10. BOX thickness and corresponding BOX breakdown field (Ebd) in SIMOX vs the implanted oxygen dose. Note that at a dose of $2x10^{17}$ cm^{-2} the E_{bd} is ~ 8MV/cm whereas at a dose of $4x10^{17}$ cm^{-2} E_{bd} drops down to 5MV/cm.

Standardization of SIMOX via MLD SIMOX

There has been a deliberate move in the last few years to standardize SIMOX process for high volume IC production. Since SIMOX can be produced in a variety of ways, it has always been difficult in the past to decide which choice of SIMOX is most suited for IC applications. In addition, there was no compelling reason to try out product based test vehicles, such as microprocessors, high density SRAMs etc that could be used to determine which particular vintage of SIMOX was most qualified for high volume IC requirements. However, since 1997 when IBM announced its CMOS SOI technology, it has been shown that microprocessors built on MLD SIMOX yield equivalent to those built on bulk-Si. Now, more than 5 generations of CMOS SOI technology has been qualified on MLD SIMOX, and this material is obviously the leading choice for SIMOX for the semiconductor industry.

New Applcations: sSOI by SIMOX

2.1.5 Silicon Germanium on Insulator (SGOI) by SIMOX

The SIMOX method has recently been extended to form SGOI for strain-Si on insulator (SSOI) applications. Strain-Si is desirable to improve electron mobility, and hence improve performance of CMOS. There are two methods to create SGOI via the SIMOX process. In the first method, O^+ is implanted into a SiGe layer grown on a Si substrate followed by a high temperature SIMOX-like anneal. The SiGe layer could be either psedomorphic or relaxed (e.g., a SiGe graded buffer layer). In the second method, a pseudomorphic SiGe layer is grown on a Si substrate that has already undergone SIMOX-like oxygen implant but has not been annealed. The composite structure subsequently undergoes MLD SIMOX-like anneal. Figure 2.1.12 depicts the concept of the latter SGOI process. It is interesting to note that highly relaxed SGOI (> 80%) is created. Target Ge composition in these layers is typically 15-20%. High quality

strain-Si layer have successfully been grown on the SGOI layer and the process has been implemented on 300 mm diameter Si wafers.

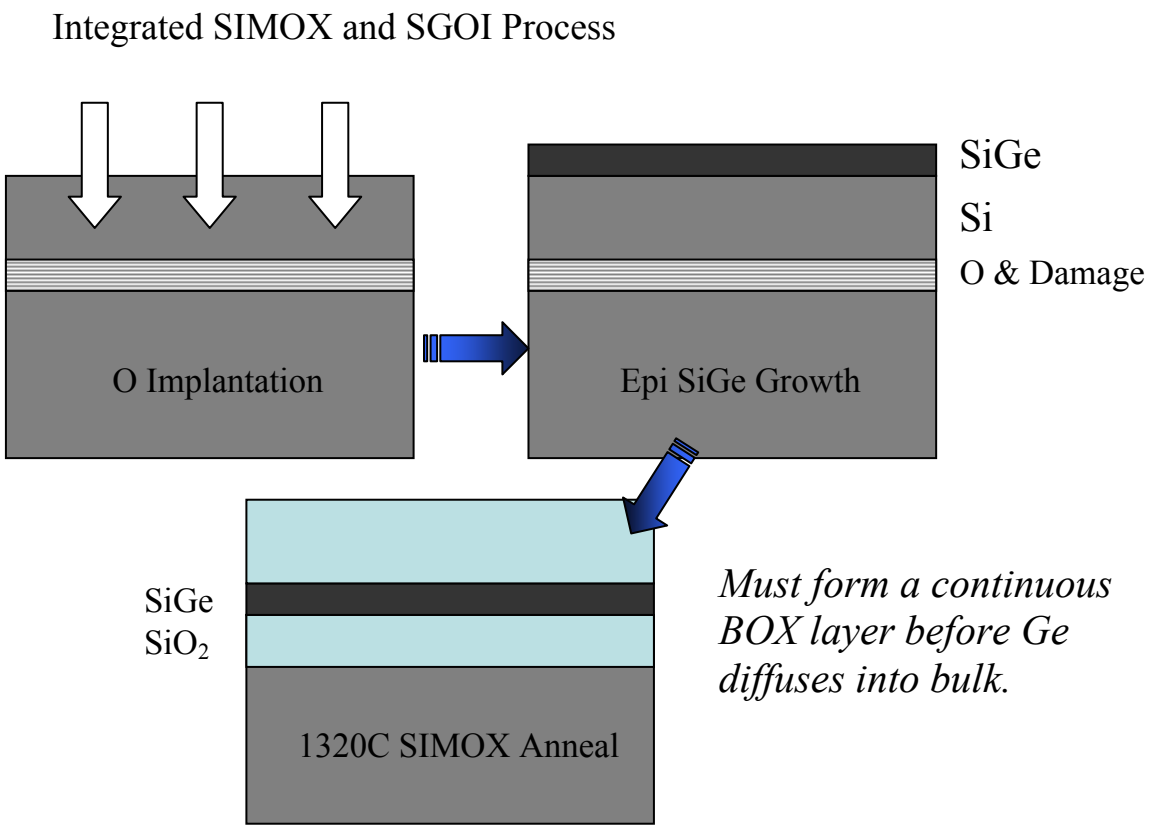


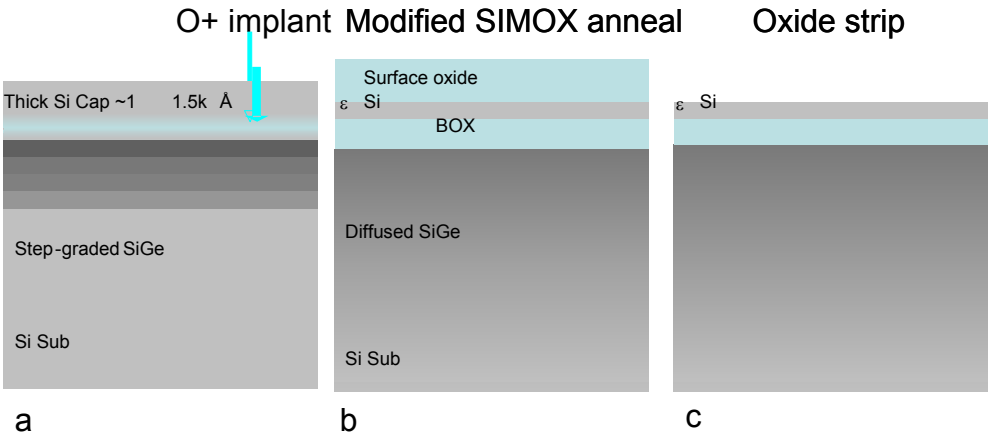
Figure 2.1.12 SSOI by integrated SIMOX-SGOI process.

2.1.6 sSOI by SIMOX

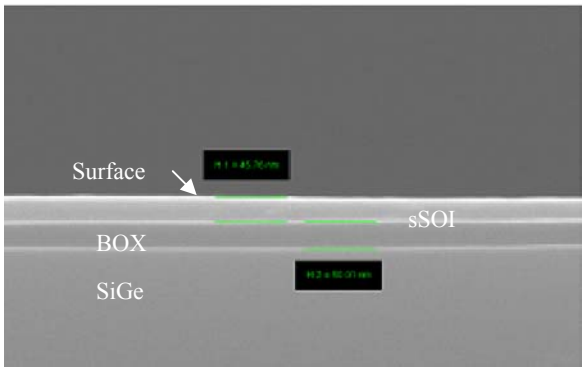
Conventionally, sSOI is fabricated by wafer bonding and layer transfer of strain Si [Langdo02]. Although this technique has successfully been used to produce sSOI substrates, its fabrication cost is a concern for commercial applications. Some of key process/substrate elements in fabricating such sSOI include (i) a device wafer that contains epitaxially grown thick graded buffer layers (GBL) of SiGe with strain-Si on top, (ii) deposition of an oxide layer on (i), (iii) bonding of the device wafer with a handle wafer (bulk-Si), and (iv) layer transfer of strain-Si/oxide stack onto the handle wafer. Substantial cost saving is expected to occur if sSOI is fabricated by SIMOX because this process uses only a single wafer (described as the device wafer above).

Figures 2.1.13 shows a schematic process flow to fabricate sSOI by the SIMOX method [de Souza06]. SiGe graded buffer layers were grown on a p-type (100) bulk-Si substrate (a) with a compositional grading starting with 5% Ge and ending up with a top layer containing nominally ~ 15% Ge, ~ 98% relaxed. Strain-Si of thicknesses 500 – 1000A was grown on top of the relaxed GBL. These thicknesses values correspond to x2 – x 4 the critical thickness of Si for a fully relaxed SiGe with 15% Ge. It has been shown previously that even though high density of stacking faults form in thick strained Si, its relaxation is minimal [Bedell04, 05]. Thick strained-Si layers allow a bigger process window for sSOI by SIMOX. Oxygen implant and subsequent anneal conditions were optimized such that strain-Si thickness of > 100A resulted in the sSOI

substrate. Typical O^+ implant was conducted at 40 keV at ~ 500°C in the dose range of 1.5-2.5 x 10^{17} cm^{-2}. Subsequent annealing was conducted in the temperature range of 1250 - 1320° C in Ar/O_2 ambient with ramp rates, soaks and soak times as described previously (5). Figures 2.1.13 b and c illustrate schematically inter diffusion in the SiGe GBL underneath the sSOI during high temperature SIMOX anneal. Figure 2.1.14 shows sSOI layer in cross-section by SEM. Strain of 0.3% in the sSOI was confirmed by XRD and Raman spectroscopy (Fig 2,1,15)[Tsang94].



Figures 2.1.13. Process flow for sSOI by SIMOX.



Figures 2.1.14. Cross-sectional SEM showing sSOI by SIMOX

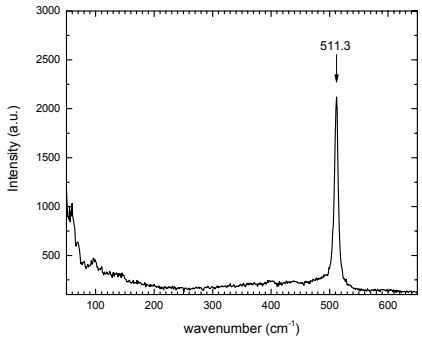


Figure 2.1.15. Confirming strain in sSOI by Raman spectroscopy

2.1.7 Characterization of SOI Materials

Not only has the task of fabrication of SOI material challenging but equally challenging has been its screening for product worthiness. Many of the optical and electrical characterization techniques developed earlier for bulk-Si cannot be directly applied to SOI materials because of the presence of the BOX. Furthermore, characteristics of the defects that limit device and circuit yield in SOI are still not fully understood. Despite these limitations, remarkable progress has been made in evaluating SOI to a point where one can sort the good material from the bad material for product with has high confidence. Some of the main parameters for evaluation include: (i) SOI thickness and thickness uniformity, (ii) BOX thickness and uniformity, (iii) HF-defect density, (iv) dislocation density, (v) surface roughness, (vi) surface pitting, (vii) concentration of metallic contaminants, (viii) carrier mobilities in the SOI region, (ix) fixed charge in the BOX, and at the Si/BOX interface, (x) BOX short density at full BOX thickness and at reduced BOX thickness. Table 2.1.1 summarizes typical physical and electrical parameters in commercial MLD SIMOX.

Physical Characterization

This section will focus on characterization of parameters (i)-(vii) listed above. SOI thickness and thickness uniformity are two key parameters that can impact the device and/or circuit operation and reliability. These become even more critical for circuits based on fully depleted device design. Thickness and thickness uniformity are generally measured by spectroscopic ellipsometry, or by other multi-wavelength spectroscopic tools. Thickness uniformity of <1% is routinely achieved for SIMOX. Highly sophisticated thickness mapping tools with fast turnaround time have been developed, such as ADE's Acumap 2. In this tool, over 30,000 measurements are made in about 1 min, and the data is converted into printable thickness maps within 2 minutes.

One of the most simple and important techniques for SOI evaluation is HF etching. The starting SIMOX or any other kind of SOI material is dipped in concentrated HF (49%) for several minutes (typically 20-30 min) to highlight any weaknesses in the SOI layer. If there is any path for HF to diffuse through the SOI layer into the underlying BOX, a HF-defect is created [Sadana94,96]. A HF-defect is disc-shaped and its size depends on the length of the HF exposure, and type of the defect. The major cause of HF-defects in SIMOX is particles that are generated in the implanter. The particles can be metallic or non-metallic. Generally speaking, a particle on the Si surface during O^+ implant shifts the peak of the implanted oxygen profile towards the Si surface such that the resulting BOX may intersect the surface and form an HF defect. In the case of a metallic particle, an HF-defect site may be created where the particle reacts with the underlying Si to form a silicide and/or a silicate (hot implant) region. HF is known to react with slicides. Depending on the origin of an HF defect, there may be a finite incubation period (extending from a few seconds to a few minutes) before the defect becomes visible under an optical microscope. A prolonged HF exposure (> 20 min) is therefore recommended to highlight tenacious defects with a long incubation time. HF-defect density in commercial MLD SIMOX has been reduced to a below detection level (< 0.1 cm^{-2}).

Another important parameter to control is surface roughness and pitting which can routinely be monitored by atomic force microscopy (AFM). Typical RMS values of surface roughness for latest MLD SIMOX and bonded SOI are 2-4 A^o, and 1-3 A^o, respectively on a 10 um x 10 um area. Higher roughness (R_{ms} of 2-3A^o) in bonded SOI occurs when non-CMP processes are used to thin SOI. It is generally found that if AFM is performed on the BOX after removing the top SOI layer, the roughness depends on the annealing procedure used. Improving roughness of the SOI surface as well as BOX/SOI interface is critical for thin SOI material.

Table 2.1.1: Physical and electrical properties of modern commercial MLD SIMOX

Parameter	Units	MLD SIMOX
Silicon Thickness	A^o	200 - 1600
Si Thickness Unif (1 Sigma)	A^o	7 – 10A^o
BOX Thickness	A^o	1200 - 1500
HF-Defects Density	cm^{-2}	< 0.1
Dislocation Density	cm^{-2}	< 10^2
Stacking Fault Tetrahedara	cm^{-2}	Below detection
Surface Roughness (10um x 10um)	A^o	2-4
Metallics (TXRF)	cm^{-2}	< 10^{11}
BOX Short Density	cm^{-2}	< 0.1
Electron Mobility	cm^2/V-s	650 - 850
Hole Mobility	cm^2/V-s	200 - 300
Oxide Charge	C/cm^{-2}	1.5 - 3 x 10^{11}
Interface State Density	$cm^{-2}eV^{-1}$	1 - 3 x 10^{11}
Transconductance (Gmsat)	mS	900 - 1200

Electrical Characterization

The presence of the BOX in SOI material makes it possible to form a pseudo-MOSFET by using BOX and substrate as the gate oxide and gate electrode, respectively, and two contacts on the SOI layer as source and drain. Earlier pseudo-MOSFET work utilized two point contacts on the SOI region for source and drain connections [Liu90, Cristoloveanu95]. However, the point contacts act as Schottky barriers and the transfer characteristics of the pseudo-FET are pressure sensitive. More recently, HgFET technique has been developed in which a combination of broad area Hg electrodes coupled with special surface treatment with HF:H_2O are used to overcome the limitations of point contacts [Hovel97]. Measurements in the linear region show that the Hg electrodes are Ohmic to electrons and Schottky-like to holes immediately after the surface treatment, but become Ohmic to holes and Schottky-like to electrons after a certain period of time. Therefore, both NFET and PFET transfer characteristics can be obtained by the HgFET technique which was not possible by the point contact pseudo-FET technique . It is interesting to note that contrary to common belief, low-field electron and hole mobilities of MLD SIMOX are quite close in values to those of the starting Si substrate (Table 2.1.1). Fixed charges at the upper Si/BOX interface, and in the BOX are typically quite low. The BOX integrity as measured by its breakdown field and number of shorts (or low breakdown field sites) is extremely good for both bonded SOI as well as MLD SIMOX (< 0.1 cm^{-2}).

BOX shorts in MLD SIMOX are primarily created by the particles which deposit on the surface during implantation and block O^+ beam from entering the surface. The BOX under is either discontinuous or absent depending on the size of the particle. Large Si inclusions can form within the BOX when implant dose exceeds 4x10^{17} cm^{-2} at energies of 170-200 keV. Such BOX can be leaky. Latest vintage of MLD SIMOX has addressed both the particle and BOX leakage issues effectively as indicated by the data in Table 2.1.1.

2.1.8 SIMOX: Present and Future Developments

The material quality of SIMOX has improved markedly in the last two decades. This progress has accelerated markedly to meet ever tightening specifications of the starting SOI substrate. 300 mm MLD SIMOX wafers with highly uniform SOI films (range < +/- 35 A^o) are being routinely produced for SOI based CMOS products. In parallel, there have been some

noteworthy improvements in SIMOX equipment as well in the last few years: (i) increasing wafer diameter from 200 to 300 mm for implantation, (ii) increase in O^+ beam current from 50 to 100 mA (iii) O^+ beam energy increase from 210 to to 240 keV, and (iv) and pronounced reduction in particle levels from 1500 to < 100 (0.2 um). Majority of particles have been shown to be generated at pins which hold wafers. Other sources of particle include beam line components that may shower particles when exposed to the beam either due to slight misalignment in its trajectory, or due to high space charge that causes beam blow-up. The cost of ownership for SIMOX process is being reduced on a continuous basis. There are several components of cost reduction that are being addressed: (i) upgrading equipment to increase the O^+ beam current to several hundreds of mA, (ii) further reducing the oxygen dose to form SOI, and (iii) more importantly, reducing wafer handling time during implantation. The handling time accounts for nearly 20-30% of the total implant time presently. Annealing issues that need attention for 300 mm SIMOX include (i) slip at the edges of a 300 mm SIMOX wafer, and (ii) increased flat temperature zone to increase wafer batch size (from 50 to 75 wafers). The latter will help reduce cost of ownership of SIMOX. In the long term, the implanter needs to be further modified to (i) increase flexibility of choosing ion species other than O^+ only, such as, O_2^+, N^+, N_2^+ etc. (ii) to increase implant temperature capability to higher than 600C, and (iii) to widen the implant energy window both in the low and high energy regimes, e.g., 10 - 300 keV, rather than the present energy regime of 40-240 keV**.** These improvements are necessary to allow wider range of SOI applications by the SIMOX process.

Advanced Products on SOI

SOI based products are already pervasive in PC and server markets. Many major IC manufacturers are in active pursuit of developing future generation SOI products. The most advanced product on SOI presently is a multi-core 64 bit cell processor developed by IBM for various applications including Sony's future play station product (Fig 2.1-16). The cell processor is designed to create a flexible architecture for computing.

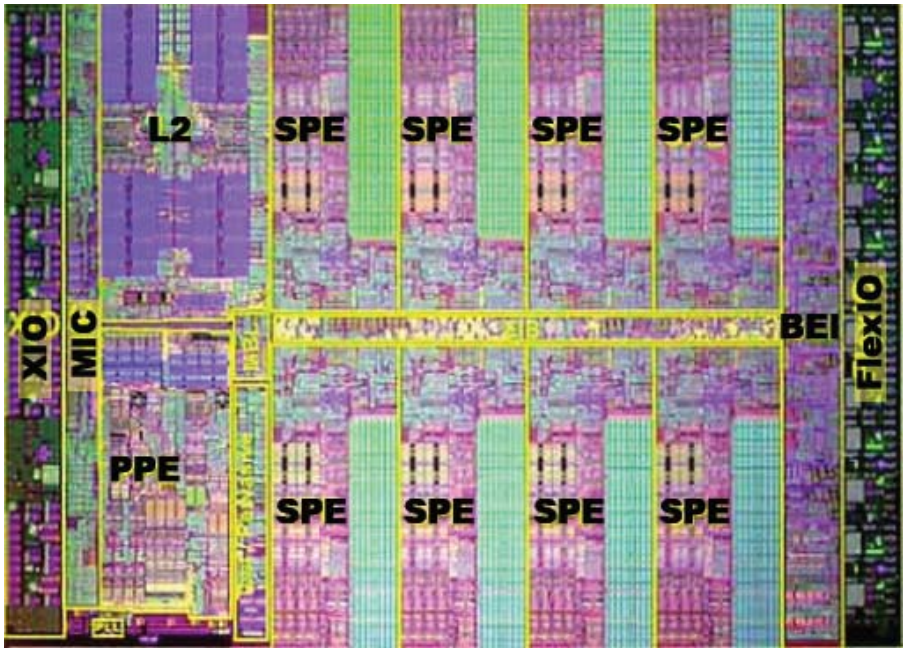


Fig.2.1-16. A schematic layout of a Cell processor for Sony's future play station.

Layer Transfer or "Bonded" SOI and sSOI Wafers

Another approach to form SOI wafers is to bond device-grade Silicon wafer containing a "splitting region" to another "handle" wafer. Then the bonded pair is separated by some process to leave the SOI layer attached to the handle wafer. "Layer transfer" concepts allows for considerable freedom in generating the "splitting region" and the bond interface and can be scaled to high production volumes. This has led to the development of at least three production methods for fabrication of SOI wafers, Smart-Cut™, NanoCleave™ and ELTRAN™. The splitting process can be extended to create strain-Si on insulator (sSOI) wafers by transferring a strain-Si layer grown over a relaxed SiGe graded buffer layer onto a handle wafer with an oxide layer.

2.2 SMART-Cut™ Process

The Smart-Cut process uses high-dose of hydrogen implants ($5x10^{16}$ to $1x10^{17}$ H/cm^2) to generate a splitting region in the bonded Si through formation of a network of hydrogen bubbles during a thermal anneal cycle [Bruel96]. The basic process flow for Smart-Cut is shown in Fig. 2.2-1.

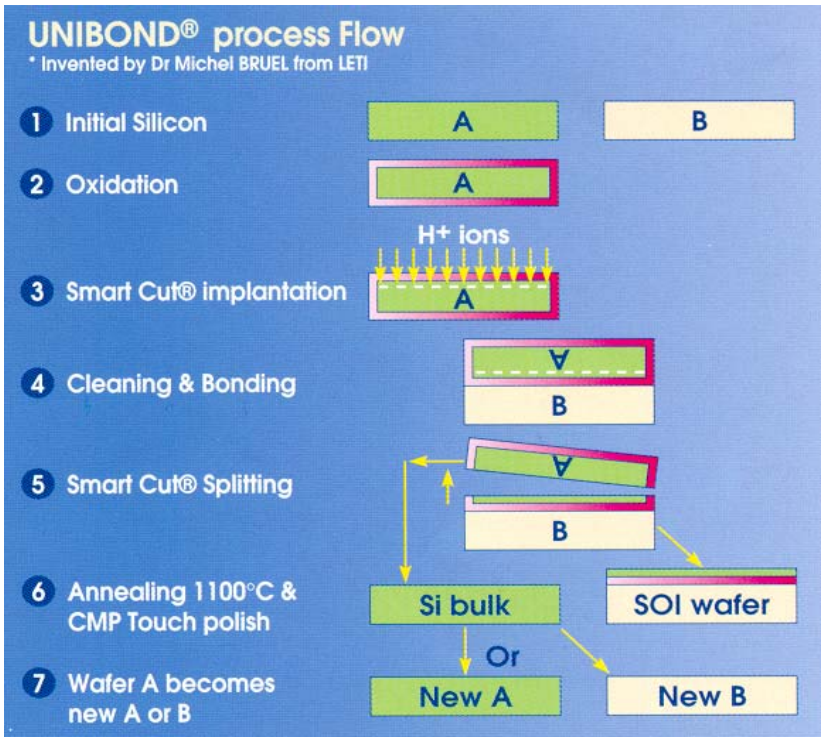


Figure 2.2-1 process flow for layer transfer using Smart-Cut.

The layer splitting process occurs as a rapid fracture of the Si layer (in the order of ms) once the fracture conditions are reached during the thermal anneal after the implant and bonding process. The Smart-Cut process builds on the extensive studies of the formation of "blisters" by implanting semiconductor materials with high-doses of light ions (usually H or He) [Chu77, Ascheron89]. The blisters form when internal gas bubbles grow together and locally deform the implanted region. When the stress is high enough, the internal gas pressure breaks of the entire implanted layer at a depth close to the implant damage depth [Ascheron89, Hochbauer99].

The time for the fracture conditions to be established depends on the anneal temperature, the implant conditions (dose, energy), the bonding process and the doping levels in the Si layer.

Some of these kinetics are shown in Fig. 2.2-2. The "standard" process uses a 69 keV H^+ implant at a dose of $5.5x10^{16}$ H/cm^2 and the "high dose" condition is 10^{17} H/cm^2. There is a sharp transition between a high activation energy (1.4 to 2.5 eV) regime at low temperatures and a low activation (~0.47 eV) process at higher temperatures. The 0.47eVactivation energy is comparable to the energy for diffusion of atomic Hydrogen in lightly doped Silicon, suggesting that at the higher temperatures the limiting factor is the diffusion of Hydrogen into the fracture region.

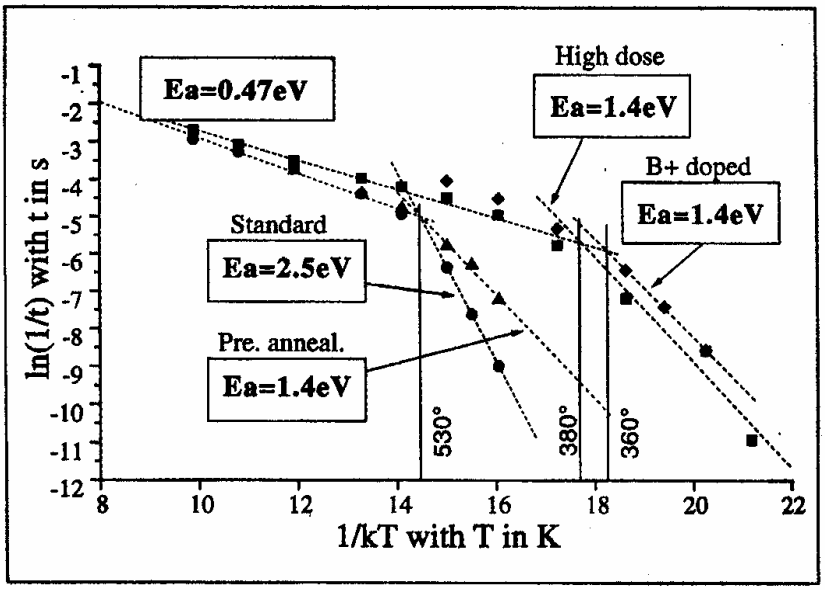


Figure 2.2-2 Kinetics of the time needed to establish the Smart-Cut fracture conditions.

The details of the Smart-Cut fracture depend on the chemistry of Si-H bonds at internal surfaces created by the implant damage and the formation of Hydrogen filled bubbles that provide the internal stress leading to the fracture event [Weldon97, Weldon99]. Changing the doping levels from ~10^{14} to $5x10^{20}$ B/cm^3 shifts the transition temperature between the two activation energies down by 200°C, a comparable effect to doubling the Hydrogen implant dose.

The implanted depth of the hydrogen ions determines the initial thickness of the transferred Silicon layer. Since the as-split surface is rough, on the order of 5 to 12 nm in root-mean-square (RMS) values from atomic-force microscope (AFM) measurements depending on the implant dose, it is then polished with a chemical-mechanical polish (CMP) tool to remove the remaining implant damage and Hydrogen-filled bubbles and to obtain Silicon surfaces smooth enough (RMS of a few Angstroms or less) for electronic device fabrication. The final thickness of the SOI wafer is then somewhat thinner than the as-split wafer and requires good control on the CMP process to obtain uniform thickness in the Si-SOI layer.

A first-order estimate of the energy needed to fracture and transfer a given thickness Silicon is the Hydrogen ion range [Fig. 2.2-3]. For Si-SOI layer thickness for partially-depleted CMOS, ~1000-3000 Å, the Hydrogen ion energy is 10 to 20 keV. In this energy range the profile straggling is a small fraction of the ion range, so the Hydrogen damage and atomic profiles are strongly peaked near the bottom of the implant profile. For thinner SOI layers needed for fully-depleted devices, Si-SOI <500 Å, corresponding to Hydrogen ion energies of 1-3 keV, the straggle scale is comparable to the ion range and the splitting region is not so sharply defined. The large relative straggling of the low energy Hydrogen profiles increases the relative thickness

of damaged and Hydrogen-soaked Silicon material which must be polished away to obtain device-quality material. So new variations on Smart-Cut will be need to be developed for ultra-thin SOI layers.

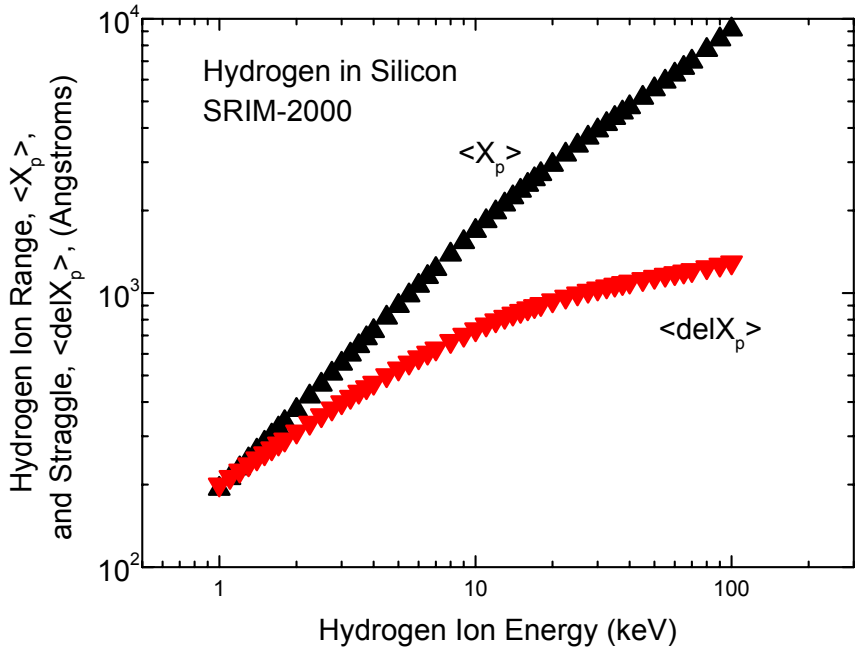


Figure 2.2-3 Ion range, <Xp> and straggling, <ΔXp> for Hydrogen in Silicon.

2.3 Atomic-layer cleaving for SOI and sSOI fabrication

Ion implantation can be combined with other layer transfer techniques to build a Si cleave plane that can be separated at room temperature with an as-cleaved surface smoothness of the order of 1 Å [Current00]. This SOI fabrication process, Nanocleave™, [Fig. 2.31.] begins with the formation of a cleave plane and a Si-device layer on a "donor" wafer. An ion implant is used to lower the bond strength of the cleave plane and serve as a "trigger" for the cleave process. An oxide is grown on the donor and a bonded wafer pair is created with a donor and an oxidized "handle" or device wafer. Since the bond strength of the donor-handle interface is significantly higher than the interface strength at the cleave plane, a novel cutting process is used to separate the Si-device layer from the donor wafer, creating a SOI structure on the handle wafer. If the device wafer contains a strained layer, SSOI structure is created.

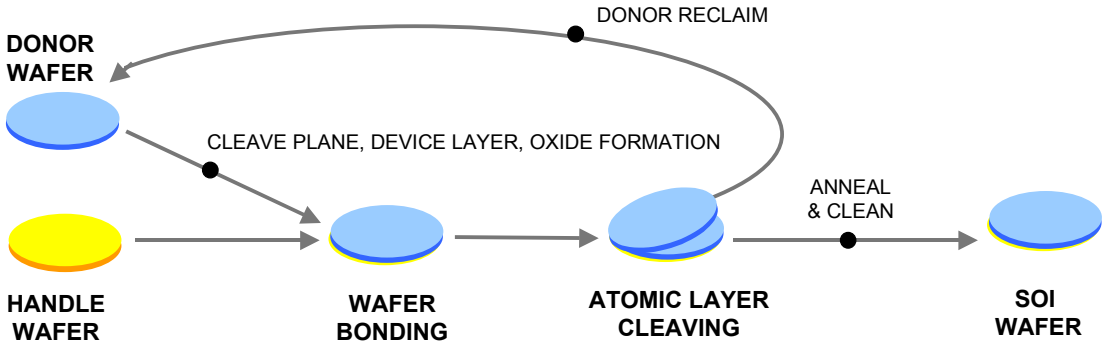


Figure 2.3.1 Schematic of the Nanocleave layer transfer method for formation of SOI wafers.

The implantation step in the Nanocleave process is designed to obtain optimal cleaving action at room-temperature [Fig. 2.3.2]. For thin-SOI, with Si-layers in the range of 50 to 400 nm, a standard high-current ion implanter is well suited to the production demands for modest volumes (5 to 20k wafers per month) of 200 mm SOI wafers. For Si-device layers thinner than 50 nm, the range of the ions used in this process dictate that efficient techniques must be available to implant these ions at energies of less than 10 to 20 keV. Since these ion energies are approaching the low end of the capabilities of beamline ion implantation systems, plasma immersion ion implantation (PIII) has been industrialized for SOI production [see the chapter on PIII techniques].

When the cleave plane bond strength properly engineered, a cleave front can be propagated smoothly across the wafer along nearly a single atomic plane. The result is an SOI wafer that does not need to be mechanically polished to remove damage or to achieve a surface roughness suitable for IC fabrication. The edge of the SOI layer, where the bevel curvature of the donor and handle wafers prevent bonding of the layers, is also defined by cleaving along <111> and <110> planes for a Si(100) surface [Fig. 2.3.3].

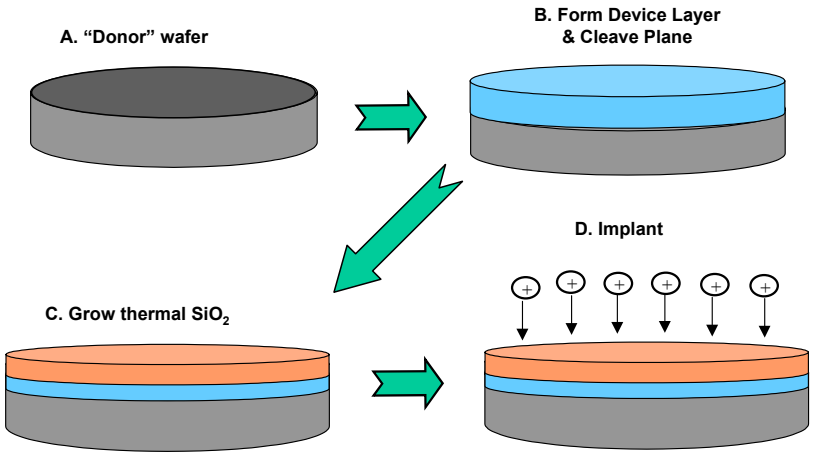


Figure 2.3.2 Schematic of the Nanocleave donor wafer process steps prior to bonding showing the implant sep to optimize the cleave plane bond energy.

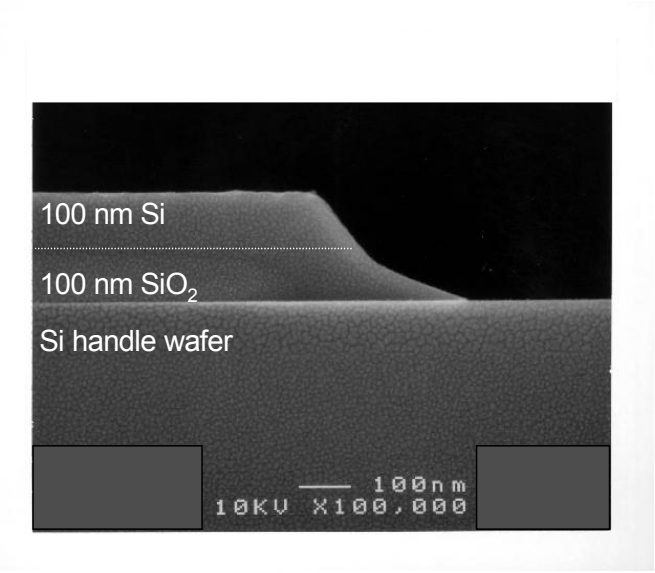


Figure 2.3.3. SEM side view of the SOI layer edge contour for Nanocleave wafers.

2.4 ELTRAN™ Process

Another layer transfer process for formation of SOI wafers, ELTRAN (Epitaxial Layer TRANsfer), uses a layer of porous Silicon to form the splitting plane [Yonehara99] and does not use ion implantation. The process flow is outlined in Figure 2.4-1. The porous Silicon layer is formed by anodic etching in an HF/C2H5OH solution and then annealed to seal the surface of the porous layer. The Silicon device layer is grown on the porous Silicon layer and then bonded to a handle wafer. The wafers are split by a water jet [Sakaguchi00] then annealed in H_2 to obtain a device-quality Silicon surface.

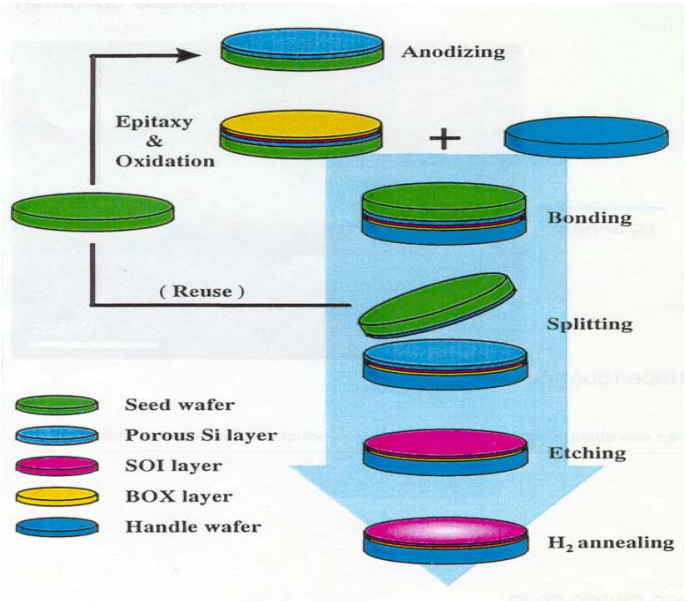


Figure 2.4-1. Process flow for ELTRAN SOI wafer fabrication

3.0 Layer lift-off in Diamond

Techniques used for SOI wafer fabrication are being extended to other electronic materials, such as SiC, InP, GaN, etc. [Tong98]. The implantation of chemically-active species provides an additional mechanism to the stress-related implants used in some SOI fabrication methods. In the case of diamond films, efficient layer lift-off can be achieved by high-dose implantation of Oxygen ions.[Parikh92, Tzeng93]. Although diamond is very stable in an oxidizing ambient, graphite react readily and produces a CO_2 gas product. This has been used to etch diamond films after high-dose implantation of Carbon and annealing to form a graphitic layer at the peak of the damage distribution [Parikh92]. The process is enhanced if Oxygen ions are used to created the buried damaged layer because the implanted ions provides an internal source of Oxygen to supplement the gases from the annealing ambient [Fig. 3.1]. An Oxygen dose of $3x10^{17}$ O/cm^2 has been used with 4-5 MeV ions to lift off ~2 um thick layers of crystalline diamond during annealing at 550-600 C [Parikh92].

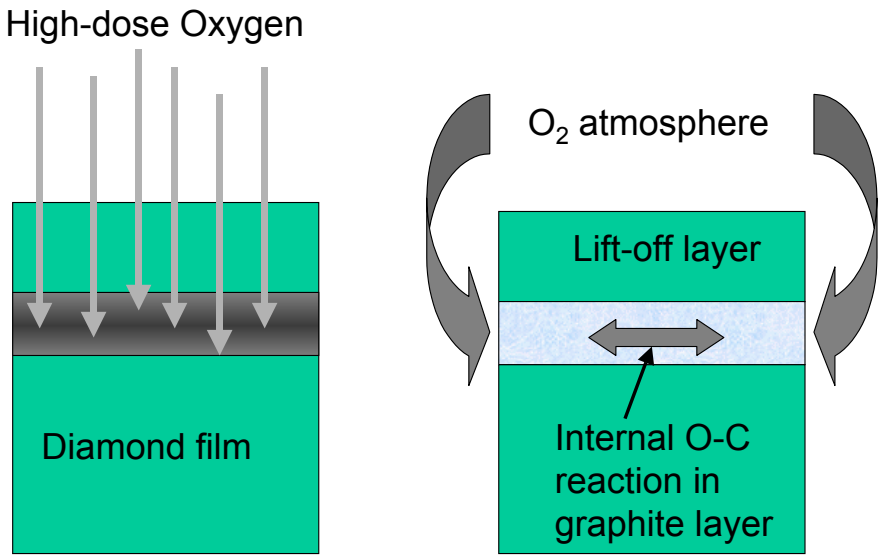


Figure 3.1 Schematic diagram of a process for lift-off of diamond films where a high-dose implant of Oxygen is used to create a buried damaged layer. During annealing the damaged layer is converted to graphite. The graphitic-carbon reacts with the oxidizing ambient and the implanted Oxygen atoms to from CO_2 gas and undercut the lift-off layer.

4.0 Challenges for SOI

One of the biggest challenges to bring SOI application into low-end consumer market is its high cost. The SOI wafer cost has to be brought down substantially from its current level to make it attractive for consumer electronics. With ever decreasing SOI thickness for future generation CMOS technology on larger diameter wafers, and increasingly tighter specifications for every physical and electrical parameter included in Table 2.1.1, meeting lower cost targets is challenging. From technology point of view, process integration with ultra thin layers will require raised source/drain structures. Doping of extension regions may lead to amorphization of the entire SOI, thus creating highly defective region next to the channel. Control of lateral diffusion of dopants (in particular boron) from extension regions into the channel will be another challenge.

In addition, there will a negative impact on carrier mobilities in the channel because of the proximity of the SOI/BOX interface to the gate. As technology moves away from conventional SOI substrates to Strain-Si SOI to increase CMOS performance, a host of additional new challenges will need to be addressed for substrate engineering and its implementation into manufacturing.

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