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Abstract

The continued scaling of complementary metal oxide semiconductor (CMOS) device technologies has lead to continued device shrinkage and decreases in the V_{dd}, the operating voltage of the device transistors. Scaling has meant denser circuitry overall, thinner silicon (e.g., SOI) in logic applications and less charge on capacitors for volatile memory. These trends have resulted in devices being more sensitive to soft errors since now low energy alpha particles can flip a memory bit or alter timing in a logic circuit. The alpha particle source is, in many cases, self inflicted, because alpha particles are commonly generated in materials adjacent to the chip, solders and in the packaging. In this paper we discuss several schemes by which these alpha particles can be blocked, such that all of their energy is absorbed before reaching the sensitive silicon circuitry at the transistor level. These alpha blocking layers are shown to be effective both through the use of modeling and through experimental measurements.

Introduction

The oldest soft error upset (SEU) problem can be tracked to certain packaging materials used in integrated circuits [1]. These materials contain traces of radioactive atoms which emit alpha particles. An alpha particle is a helium-4 nucleus, which is composed of two protons and two neutrons, and carries two units of electronic charge which can ionize material along its path. A noteworthy example is lead (Pb) which is a common soldering material used in integrated circuits. An isotope of lead, ^{210}Pb is radioactive, and eventually decays through β-emission to ^{210}Po, which itself is radioactive and emits an alpha particle as shown in equation 1:

$$^{210}\text{Po} \text{ -------> } ^{206}\text{Pb} + ^{4}\text{He (5.3 MeV)} \qquad (1)$$

The alpha particle in (1) carries a kinetic energy of 5.3 MeV. When an alpha particle penetrates the materials above a device and hits a sensitive volume, e.g., a depletion region in a semiconductor device, it can generate an electrical pulse

which can lead to a SEU in the circuit (A 5.3 MeV alpha travels about 5% of the speed of light; it has a mean range of 26 microns in silicon, and 23 microns in SiO_2).

The origin of alpha-induced SEU is well known. The mitigation of this problem relies on improvements in the packaging processes and using materials which do not emit alpha particles. From a research standpoint, alpha-induced SEU for each new technology provides a prototypical scenario for how an ionizing particle interacts with a semiconductor device. Experiments using mono-energetic alpha ions (and other heavy ions) and theoretical device simulations of ion strikes are essential to form an understanding of device sensitivity to this failure mechanism.

As an example of alpha particles emitted from semiconductor materials, Fig. 1 shows the energy spectrum of alpha particles from a Hitachi ceramic package, as a function of energy. A large area silicon detector located just above the ceramic was used to determine the energy distribution for the alpha particles. Since the count rate was very low a background subtraction was performed, using a silicon wafer in place of the ceramic. The integrated count rate was 30 cts/cm^2-khr, with 12% of the alphas having energies higher than 5 MeV. The discontinuous count rate at ~5.3 MeV is associated with detector contamination from a ^{210} Po source.

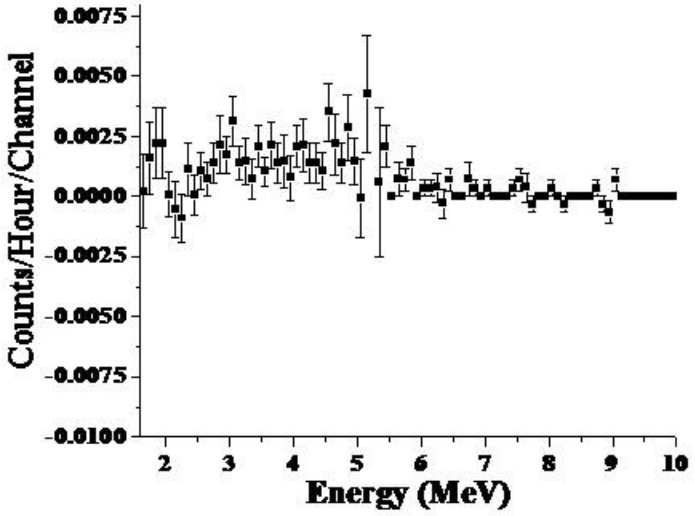

Fig. 1

Figure 1: The alpha-particle emission spectra SEU from a commercially available ceramic package. Twelve percent of the alphas have energies higher then 5 MeV. The background count rate from the detector has been subtracted.

Soft error upsets have become increasingly problematic in newer CMOS technologies. The primary cause of such upsets is the generation of alpha particles which propagate through the IC leaving a track of electron-hole pairs (charge) causing transitory effects such as adding or depleting charge on

capacitors and altering the timing. These non-repeatable events cause information to be lost (changing bits in the volatile memory) or computers to lock (incorrect timing causing latches to freeze). Alpha particles are generated through a radioactive decay process in certain elemental isotopes. Materials in or near the IC such as lead in the solder or uranium and thorium in the ceramic package can generate alphas.

To improve the density and speed of CMOS devices the trend has been a continual scaling of geometric dimensions and electrical parameters. This has lead to changes in SEU's. Overall the increased density and lower power requirements (V_{dd}) has lead to increased SER, since it takes less charge (energy) to cause failures [2]. SER in volatile memory, in many cases, can be ameliorated through software using error correction code (ECC). This luxury does not exit in logic, where circuit redundancy is required. This, however, can be costly. In this paper we have investigated several hardware approaches to overcome some of these alpha particle-induced SEU issues.

The approaches we have investigated entail additional layers sandwiched between the traditional last level of metallization on the chip and the solder used for attachment to the ceramic package. There are two approaches to consider; the first is to extend the current BEOL using a copper damascene integration approach and the second is to add a layer of Si (silicon interposer), containing through vias for contacts. For the first approach two options were explored; (1) Cu in SiO_2 and (2) Cu in photosensitive polyimide (PSPI). In addition to serving as blocking layers, additional circuitry can be added to these layers, such as passive electronic components, to enhance chip performance. The advantage of the Si interposer approach over the Cu damascene approach is that it can be produced and tested independent of the IC chip, lowering both the cost and good die yield loss.

Figure 2 shows how a blocking layer can be used to absorb alpha particles to reduce the total flux and the average energy. A thick thorium foil (^{232}Th) was used as a source of alpha particles, Kapton foils of various thickness (0.5 and 1.0 mil) were used as blocking layers and a Frisch Grid detector [3] used to determine the energy distribution of the transmitted alpha particles. In the figure, the curves show the energy spectrum from the source and after passing through 0.5 mil or 1.0 mil of Kapton foil. Note that the alpha-particle spectra from the unblocked thorium source is continuous (no distinct peaks). This comes about because alphas are generated from various depths in the source and undergo absorption before leaving the surface. It is clear that as the thickness of the Kapton foil is increased a decrease in the alpha particles maximum energy and average count rate occurs.

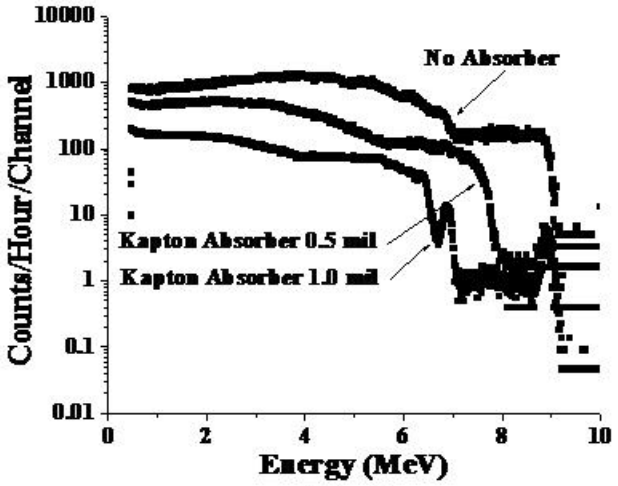

Figure 2: Alpha particle emission spectrum from a ^{232}Th source shown as counts/hr-channel vs. energy with and without Kapton absorber layers of 0.5 and 1.0 mil thick.

Experimental

The experimental structures (alpha blocking layers) were built on the microelectronics research laboratory (MRL) semiconductor pilot line at the IBM Thomas J. Watson Research Laboratory. The metallic materials used in the structures were electroplated Cu, sputtered Ta, TaN, Ti and chemical vapor deposited W and TiN. The dielectric materials used were low pressure chemical vapor deposited SiO_2 Si_3N_4, and spun on photosensitive polyimide (DuPont HD-4010 PSPI). The processing of the features was completed using conventional semiconductor technology processing tools and techniques. The final structures consisted of Cu damascene pads in SiO_2, 15 or 30 μm thick, Cu damascene pads in PSPI, 12 μm thick and 70 μm thick Si with W annular, through vias, to provide electrical connection to the chip.

In order to test the effectiveness of the blocking layers, free standing membranes were fabricated and tested, with the Si being removed from the Si wafer backside using a XeF_2 dry, chemical process.

The transmission of alpha particles through the structures was modeled using SRIM [4,5] and experimentally measured using an alpha-particle beam from a 3 MV Tandem accelerator equipped with suitable sample holders, pin hole apertures and Si detectors.

The monoenergetic alpha particles used for the transmission experiment of the copper structures had incident energies of between 3.5 and 8.5 MeV. The alpha particles struck membranes at normal incidence. Alpha particles that were energetic enough to pass through the membrane were collected on a solid state

detector with a 0.25 mm diameter pinhole aperture, used to keep the count rate low in the detector, and to ensure than the beam passed through the membrane and not the surrounding areas.

Testing of the Si interposer blocking scheme required energetic particles with longer ranges in Si than alpha particles, since even at 8.5 MeV, 60 μm of Si is a complete alpha block. Monoenergetic protons of normal incidence were used for the transmission experiment with energies of between 2.5 and 4.0 MeV. SRIM was used to model the transmitted proton energies.

Results

It is first necessary to determine the materials and their thicknesses for an effective alpha blocking layer. Figure 3 was generated using SRIM modeling and gives one a general idea of the required blocking layer thickness. It shows the alpha blocking layer thickness as a function of copper concentration in a Si-Cu homogeneous alloy necessary to stop alpha particles of 5.3 and 8.8 MeV. Also represented are the stopping thickness for common CMOS materials such as SiO_2, photosensitive polyimide (PSPI), tantalum and aluminum. The alpha energies were chosen based on the most energetic particles from Pb based solder (5.3 MeV) and from Th, where trace amounts can be found in ceramic chip carriers (8.8 MeV).

As an example one can consider a Si(40% Cu) alloy and determine the thickness necessary to stop both low and high energy particles. In order to stop 5.3 MeV alpha particles a 16 μm thick layer is required. To be more conservative one should account not only for the range of the alpha particles in the material but, in addition, the variation in stopping distances (straggle). In this example, a thickness of 17 μm, will cause ~99.7% of the alpha particles to be blocked. A thickness of 35.5 μm is needed to stop 8.8 MeV alpha particles. The conventional back end of the line (BEOL) for state-of-the art CMOS devices is necessarily between 8 - 12 μm in thickness. Therefore the actual amount of extra material necessary to block the alpha particles is 23.5-27.5 μm for the higher energy particles. Note that a homogenous Si-Cu alloy has been used for ease of modeling. In actual chips many paths exist with a large variation in Cu density, so, e.g., as an alpha particle transverses the BEOL, it may in some cases see no Cu or in other cases more than 40% Cu.

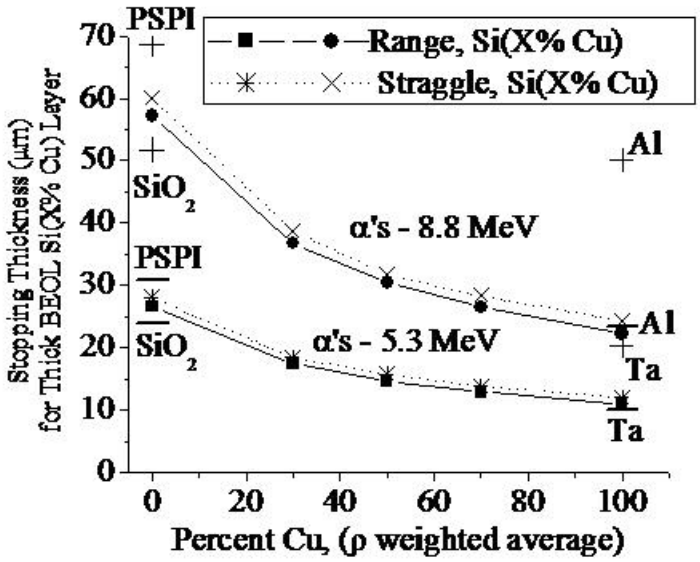

Fig. 3

Figure 3: Alpha particle stopping thickness in micrometers for a homogeneous Si(X% Cu) layer as a function of Cu in the layer. Alpha particles of two energies are considered; 5.3 and 8.8 MeV. Also shown are the stopping thicknesses for SiO_2, PSPI, Ta and Al, pure films.

A comparison of alpha stopping thickness for other common CMOS materials reveals why the choice of Cu imbedded in SiO_2 or photosensitive polyimide is good. A Cu thickness of 24.5 μm is needed to stop higher energy alpha particles. A common Cu barrier material, Ta, has to be 20 μm thick whereas an Al layer, 50.0 μm. The alpha stopping power of Cu is fairly large, there is not much to be gained going with a higher atomic weight material. Over the past eight years much effort has gone into the Cu damascene metallization scheme for the BEOL, therefore there is a big integration advantage for using Cu compared to other metals. The higher energy alpha stopping thickness for Si is 57 μm as compared to 51.5 μm for SiO2, and 69 μm for PSPI.

In summary Fig. 3 allows one to determine the thickness necessary for alpha mitigation layers. The blocking layers considered in this paper consist of a damascene Cu structure in SiO_2 and in PSPI with about 40% Cu by volume. A third blocking layer scheme considered consists of a Si layer with through vias for electrical connections. The thickness of the blocking layers necessary for the three schemes are; ~40 μm for the Cu in SiO_2, ~50 μm for the Cu in PSPI and ~60 μm for the Si layer, to effectively stop all of the high energy alpha particles typically encountered in modern IC and packaging fabrication.

The three alpha blocking layer schemes are depicted in Fig 4. Figure 4a shows damascene Cu in an SiO_2 dielectric. A Cu via is used to connect to the last layer of the BEOL, on the IC, and the pad is used to connect to a package. The drawing shows a one level, dual damascene process, but many layers can be produced to meet the ~50 μm thickness needed. Besides connecting the IC to the package the additional layers can be used to build passive components and clocking circuitry which take up large areas and would be prohibitively expensive if laid out using a conventional BEOL. Fig. 4b is identical to Fig. 4a except the SiO_2 dielectric is replaced with photosensitive polyimide, making the processing simpler. The reactive ion etching (RIE) steps needed for Cu in SiO_2 are eliminated. After the final PSPI cure the damascene structures can be metallization.

The third scheme, Fig. 4c, depicts a layer of Si interposed between the last BEOL layer and the package. The connections are made with W filled annular vias. The advantage of such vias is minimal deposition of W, thus, reducing the amount of chemical mechanical polishing (CMP) time for W removal in the field areas. The width of the annular vias is < 4 μm, and, since the CVD W process is conformal, only 2 μm of CVD W accumulates on the field region during fill. The depth of these vias is as much as 70 μm. After via formation a Cu pad is placed on one side. Next the Si is ground and wet etched (removed) from the opposite side to expose the W vias. Finally, a second Cu pad is deposited, covering the exposed W vias. The package attach is done using conventional solder, whereas attachment to the IC is done through the use of a Cu-Cu, high pressure and temperature, bond.

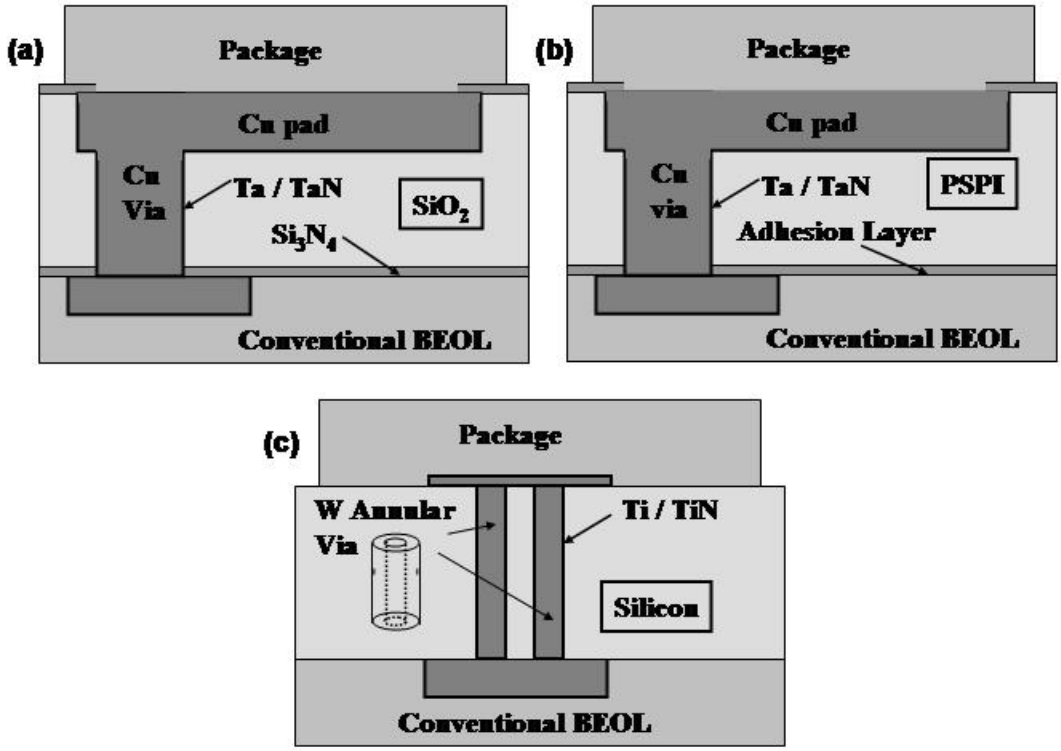

Fig. 4

Figure 4: Schematic representations of three different alpha mitigation layer builds; a) a Cu damascene build in SiO_2**,** b) a Cu damascene build in photosensitive polyimide and c) a silicon interposer build.

The reduction to practice of the alpha mitigation scheme shown in Fig. 4a is demonstrated in Fig. 5. The top down and cross sectional Scanning Electron Micrograph's (SEM's) reveal one layer of damascene Cu in SiO_2. Figure 5a shows the checkerboard Cu fill pattern that was used and Fig 5c shows the wire bond features at the edge of the individual chips. The cross sectional SEM images of Fig. 5b and 5d show the ~15 μm thick layer with imbedded Cu pads. The volume fraction of Cu in the checkerboard pattern region is ~40%.

The structure depicted in Fig. 5a was tested using an alpha-particle beam. After the Cu damascene-in-SiO_2 structure was fabricated, Si from the substrate was removed from the backside in a ~3 mm area using XeF_2. The remaining membrane ~ 15 μm thick was then placed in an alpha beam at normal incidence. The energy of the beam was adjusted from 4.5 to 8.5 MeV. An aperture of ~ 0.25 mm diameter was placed in front of the sample, and aligned so as that the beam passing through would be in the center and most uniform region of the membrane. Behind the sample a silicon detector was used to collect the transmitted alpha particles as a function of energy. Figure 6a shows the measured alpha particle energy spectra of the beam after passing through the membrane as a function of

the incident energy. Note that for each incident alpha energy there are two major peaks in the spectra. The high energy peak is associated with alpha particles propagating through the SiO_2 and the low energy, broader peak is associated with those alpha-particles transiting the Cu.

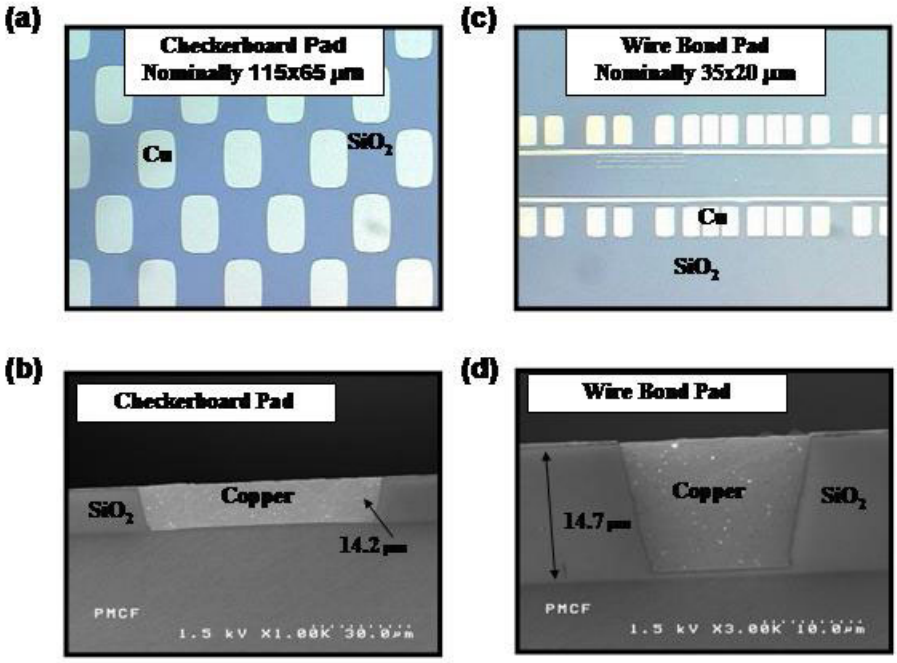

Fig. 5

Figure 5: Scanning electron microscopy (SEM) images both top down and in cross section showing an actual build represented by the schematic in Fig. 4a. a) and b) represent the "checkerboard" Cu damascene features and c) and d) the "wire bond" features.

Modeling of the transmission of alpha particles through the Cu and SiO_2 was performed using SRIM [4] and the results are shown in Fig. 6b. In this figure transmitted alpha-particle energy is plotted against incident alpha energy. The curve with solid, circular symbols indicates the transmission through SiO_2 and the solid, squares through the Cu. Incident alpha-particles with energy less than ~3.75 MeV are completely blocked, those between 3.75 and ~6.5 MeV are blocked by the Cu but pass through the SiO_2, and those with energies higher than 6.5 MeV pass through both materials. Transmission energies for incident alpha particles of 7.5 MeV are indicated on the plot with dashed lines.

If one considers an incident alpha particle of 7.5 MeV one can determine the energy it has after transmission through the membrane. Following the vertical dashed line at 7.5 MeV (incident alpha energy) in Fig. 6b, one notes that if the

particle goes through the oxide layer, the transmitted energy is ~5.5 MeV, while those particles traveling through the Cu have a transmitted energy of ~1.5 MeV. The experimental results in Fig. 6a for an incident alpha-particle beam of 7.5 MeV shows a small peak at ~1.1 MeV, and larger peaks at 1.6 and 5.8 MeV, with the latter two in close agreement to the modeling results. The smaller peak at 1.1 MeV is associated with the beam going through the Cu in the "wire bond" region as opposed to the "checkerboard region", see Fig. 5. It was found due to the processing conditions used (dishing during the chemical mechanical polishing) that the Cu in the "wire bond" regions is slightly thicker compared to that in the "checkerboard" regions, by about 0.5 um and therefore the incident beam loses more energy through the thicker Cu.

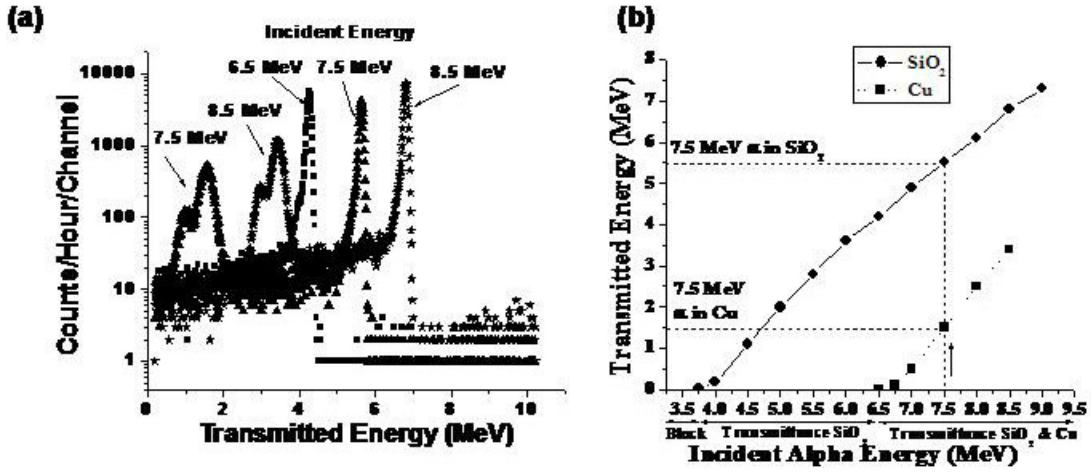

Fig. 6

Figure 6: Experimental data and modeling results for the Cu damascene build in oxide, shown pictorially in Fig. 5. a) The experimental transmission energy spectrum and b) The modeling results using SRIM data, which are in good agreement with the data.

The results of a two level Cu damascene build in SiO_2 are shown in Fig. 7. Figure 7a shows a cross sectional SEM of two "checkerboard" pad regions approximately 15 μm thick, built one on top of the other, for a total thickness of 29 μm. For the measurements the Si of the substrate was removed using XeF_2. The Cu is thick enough such that even alpha particles with incident energies of up to 8.5 MeV are blocked, although alpha particles with energies greater than about 6.2 MeV are transmitted through the SiO_2. Figure 7b shows a plot of alpha-particle transmission data for this membrane and only one peak is evident from the alpha-particle transmission in the SiO_2. Figure 7C shows a plot of experimental

and simulated transmission energies versus incident alpha energy. The results of the simulation and the experimental data are in close agreement.

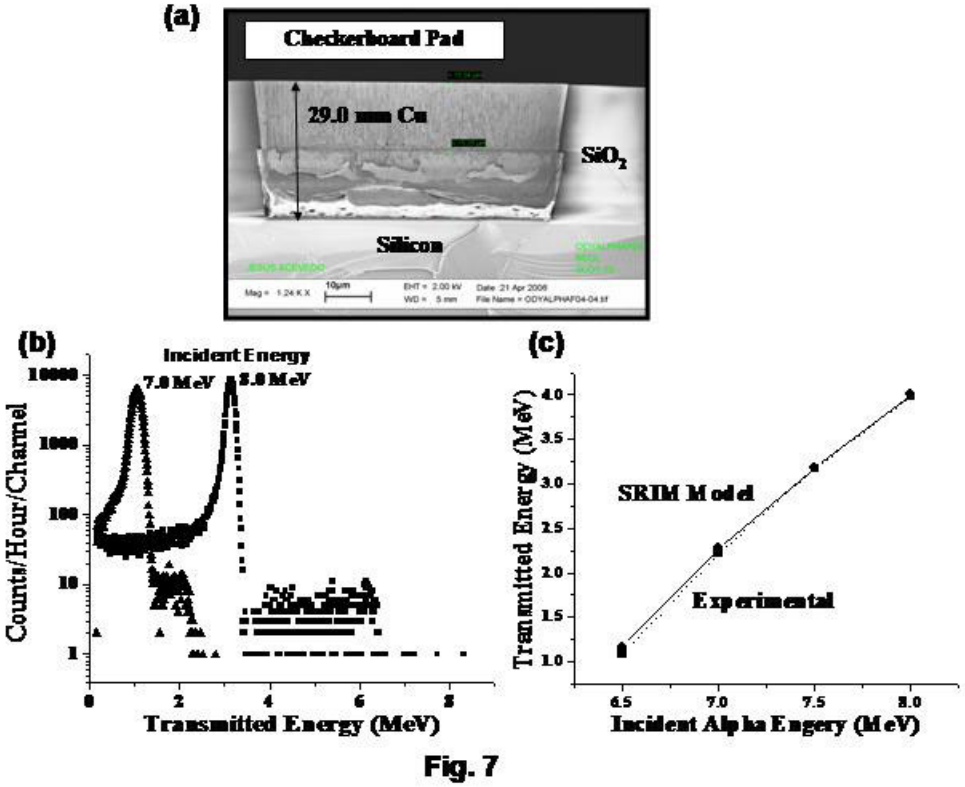

Figure 7: SEM**,** experimental data and modeling results for a two level Cu damascene build in oxide. a) SEM cross section of the structure which is 29 μm thick, b) The experimental energy spectrum and c) A comparison of the experimental to the modeling SRIM results which are in good agreement.

The Cu damascene-in-photosensitive polyimide build and alpha transmission results are shown in Fig. 8. Figure 8a shows a cross section view of this structure: a Cu pad in PSPI, ~12 μm thick with a ~1 μm SiO2 layer below. As opposed to the sharp features for the Cu in SiO_2 build, the PSPI build (by the nature of the polymer) has rounded features. The experimental and simulated results for this structure are shown in Fig 8b and 8c, respectively. Incident alpha particle energies from 3.5 to 8.0 MeV were used. Figure 8b shows the transmitted energies through the PSPI (higher energy peaks) and Cu (lower energy peaks). The rounded features lead to some particles being transmitted though both the PSPI and Cu and this gives rise to a long high energy tail on the Cu peaks. The simulated results

shown in Fig. 8c are in good agreement with the experimental data taking into account the oxide layer beneath the PSPI.

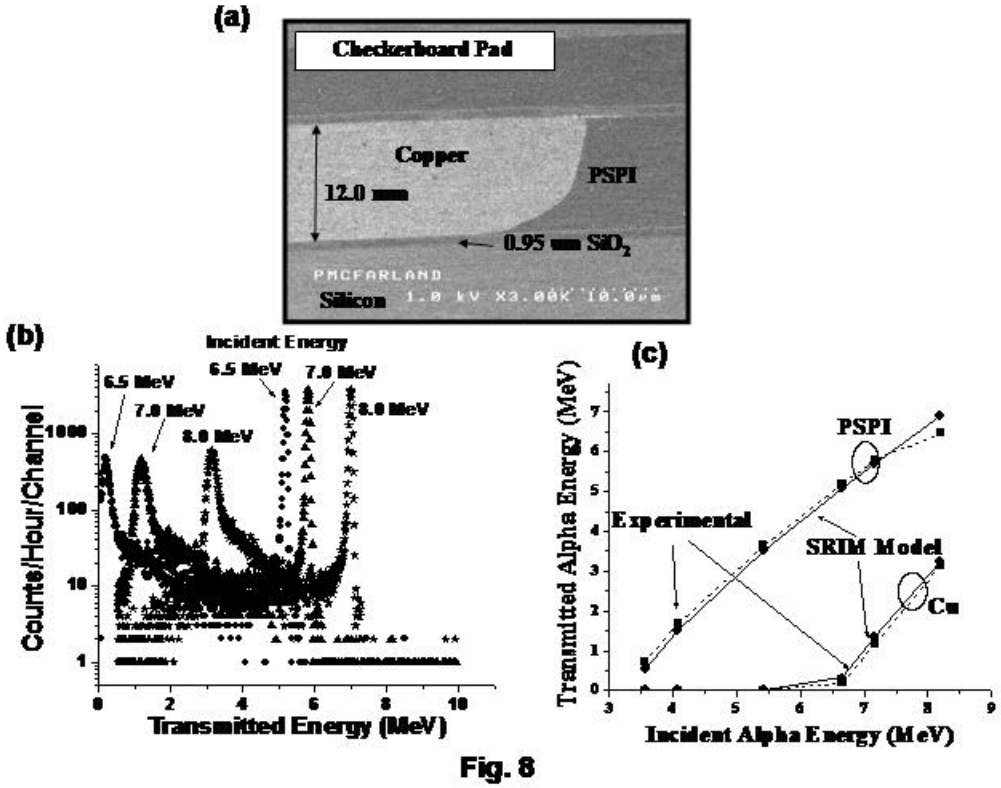

Figure 8: SEM, experimental data and modeling results for the Cu damascene build in photosensitive polyimide, shown schematically in Fig. 4b. a) SEM cross section of the build, b) The experimental energy spectrum for transmitted alpha energy through the membrane as a function of incident alpha energy and c) The SRIM modeling results.

The Si interposer alpha particle mitigation approach is depicted in Fig. 9. Figure 9a shows a cross sectional view of the structure which is ~ 64 μm thick with tungsten annular vias spanning the thickness for electrical interconnection. The experimental proton transmission data are shown in Fig. 9b, where the number of transmitted protons is plotted as a function of transmitted energy. The thickness of the Si layer (~ 64 μm) stops all alpha particles (up to 8.0 MeV tested), therefore it was necessary to consider the transmission of particles with longer range. A proton with as little energy as 2.5 MeV will pass through the Si layer (range 70 μm). Monenergetic protons of normal incidence and energies from 2.5 to 4.0 MeV were used to determine the quality of the blocking layer. The experimental transmission peak energies in Fig 9b are plotted along with the

SRIM modeled data in Fig. 9c, as a function of incident proton energy. The experimental results agree well with the modeled data. The additional transmitted proton energies above the peak maxima in, Fig. 9b, are associated with nuclear reactions between the proton beam and the materials used to form the annular vias.

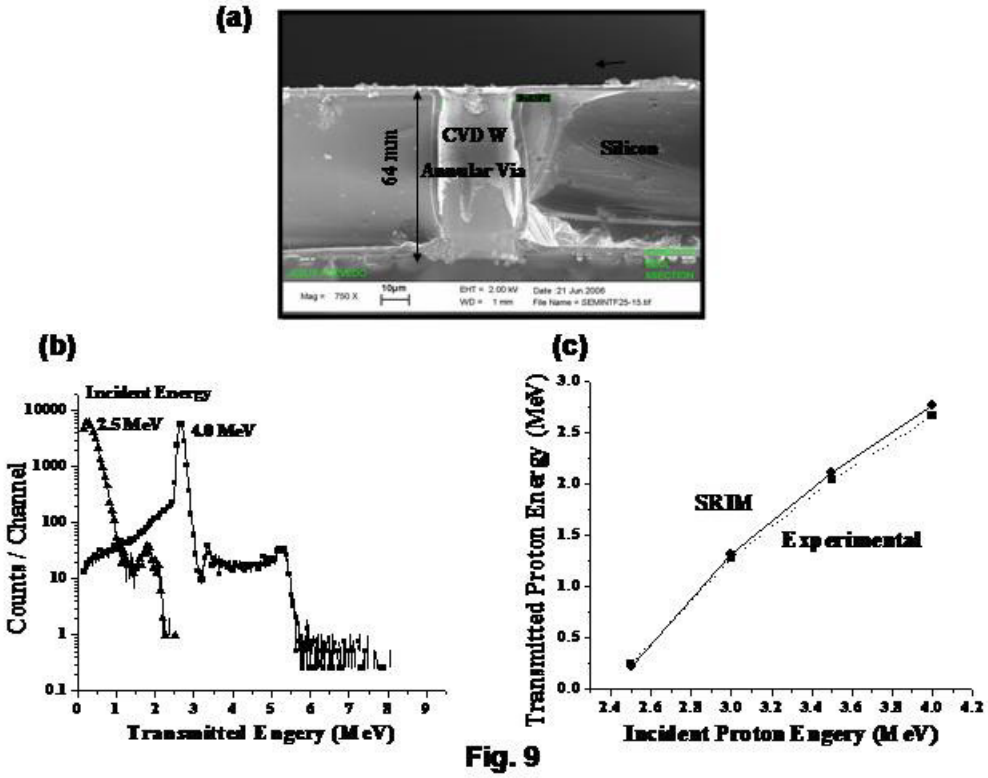

Figure 9: SEM, experimental data and modeling results for a silicon interposer build, shown schematically in Fig. 4c. a) SEM cross section of the build representing an annular through via, b) The experimental energy spectrum for transmitted proton energy through the membrane as a function of incident proton energy and c) The SRIM modeling results.

Discussion

It is clear that alpha particle mitigation will be necessary for current and future CMOS logic technologies. Possible approaches for such mitigation include transistor, circuit or system level deign to minimize SEU, low alpha generating materials and various types of blocking layers. All the approaches can be made to work, but in the end the cost of implementation will be the determining factor.

The first approach, optimized transistor, circuit or system design includes modifications to the conventional CMOS transistor (e.g. substrate/well

engineering, isolation using a buried oxide layer like SOI, and double gated devices) [6], modification of circuit layout (e.g. added devices on latches to increase capacitance or resistance) [6] and system level redundancy (e.g. either transistor or latch level) [7,8]. These approaches can lead to increased area and/or power usage and degradation in performance. Overall techniques to address SEU in logic are difficult compared to memory, since logic operations are performed precisely because the next machine state can not be predicted [9].

In terms of low alpha generating materials, currently low alpha lead is used in CMOS logic applications where the content of ^{210}Po is reduced by a factor of 100 to 15,000 to obtain alpha levels of 2 to 10 cts/cm^2-khr. To achieve such levels, purification is possible, but it is an extremely expensive process entailing vaporization, ionization and electrostatic separation. The standard method is the use of antiquity lead. This lead has been refined 100's of years ago removing the uranium and thorium content, such that the ^{210}Pb content has had time to decay without regeneration. ^{210}Pb has a half life of 22.3 years and is reduced by a factor of 15,000 in 310 years. The cost of obtaining antiquity lead is high, since the quantity is limited. Lead free solders are not quite the solution, since ^{210}Pb is a contaminant in materials like Ag, Bi and Sb. The current and most used mitigation approach, low alpha generating lead, does contribute to the increased cost of CMOS logic.

Likewise it is important to minimize the uranium and thorium content in the materials used to make up the ceramic / plastic packages. As with low alpha lead, it is expensive to refine these materials such that the alpha generating contaminants are greatly reduced or eliminated. As an added issue many of the machining / processing techniques for the ceramic packages themselves add alpha generating material.

There are several approaches to minimize or eliminate the alphas coming from the package by using adjacent absorbing layers. As an example instead of the entire ceramic package being made from low alpha generating materials only the top ~70 μm is necessary, since this layer will block the alphas from the bulk. This can be accomplished with the use of a thick, low alpha content ceramic or polyimide layer. Another absorbing layer scheme entails filling the volume between the package and the IC chip, surrounding the solder pads, so as to block the alpha particles coming from the package. Under-fill materials such as ceramic pastes, Kapton, and high viscosity liquids can be used to absorb the alpha particles. Unfortunately, none of these approaches stop the alpha particles from the solder, still necessitating the need for the added cost of low alpha generating Pb.

The schemes described in this article will stop alphas emanating from the solder and ceramic eliminating the need for low alpha content materials (e.g Pd, Al_2O_3), a large cost savings. Of the three schemes; Cu-damascene-in-SiO_2, Cu-

damascene-in-PSPI and the Si interposer, the later has a distinct advantage. The Si interposer is built independent of the logic circuitry and thus can be tested and sorted before installation. Depending on the attachment method (e.g. die to die) known good interposer chips and known good logic chips can be attached limiting yield loss.

Conclusion

Three different structures were shown and tested for blocking of alpha particles in order to reduce soft error rates. Two of these structures entailed increasing the thickness of the CMOS back end of the line, while the third introduced a silicon interposer layer. For adequate mitigation of high energy (8.8 MeV) particles a 40 μm Cu damascene scheme in SiO_2 , a 50 μm Cu damascene scheme in photosensitive polyimide, and a 60 μm scheme in silicon are required. Alpha transmission experiments were performed on 15 and 30 μm Cu damascene membranes in SiO_2, 12 μm Cu damascene membranes in photosensitive polyimide and a 70 μm silicon membrane. The experimental data correlate very well with modeled results using SRIM. All three approaches will adequately block the alpha particles, but for manufacturability, the cost and reliability will be the determining factor on choice.

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