RC24175 (W0702-031) February 7, 2007
Physics

IBM Research Report

Low-energy Proton-induced Single-event-upsets in 65 nm Silicon-on-Insulator Latches and Memory Cells

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Session Preference: Single-Event Effects: Mechanisms and Modeling

Presentation Preference: Oral , Presenter: K. Rodbell

Abstract

Experimental data are presented showing that low energy (< 2 MeV) proton irradiation can upset exploratory 65nm Silicon-On-Insulator (SOI) circuits. Alpha particle SER data, modeling and simulation results provide a plausible mechanism.

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I. Introduction

In earlier work the soft error rate (SER) critical charge required to upset 65 nm exploratory Silicon-on-Insulator (SOI) devices was found to be < 1 fC. The onset of single-event upsets was determined by measuring the upset frequency as a function of angle of incidence between a charged-particle beam and the device under test using He ions [1]. This paper explores the possibility of single event upsets induced by low-LET (linear energy transfer) fragments, using low-energy (1-2 MeV) protons from a Tandem accelerator. In this paper, data are presented showing that 65 nm circuits can be upset by direct ionization from low-LET protons. The implications of these new results are important for modern devices since terrestrial neutron-induced spallation events produce a substantial number of low energy protons. Also, in space applications, circuits and devices and their surrounding materials are constantly bombarded by high-energy protons and heavy ions, producing secondary nuclear debris. These secondary fragments (from spallation events) consist of a substantial number of both low-energy protons and alpha particles. As an example, Table 1 shows a few typical cross sections from proton-silicon spallation reactions. Fig. 1 shows the energy differential cross sections from the inclusive ^{28}Si(p, p' x) and ^{28}Si(p, ^{4}He x) reactions. The underlying energy spectra are simulated using the NUSPA code [2], and weighted by the terrestrial neutron flux at sea level over the neutron energy range from 20 MeV to 1 GeV. An implication of this work is that low energy protons, produced by spallation reactions, are able to upset modern SOI chips, containing low critical charge devices.

Table 1. Some Typical Cross Sections for Proton-Silicon Reactions Simulated by NUSPA

Proton Energy (MeV)	Reaction Cross Section (XS) (mb)	Proton Inclusive XS (mb)	He-4 Inclusive XS (mb)
50	563	858	138
150	422	867	197
500	448	1226	371

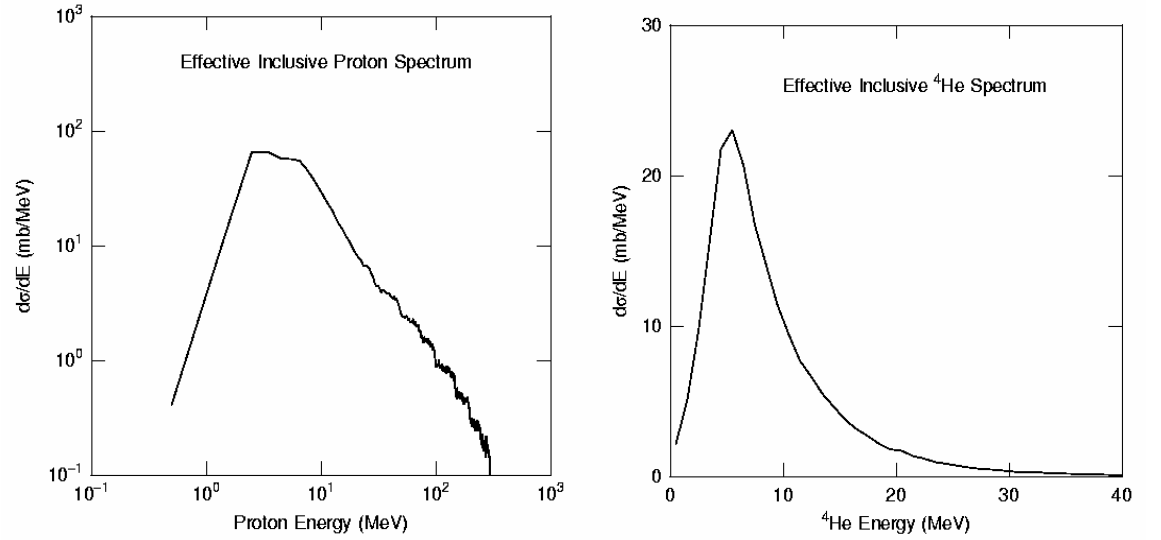

Figure 1. Plot of the energy differential cross-sections of protons (left) and alpha particles (right) vs. particle energy for (a) left, ^{28}Si (p, p' x) and (b) right, ^{28}Si (p, alpha x). The energy spectra are computed using NUSPA code [2], and have been weighted by the terrestrial neutron flux at sea level over the neutron energy range from 20 MeV to 1 GeV.

II. Experimental setup

The IBM T.J. Watson Research Center 3 MV Tandem Van de Graaff accelerator was used for Single Event Upset (SEU) experiments. Details of the experimental setup are given in [1].

III. Experimental data and analysis

Using IBM's 65 nm SOI technology, a series of test sites were built with exploratory array cells (SRAM) and latch designs to study the critical charge needed to upset these circuits. The array data were taken on one of these 65 nm array cell designs. Latch data were taken on the latch designs in both the data=0 and data=1 state. Data were typically taken at several voltages ranging from 0.4 - 1.6V and several different beam energies were used for the incident particles in order to avoid SEU's at normal incidence. The test sites were built using only a limited number of wiring levels with a total BEOL thickness ranging from 8 - 11 micrometers. Initially data were taken using an alpha particle beam and the Qcrit was determined by the method outlined in [1].

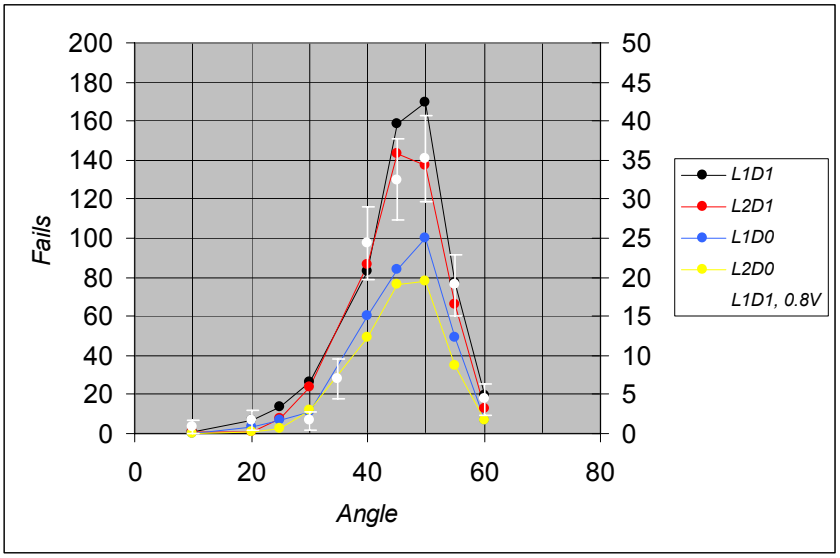

Figure 2. SEU fails as a function of angle of incidence for L1/L2 and data=0 and data=1, at 0.4V (left-hand scale), and at 0.8V for the L1 latch, data=1 state (right-hand scale), using 1.25 MeV protons.

Based upon our alpha-particle data, we did not expect to see SEU events from proton bombardment (direct ionization) [3] since the maximum deposited charge with protons is considerably less than that for alpha particles. However SEU fails were found to occur with low energy proton irradiation. Fig. 2 is an example of data obtained on a scan chain, and shows the fail rate as a function of angle for both data states of the L1 and L2 latches using 1.25 MeV protons. Table 2 contains a summary of the critical angles and critical charge (fC) for both the SRAM and latches evaluated in this paper. The proton-induced critical charges are consistent for the two proton energies used in both the SRAM and latch exposures.

IV. Discussion

In this paper, experimental data are shown for upsetting 65 nm SOI SRAM and latch circuits with direct ionization from protons. For many years, it has been predicted that technology scaling

Table 2. Critical deposited charge (fC).

		He (alpha particles)		H (protons)		
Device	**Beam Energy (MeV)**	**Critical angle (degrees)**	**Critical charge (fC)**	**Beam Energy (MeV)**	**Critical angle (degrees)**	**Critical charge (fC)**
SRAM	**7**	**19 – 37**	**0.38 – 0.47**	**1.0** **1.5**	**38 - 41** **60 - 63**	**0.21 – 0.23** **0.24 – 0.27**
Latch	**5**	**20 - 26**	**0.6 – 0.65**	**1.25** **1.5**	**26 - 32** **40 - 47**	**0.14 - 0.15** **0.14 - 0.16**

would lead to SEU's with direct ionization from protons [4] and recent published data have shown this upset mechanism to exist in a bulk SRAM [3]. The work presented in this paper extends the analysis of upsets due to direct ionization with protons to SOI circuits built in the 65 nm technology node. In addition, this work shows that this upset mechanism exists in both SRAM and latch circuits. For the 65 nm SOI circuits operating in a terrestrial environment, one would expect only a modest increase in the total soft error rate due to upsets from direct ionization with protons (due to the low terrestrial neutron flux).

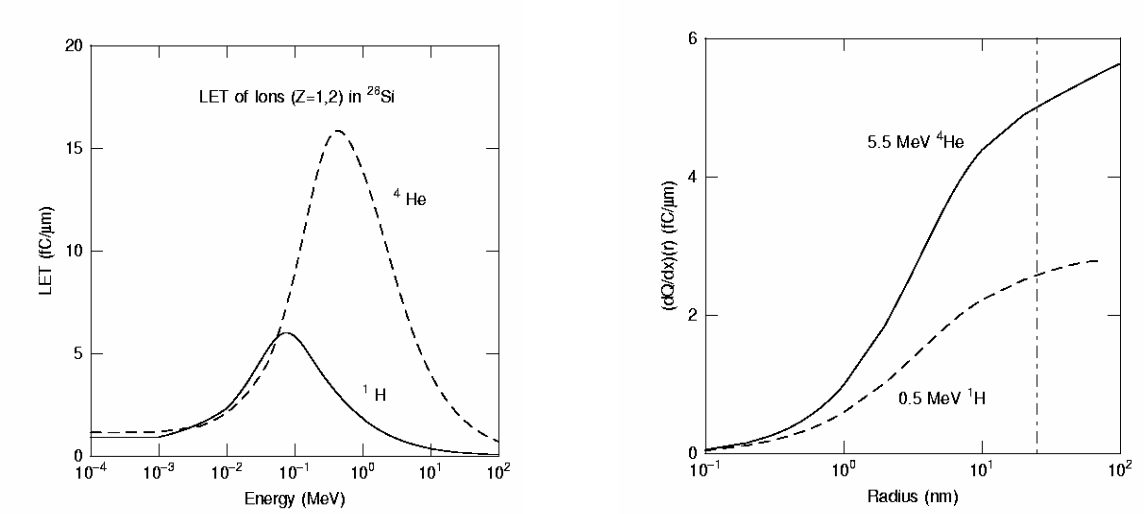

Figure 3(a), left, Plot showing LET (in units of fC/um) vs. energy for protons and alpha particles, and 3(b), right, the restricted LET vs. track radius of protons and alpha particles at energies, at the silicon surface, that correspond to the experimental conditions described in the text. The vertical dashed-dot line corresponds to a track radius of 25 nm.

Another important issue, highlighted in the data shown in this paper, is the relative effectiveness of upsetting the circuits with protons vs. alpha particles. As shown in Table 2, the critical deposited charge derived from testing with a proton beam is significantly lower than that obtained from alpha particle testing. This experimental result cannot be explained by a simple mechanism; it is most likely a result of the physical features of the 65 nm devices being comparable to the ionization charge track size of the striking protons and the alpha particles (see Figure 3). The 65 nm devices have source-to-drain separations of less than 50 nm. Figure 3(b) shows plots of the restricted LETs, (computed using models detailed in [5]) as a function of the ion track radius for a 5.5 MeV alpha particle and for a 0.5 MeV proton. These restricted LET's have units of charge/length, but are restricted (or limited) to the charge contained in a specified track radius.

The restricted LET, at a finite radius, is associated with the number of electron-hole pairs contained in a column bounded by this finite radius, computed by integrating the dose density over a finite radius. The proton and alpha surface energies shown in Fig. 3(b) correspond to the surface energies achieved during the proton and alpha particle irradiations. For protons most of the total charge is contained within the typical 50 nm device dimension. However, for alpha particles, the restricted LET curve is still rising at a radius of 25 nm implying that part of the alpha particle generated charge is spread out over a wider area (> 50 nm in diameter). Therefore, strikes directly through the device with a proton will tend to concentrate more of the generated charge in the body of the SOI device while the alpha particle will distribute more of the generated charge over a wider source – body – drain region. This suggests that an alpha particle experiment may overestimate the deposited charge required for upsetting modern SOI devices.

V. Conclusion

We have determined the critical charge required to cause SEU's in special 65 nm SOI latches and SRAM circuits using low-energy proton beams. These data show that low energy protons are capable of upsetting these circuits, even though the charge deposited in the device is less than expected based upon alpha particle beam experiments. Therefore, to accurately determine the total soft error rate, one must consider the upset rate generated by the direct ionization of protons. A significant number of these low energy protons are generated as a result of cosmic radiation spallation events

VII. References

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