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Circuit Techniques Utilizing Independent Gate Control in Double-Gate Technologies

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Abstract

Independent gate control in double-gate (DG) devices enhances circuit performance and robustness while substantially reducing leakage and chip area. In this paper, we describe circuit techniques which take advantage of the independent biasing properties of symmetrical and asymmetrical DG devices in design. DG circuits at the 25nm node are analyzed via mixed-mode numerical simulations using Taurus MEDICI. In dynamic circuits, we give examples of conditional keepers, charge sharing prevention scheme, and static keepers. A conditional keeper can dynamically achieve the optimal strength ratio between keeper and evaluation devices by utilizing the front- and backchannel currents in DG devices. A charge sharing mitigation scheme utilizing the back-gate of a logic transistor is then described. Static data retention scheme in dynamic circuits is proposed. A case study for analog applications using a voltage controlled oscillator (VCO) illustrates the specific advantages of DG devices.

I. Introduction

Double-gate (DG) devices are potential candidates for replacing planar CMOS beyond the 45nm technology node due to significantly better short channel effect (SCE). DG devices can be employed with tied gates or independently controlled gates configurations [1], [2]. The back-gate bias can control the threshold voltage (V_T) in fully depleted silicon-on-insulator (FD/SOI) devices with thin buried oxide (BOX) or in DG devices [3], [4]. However, V_T centering and multiple V_T's have been difficult with the tied-gate DG technologies. In contrast, independently controlling the front and back gates provides wide design and application opportunities without aforementioned constraints.

In symmetrical DG devices, very high body doping density with poly-silicon gate, or un-doped body with near mid-gap metal-gate materials, shown in Fig. 1(a), is used to set the desired V_T. In asymmetrical DG devices, the two gate electrodes consist of materials of differing work functions as shown in Fig. 1(b) [1], [2]. . For asymmetrical DG NFET, the front- and back-gate typically, consists of *n*+ and p+ poly-silicon, respectively. For asymmetrical DG PFET, the opposite type of gate is applied, i.e. *p*+ poly-silicon for the front gate and *n*+ poly-silicon for the back gate. The predominant front-channel has a significantly lower V_T and much larger current drive compared with the weak backchannel [7]. The front-channel V_T can be modulated by back-gate biasing through gate-to-gate coupling. This V_T modulation mechanism is significantly stronger than the well/body bias in bulk or partially depleted silicon-on-insulator (PD/SOI) CMOS devices. Fig. 2 shows the front-gate V_T vs. back gate bias characteristics of the two types of DG devices. For symmetrical DG device, the front-gate V_T remains relatively constant with back-gate bias, as the gate-gate coupling is limited when strong inversion charge at back surface pins back surface potential and shields further gate-gate coupling. For asymmetrical DG device, the V_T modulation effect is very significant, as the gate-gate coupling is extended until the back surface becomes strongly inverted (the weak back-channel has a high V_T, about 1.0 V higher than the front-channel). Notice that in bulk and PD/SOI devices, the effectiveness (and operating frequency) of the well/body bias is limited by the distributed RC of the well/body contact. It also tends to degrade with technology scaling due to the lower body factor in scaled devices. In contrast, the effectiveness (and frequency) of back-gate biasing in

asymmetrical DG devices is limited only by the gate and wire RC, same as the core logic. In addition, this modulation effect improves with transistor scaling due to stronger gate-to-gate coupling (as a result of thinner gate oxide and thinner silicon body).

DG devices can be employed with tied-gate or independently controlled gates [3-7]. Tied–gate circuit topology resembles conventional planar CMOS configuration while higher current density and drive capability is achieved with more compact layout area. When gates are controlled independently, symmetrical DG devices can reduce the transistor count, thus chip area, required to implement a given logic function [4]. In asymmetrical DG devices, the back gate modulates the predominant front channel current via gate-to-gate coupling [2]. Fig. 3, illustrates the design concept that uses the back-gate knob to select the desired saturation current level when the DG device is ON, and to select low OFF-state leakage or a quiescent current level for state retention purposes. For instance, the top curve depicts the front-gate current when the back-gate bias is at V_{DD} (1.0V), corresponding to dual-gate operation with high I_{on} for fast mode operation. Notice that the higher I_{OFF} at BG = V_{DD} can be used for data retention. The bottom curve depicts the case when the back-gate bias is at GND, corresponding to single-gate operation with a low I_{OFF} state. The middle curve depicts the case when both gates are tied together. Such features, however, are not available in conventional planar CMOS technologies even though similar well contacts (in bulk) or body contacts (in SOI) work as V_T modulators.

Increased leakage in scaled technologies limits the robustness of dynamic circuits, especially wide OR- and MUX-style dynamic gates commonly used in high-speed designs. Strong keepers are needed for the precharge state or after the completion of evaluation to compensate for leakage and hold the correct state of the dynamic node. Strong keepers, however, cause aggravated contention and speed degradation during evaluation, which is particularly severe at skewed (stronger-PFET weaker-NFET) process corners and low-voltage operating conditions. Previously, a conditional keeper technique was proposed where only a fraction of the keeper strength is turned on at the onset of evaluation phase while the full strength is enabled after a delay time [1]. Alternatively, a programmable keeper technique where the effective keeper width tracked the on-die leakage was proposed to compensate for die-to-die variation [2]. Nevertheless,

employment of additional devices increases the logic gate area as well as the capacitance at the dynamic node. Charge sharing is another concern which causes voltage droop in the dynamic node and degrades the noise margin. A common method to prevent the charge sharing effect consists of charging the intermediate node in a stacked configuration to full rail before evaluation. While the technique is effective, the intermediate node precharge device adds capacitance to that node and increases the circuit area. To address these issues with continued device scaling requires diligent technology circuit co-design efforts.

II. Circuit Design with Double-Gate Devices

Compared with planar CMOS devices, DG devices exhibit smaller subthreshold and gate leakage currents while offering stronger current drive. Independent biasing of the front- and back-gate in double-gate (DG) technologies has been reported to enhance performance and reduce chip area due to the reduction of transistor count to implement a given logic functions [3-4]. Separate gate access allows for simplification of circuit topologies and area compactness, both lead to power and speed improvement in addition to design flexibility. This flexibility is illustrated by using the example of a simple inverter given in tied-gate (Fig. 4 (a)) and independent gate-controlled (Fig. 4(b)) configuration, which correspond to implementation choices for low-leakage/high-drive, and variable drive purposes, respectively. Area compactness is best understood in more complex gates, in an area containing a multitude of logic gates, or directly observed in area reduction due to the simpler equivalent logic topology. For instance, shown in Figs. 5 (a) and (b) are two representations for 4-input NAND gate layout.

In the following sections, keeper schemes utilizing independent front- and back-gate control in DG devices are presented. The proposed schemes realize the conditional keeper function with fewer devices, effectively reducing area and capacitance while achieving improved speed, noise margin, and reliability in dynamic circuits. Also introduced is a method that utilizes the back-gate device of a logic transistor as the precharge device for the intermediate stacked node, to prevent charge sharing, thereby reducing the capacitance and area of the intermediate node precharge device. Subsequently, a static keeper and footer method using the asymmetrical DG devices is described taking advantage of the unique front and back

channel current characteristics. Finally, a detailed case study for analog application of a high frequency voltage controlled oscillator (VCO) design with wide tunable range is presented.

III. Conditional Keepers

Fig. 6 depicts the schematic diagram of a conditional keeper using independently biased symmetric DG PFET. The "slow mode" pin can be either a test mode signal that preserves the dynamic node state during low-frequency debug, or an at-speed delayed clock that turns on the back-gate keeper after a successful evaluation.

For symmetric DG devices, the strengths of the front- and back-gate are equal when only one gate is turned on. When both channels are on (DG mode), the total current in the front- and back-channel increases to more than two times higher, compared with the one-gate-on case due to the ideal subthreshold slope in the DG mode of operation. At lower V_{DD}, the DG mode current improvement becomes larger as the effect of gate-to-gate coupling becomes more significant [5]. Thus, this dynamic circuit technique is viable for voltage scaling, considering the timing, current drive, and device strength requirements. Two alternative circuit configurations are shown in Figs 7 (a) and (b), both of which delay the turn-on of the back-gate keeper device. These schemes utilize a single DG PFET to perform the functions of both weak keeper and strong delayed-on keeper, thus reducing the capacitance and area associated with multiple keeper devices to reduce contention, improve speed, area, noise immunity, and circuit robustness.

The unique features, shown in Fig. 3, of asymmetrical DG device structure can be preferentially utilized in circuit design. When only the back-gate is biased and the front-gate is grounded, the back-channel current is more than one-order-of-magnitude lower than the predominant front-channel current due to the ~1V higher threshold voltage for p+ gate [5]. When both the front- and back-channel are turned on, the front-channel current is enhanced by approximately 2 times at V_{DD}=1V, due to gate-to-gate coupling, compared with the case when only the front-gate is on. In the circuit of Fig. 6 for the asymmetrical DG devices, the front-channel with the off back-gate serves as a weak keeper. The back-gate is turned on to increase the front-channel current only when a strong keeper is desired. Thus, the circuit provides the

keeper function with its strength conditionally modulated by the back-gate. Figs 8 (a) and (b) show the MEDICI [6] simulation results for the fast and slow mode, with heavy and light output load, respectively. A significant slow-down of the evaluate edge in the slow mode operation is observed, thereby demonstrating the performance advantage of the proposed method. The difference between the slow and fast mode operation is larger in the case of light output load because of the more pronounced difference in effective drive current and hence the transitional slews.

IV. Charge Sharing Mitigation

Fig. 9 depicts a scheme, using symmetric DG devices, where the back-gate of logic transistor A1 is used as the precharge device for the intermediate stacked node “int” to prevent charge sharing. The scheme reduces the capacitance and area of the intermediate node pre-charge device, thus effectively circumvents charge sharing and conserves area with the intervention of signal “clock_b”. The insert of Fig. 9 compares the dynamic node “dyn” waveforms, under a severe charge sharing condition during evaluation, with and without the anti-charge sharing back gate device. The use of anti-charge sharing back gate device prevents the collapse of dynamic node voltage and catastrophic logic fault.

V. Static Keepers and Footers

If a dynamic stage uses a static keeper instead of the feedback half latch, the leakage current through the always-on keeper would be unacceptably high for conventional bulk silicon, PD/SOI, or symmetrical DG technologies. In contrast, the asymmetrical DG PFET incorporates the function of two PFETs: the front -gate with a strong front-channel current can be connected to the clock to perform the reset function while the weak back-gate, at a 1/10th - 1/20th drive strength, can be used as a static keeper without excessive leakage current.

Fig. 10 shows a domino stage using asymmetrical DG devices where p1 replaces both the precharge and keeper device. The front gate precharge device of p1 is connected to the clock with only half the gate loading and no performance penalty. The back gate keeper device of p1 is tied to constant (hard wired for

all modes, as shown in Fig. 10) or conditional voltage levels (for higher current in active mode, and low leakage at stand-by to further reduce leakage, Fig. 11). When the front-gate is off during evaluation, the back-gate becomes a keeper. MEDICI simulation results showing well behaved state transitioning are presented in Fig. 12. It is observed that $I_{on(n1)}/I_{on\_strong(p1)}=3.85$; $I_{on\_strong(p1)}/I_{on\_weak(p1)}=14.50$; $I_{on\_weak(p1)}/I_{off(n1)}=1.84x10^4$. The circuit functions with a wide noise margin as shown in two examples of noise event simulations (Fig. 13) for both precharge and evaluate. The static keeper can maintain or restore the desired V_{DD} level. During burn-in and debug mode, there is an additional option of keeping clock high. Thus, the circuit functions as a pseudo-NMOS gate at low frequencies.

Similarly, when designing a footer device, we can exploit the asymmetrical DG device feature: the front-gate with strong coupling to the front-channel determines the on/off state; and the back-gate with weak coupling to the channel controls the strength of the front-channel. When the r front- and back -gate of the footer device are tied to the clock, as depicted in Fig. 10, faster reset and lower leakage are achieved for the on and off state, respectively. Alternatively, the footer back gate can be tied to constant or conditional V_{DD} to achieve clock load reduction, shown in Fig. 11, in vast or dense clock grid systems.

VI. High-Speed Voltage Controlled Oscillators

A. VCO Design

VCO is an important building block for phase locked loops (PLLs) and other frequency synthesizers. Previously, the current-starved inverter-based VCO was proposed to provide a wide tuning range but operated at relatively low frequencies with poor noise rejection due to the very sensitive delay variation with controlled bias [1]. In order to operate at higher frequencies while achieving a wide tuning range, efforts have been made in VCO designs such as the interleaved VCO topology [2] shown in Fig. 14. Well/body bias [3] techniques can also be utilized to widen the high frequency range [4]. Fig. 15 shows an example of this method. However, these approaches have inherent limitations [5].

Consider the interleaved VCO of Fig. 14. The outer inverters of nodes {*pqrst*} form a main five-stage ring oscillator which is assisted by five interleaved three-stage oscillators. For example, the three-

stage oscillator {*pqr*} is interleaved with the main ring. When connected in this fashion, the circuit interpolates between three and five-stage ring to form an equivalent four-stage ring oscillator. The outer inverters are sized to have stronger drive strength in order to achieve high frequency and wide tuning range. These advantages come at the expense of increased contention and, subsequently, stability issues. As illustrated in Fig.14(c), the VCO does not exhibit monotonic behavior as a function of control voltage. Moreover, this phenomenon is difficult to predict, making these oscillators less attractive for wide tuning range applications.

While well/body bias in bulk CMOS or PD/SOI devices can be used to modulate the threshold voltage, the effect is quite limited. Large reverse well/body bias causes exponential increase in the reverse junction leakage including band-to-band tunneling current, while forward well/body bias results in exponential increase in the forward diode leakage [5]. The V_T modulation effect also diminishes with device scaling due to low body factor in scaled, low V_T transistors. Additionally, the distributed RC for well/body contacts limits the viable operating frequency.

B. VCO Design with Asymmetrical Double-Gate Devices

Fig. 15 shows a five-stage asymmetrical double-gate VCO. The front-gates are connected in a ring fashion which forms the main path of the VCO. The NFET back-gates are connected to the control voltage *VC* while the PFET back-gates are connected to the control voltage *VCB*. In typical PLL operations, *VC* and *VCB* are usually adjusted in complementary directions, so that the VCO produces a desired frequency that is in phase with the reference clock. As illustrated in Fig. 2, the ability of asymmetrical double-gate devices to modulate the front-gate V_T is suitable for tuning applications like the VCO.

When the back gates are turned off (*VC* = 0 and *VCB* = *VDD*), the VCO operates at the lowest frequency. When the back gates are fully on (*VC* = *VDD* and *VCB* = *0*), the VCO achieves its highest frequency. The output frequency can be tuned by varying the voltage control signals. Since the back-gate device can modulate the front-gate current by over a factor of 2, the operating frequency for this VCO is expected to exhibit a similar tuning range. Mixed-mode MEDICI simulation results, described in the following section, confirm our expectation. The average propagation delay (τ_{ave}) is defined as the average

of pull-up and pull-down delays, and the oscillation frequency is estimated as $f = 1/(2 \times n \times \tau_{ave})$ where n is the number of stages in the ring. The frequency ratio of (short-channel) double-gate VCO at $VC = VDD$ (and $VCB = 0$) and $VC = 0$ (and $VCB = VDD$) can be expressed as

$$\frac{f_{high}}{f_{low}} \cong \frac{VDD - V_{T(VC=0)} + r \cdot VC}{VDD - V_{T(VC=0)}} \qquad (1)$$

where r is the gate-gate coupling factor [7]. The relative frequency range of double-gate VCO by back-gate bias increases when VDD decreases and $V_{T(VC=0)}$ increases due to the increased gate-gate coupling effects [7].

With the proposed scheme, a VCO can be designed with a minimum number of devices. This leads to better noise immunity, tuning range, power efficiency, and an operating frequency only limited by the gate RC (the same constraint as the rest of the core logic). Additionally, with thinner gate oxide and thinner silicon body film, the gate-to-gate coupling becomes stronger in scaled technologies, thus further improving the frequency and its tuning range.

C. Simulation Results

The double-gate VCO was analyzed using the mixed-mode MEDICI simulator. Nine double-gate inverters are connected in a fashion similar to Fig. 15. *VC* and *VCB* were swept from 0.0-1.0V and 1.0-0.0V, respectively. As the back-gates are turned on, the frequency increases from approximately 12.5GHz to 25GHz. Fig. 16 shows the waveforms of the third, fourth, and fifth stage of the VCO. Fig. 17 illustrates the output frequency of the VCO as the control voltage signals vary.

In comparison, applying the control voltages to the wells of a VCO of the same topology in bulk technology, an inferior operating frequency as well as narrower tuning range is observed as shown in the lower frequency curve of Fig. 17. This is because the threshold voltage change for either NFET or PFET is not sufficient to significantly change the current drive, and hence the delay, of each stage. In addition, the respective range for each control (well) bias in bulk technology is practically limited to less than 400mV in

order to avoid catastrophic junction leakage. In our simulation, as depicted in Fig. 17, *VC* and *VCB* sweeps were limited to 400mV for bulk Si technology, which abruptly cuts short the progression of the lower frequency curve in Fig. 17. Clearly, this limitation further reduces the usefulness of well bias technique. In contrast, the proposed scheme does not suffer junction leakage at any control bias.

Although the double-gate VCO operates at a much higher frequency than the bulk-silicon VCO at the same bias condition, it actually consumes less power, as indicated in Fig.18. The reason is, in bulk silicon, the increase of the forward well bias increases junction capacitance tremendously, causing higher dynamic power consumption.

Notice that connecting the front-gates f to form the main ring and the back-gates to the control voltage signals is preferred. Alternate topologies, such as swapping the front- and back-gate connections, result in un-sustainable oscillations due to reduced gain. The reduction in gain stems from the difference in the work functions of the NFET/PFET device's front- and back-gates. Furthermore, the front gates would be very leaky when controlled voltages are applied, leading to increased contention since the devices are always on even in the off state. Therefore, the proposed scheme is only applicable to back-gate biasing.

Fig. 19 compares the different outcomes of the two topologies. It shows the waveforms of the third stage of the proposed VCO and the same VCO with the connections swapped. *VC* and *VCB* are swept from t = 0.0ns to 0.5ns. The oscillation is then allowed to settle until t = 2.0ns. For the VCO that has swapped connections, the amplitude of oscillation decreases and eventually vanishes as both NFET and PFET front-gate devices are turned on, thereby, shorting the supply rail to ground. On the other hand, the back gate-biased double-gate VCO continues to ramp up in frequency. The proposed VCO also exhibits a typical characteristic of a high speed oscillator whose magnitude slightly decreases at the upper end of the frequency spectrum. This phenomenon is attributed to the current from the off device that must be sourced or sunk by the active device. When the VCO output is pulling low, the additional current of the PFET load prevents the NFET form pulling completely low. Based on our study, the back-gate bias controlled VCO fully utilizes the asymmetrical double-gate device characteristics to achieve wide/high frequency range and

efficient power without extra device/layout penalty, process complexity, and problem for latch-up and noise.

VII. Conclusion

In summary, we have presented independent gate biasing design techniques, which take advantages of the V_T/drain current modulation properties, layout compactness, and circuit topological flexibility intrinsic with symmetric and asymmetric DG devices. We discussed topics covering conditional keeper design in dynamic circuits for speed improvement while maintaining noise margin, charge sharing prevention to enhance functionality robustness, and means to reduce clock loads, therefore power, in large and dense clock grid designs. A case study of analog application using voltage controlled oscillator design is also presented. Performance benefit, noise immunity, area and power efficiency can be simultaneously achieved when the distinctive technology features offered in DG devices are judiciously utilized.

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Figure Captions

Fig. 1 Double-gate device cross sectional diagrams (L_{eff} = 25 nm, t_{oxf} = t_{oxb} = 1 nm, t_{Si} = 10 nm): (a) symmetrical double-gate NFET, (b) asymmetrical double-gate NFET. For PFET, the front gate is p^+-poly and the back gate is n^+-poly.

Fig. 2 Front-gate V_T versus back gate bias for asymmetrical and symmetrical double-gate devices. The asymmetrical double-gate device shows strong V_T modulation while the symmetrical double-gate device shows relative constant characteristics over a wide back gate bias range

Fig. 3 Design concept of independent-gate biasing scheme. MEDICI-predicted drain current versus front-gate voltage for asymmetrical DG NFET for three different back-gate bias conditions. Gate electrodes can be connected flexibly to meet the drive strength, leakage reduction, or data retention requirements.

Fig. 4 A CMOS inverter with (a) tied-gate, and (b) independent gate-controlled configuration.

Fig. 5 add nand4 layout here

Fig. 6 Conditional keeper using independently controlled front- and back-gate double-gate PFET. The "slow mode" pin can be a test mode control signal during low-frequency debug, or an at-speed delayed clock.

Fig. 7 Two alternative conditional keeper topologies using a DG PFET

Fig. 8 MEDICI simulation results for DG conditional keeper: (a) heavily loaded output: clock-up to dyn-down = 55 ps (fast mode), 70 ps (slow mode), and clock-up to output-up = 123 ps (fast mode), 130 ps (slow mode), and (b) lightly loaded output: clock-up to output-up = 83 ps (fast mode), 100 ps (slow mode).

Fig. 9 Schematic diagram showing the precharge of internal stacked node "int" using back- gate of the logic transistor A1. The insert shows the well behaved and collapsed dynamic node waveforms with and without the intervention of the back gate anti-charge sharing device, respectively.

Fig. 10 Schematic diagram for a shared precharge/keeper implementation using asymmetric DG devices, where the front-gate of p1 is the precharge device and back-gate of p1 is the weak always-on static keeper

Fig. 11 Precharge/keeper device back gate control for leakage power and/or clock load reduction. The common node p1b is at ground and V_{DD} for active and standby mode, respectively. The common node n2b is at V_{DD} and ground for the active and standby mode, respectively.

Fig. 12 MEDICI results showing the waveforms for data, clock, dyn, and output nodes for two precharge/keeper device (p1) widths of 0.6 and 0.8μm. Data and clock arrival times are assumed to be perfectly aligned in simulation.

Fig. 13 Observation of the dynamic node "dyn" for noise rejection behavior for the circuit of Fig. 10 during the (a) precharge and (b) evaluate interval, respectively. Node "dyn" recovers to V_{DD} in both cases in the presence of the precharge/static keeper device.

Fig. 14 Schematic diagram of (a) an interleaved VCO [2] and (b) a VCO utilizing well/body bias, and (c) frequency versus control voltage for an interleaved VCO

Fig. 15 Schematic diagram of a back-gate bias controlled asymmetrical double-gate VCO

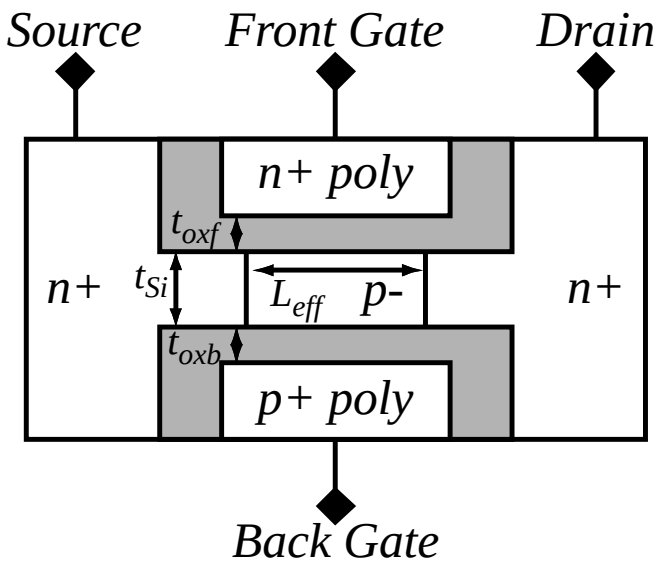
Fig. 16 Waveforms of the third, fourth, and fifth stage of the VCO utilizing bulk silicon well bias and asymmetrical double-gate back-gate bias along with their associated control voltages *VC* and *VCB*

Fig. 17 Frequency range of the well-biased bulk silicon VCO and back-gate biased asymmetrical double-gate VCO

Fig. 18 Switching power of well-biased bulk silicon VCO and back-gate biased asymmetrical double-gate VCO

Fig. 19 The upper graph shows the control voltage timing. The lower graph shows the waveforms of the third stage of DG VCO. The topology with swapped connections does not sustain oscillation.

Fig. 1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Front Gate
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n+
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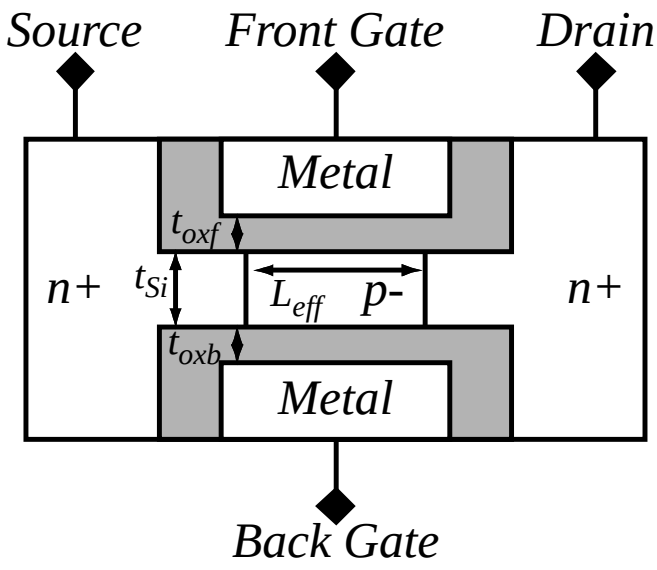
p+ poly
Back Gate

(a)


Source
Front Gate
Drain
Metal
t_{oxf}
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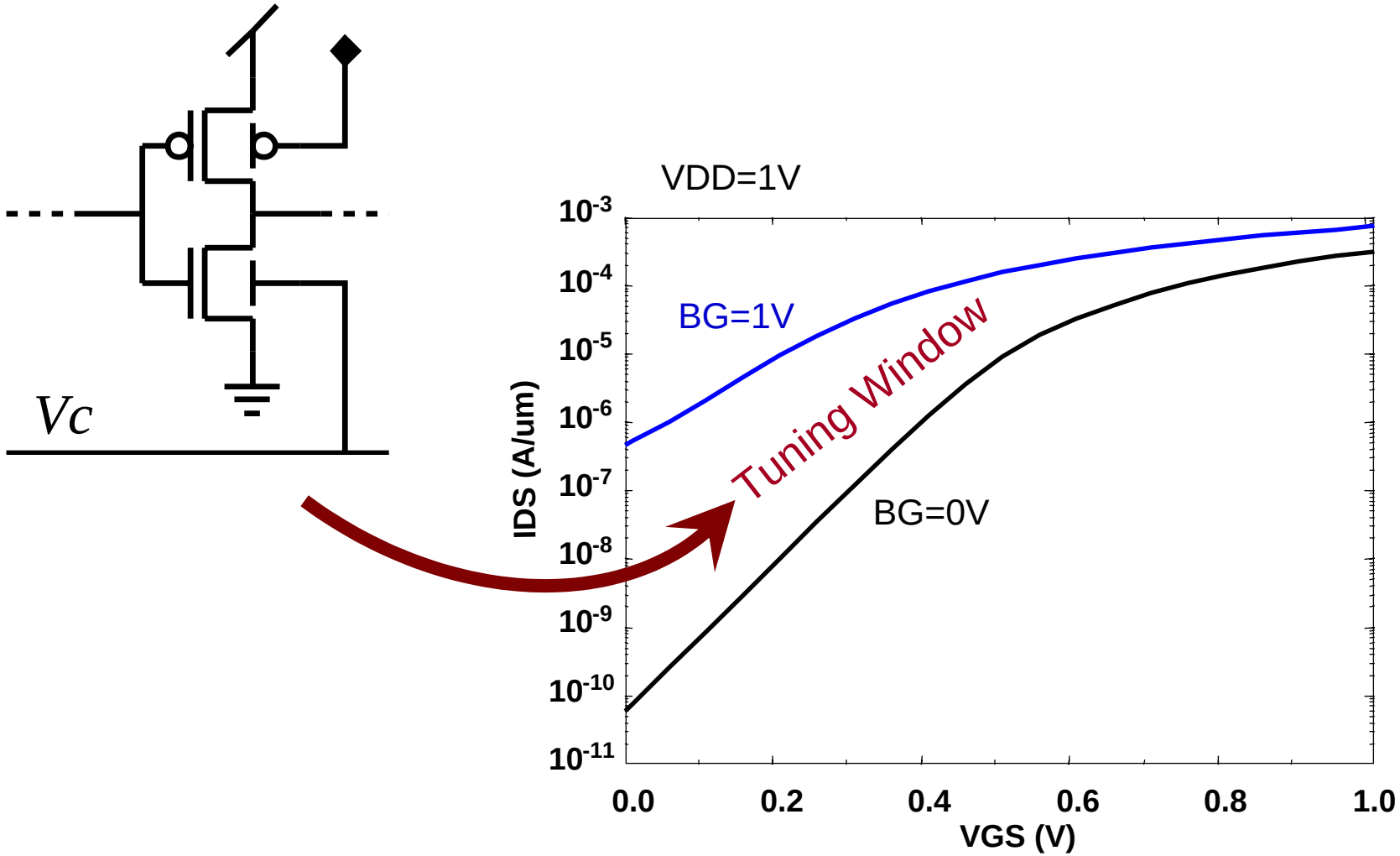
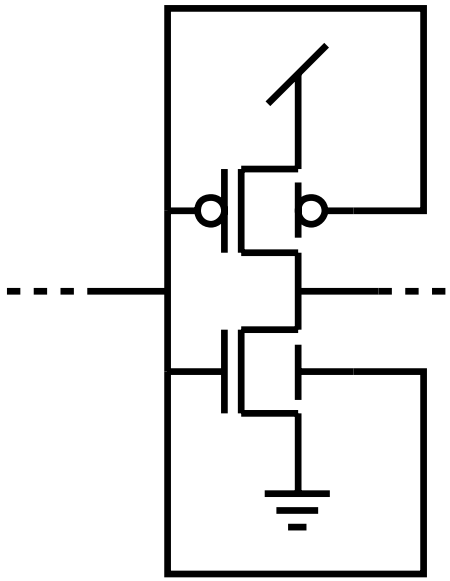
p-
n+
t_{oxb}
Metal
Back Gate

(b)

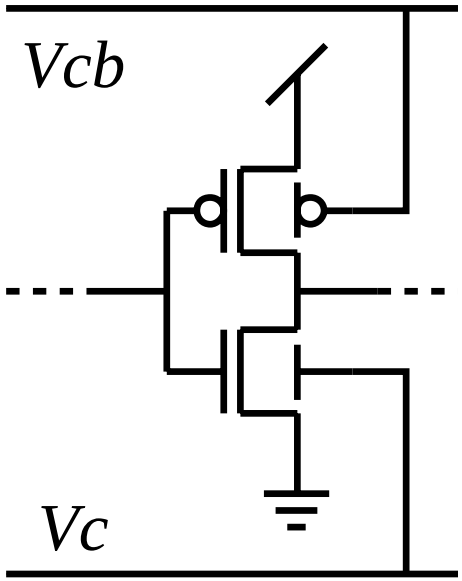
Fig. 2


Vc
VDD=1V
BG=1V
Tuning Window
BG=0V
IDS (A/um)
10-3
10-4
10-5
10-6
10-7
10-8
10-9
10-10
10-11
0.0
0.2
0.4
0.6
0.8
1.0
VGS (V)

Inverter Schematic



Tied-gate configuration



Independent gate-controlled configuration

Fig. 3

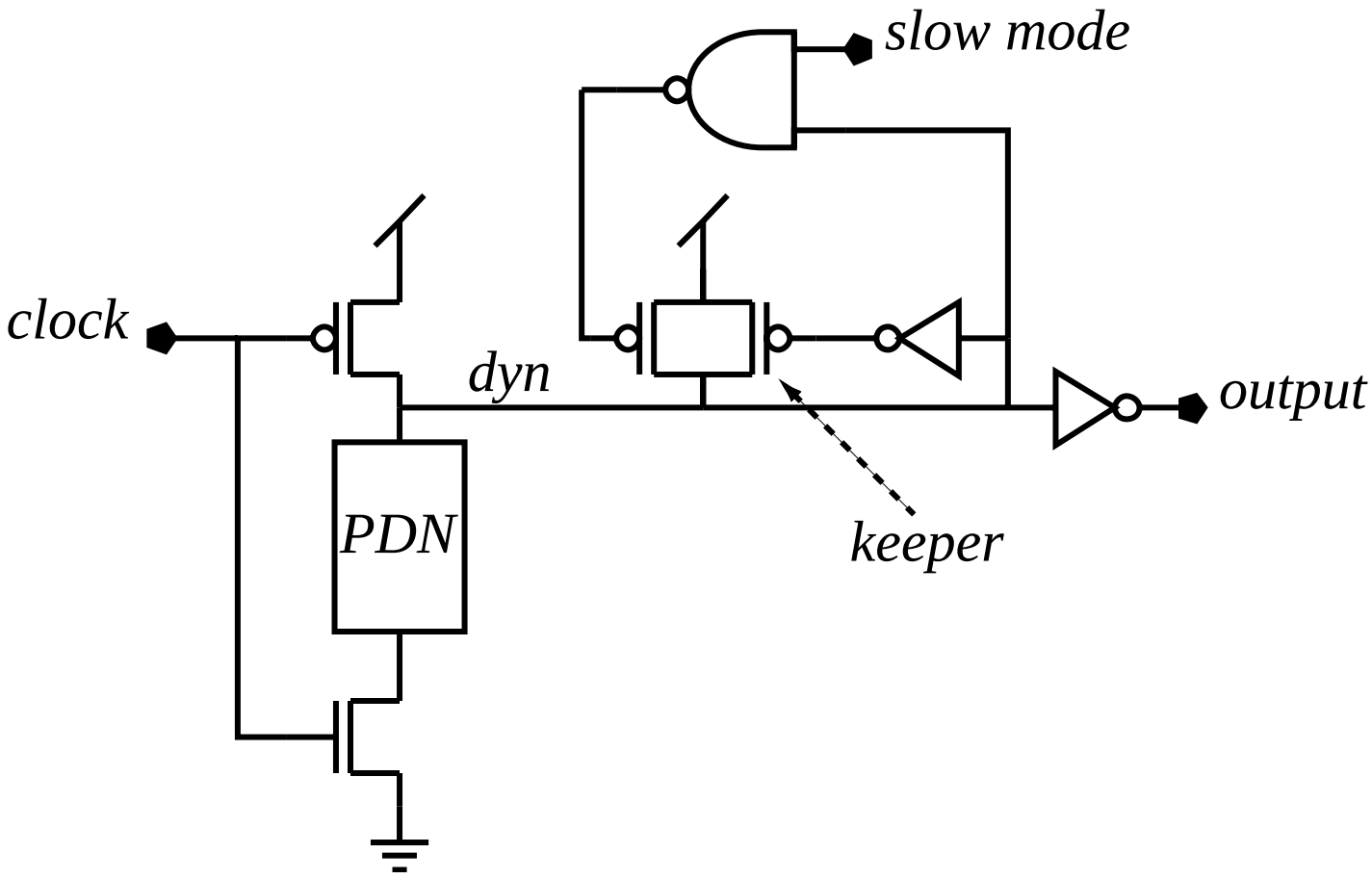


Fig. 4(a)

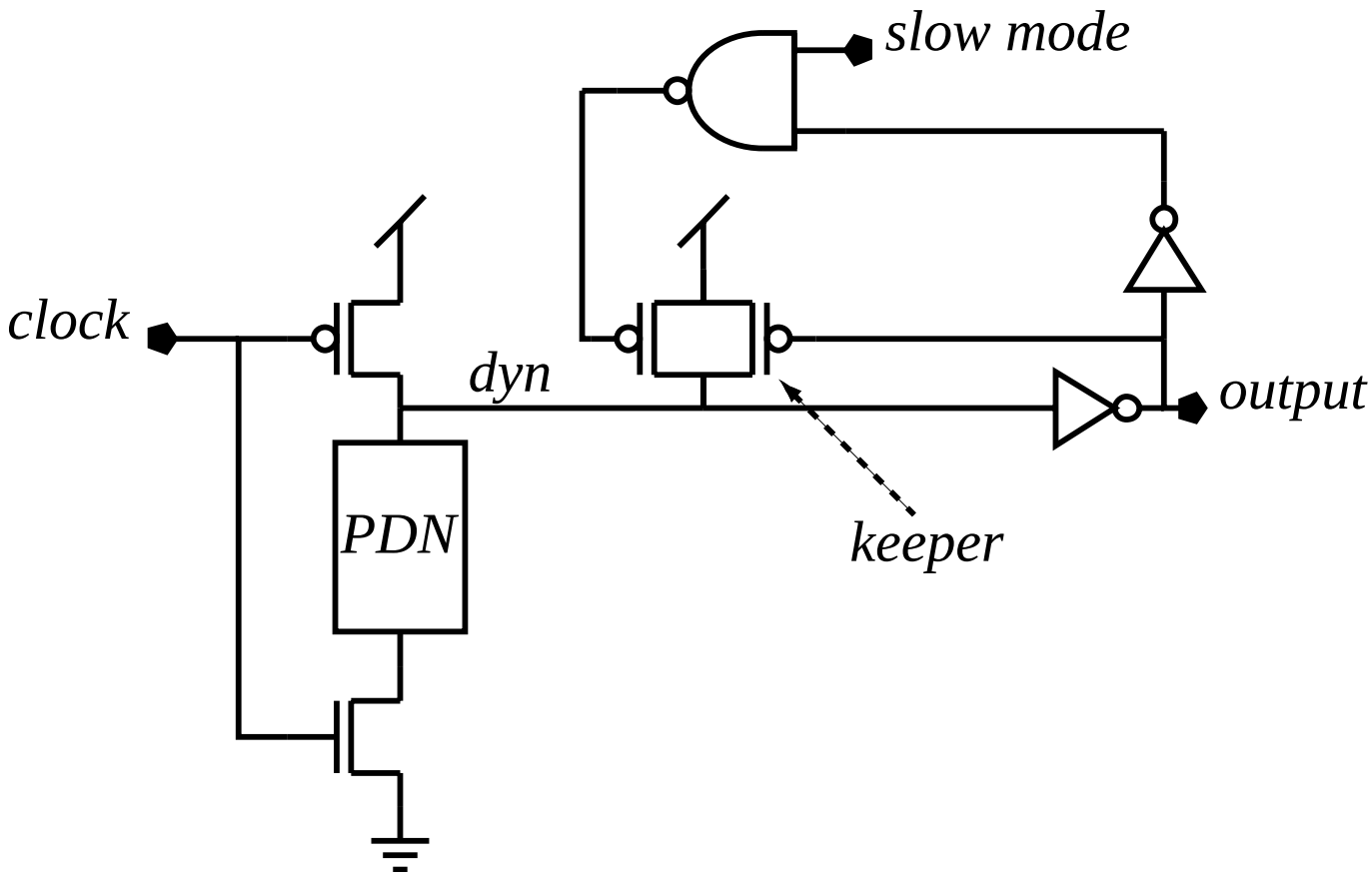


Fig. 4(b)

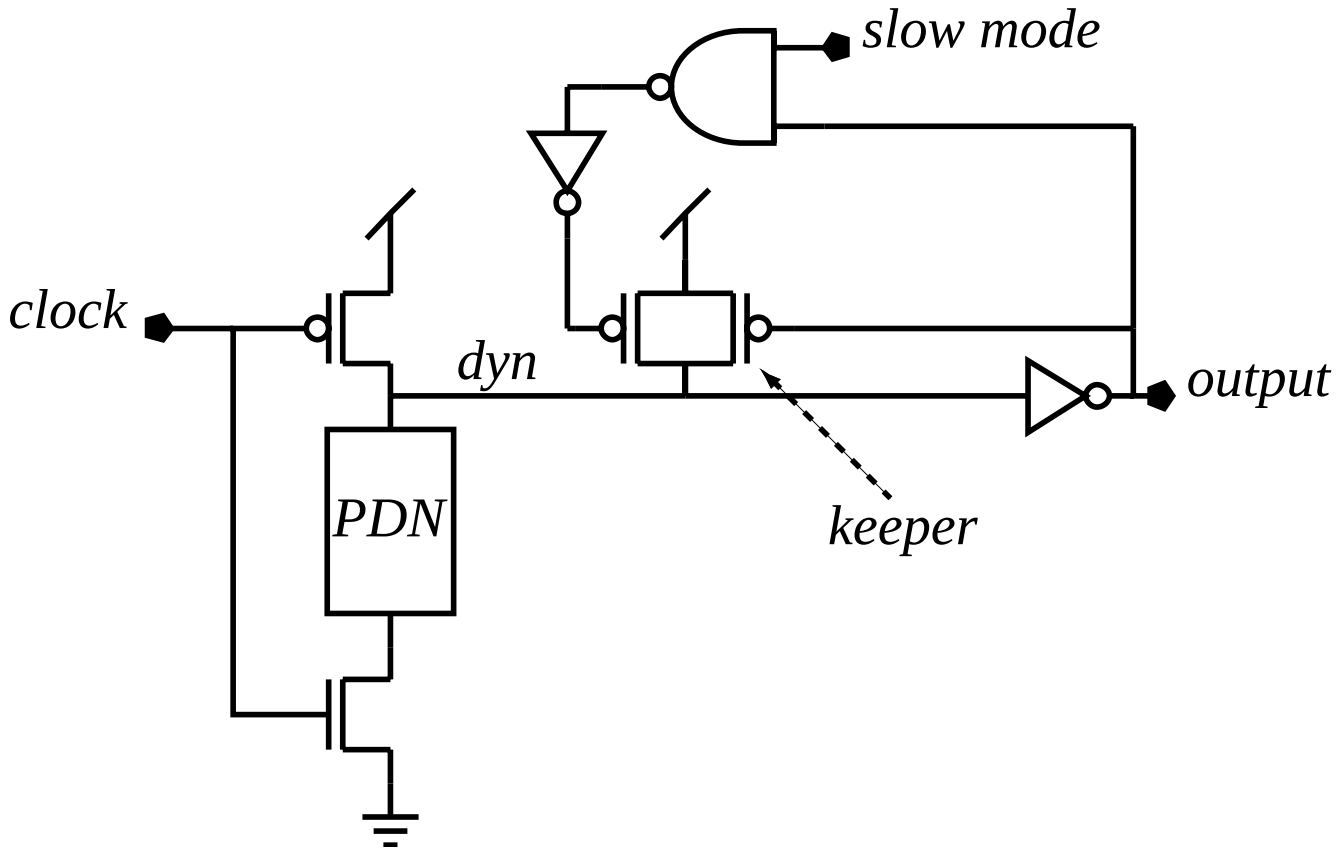


Fig. 5

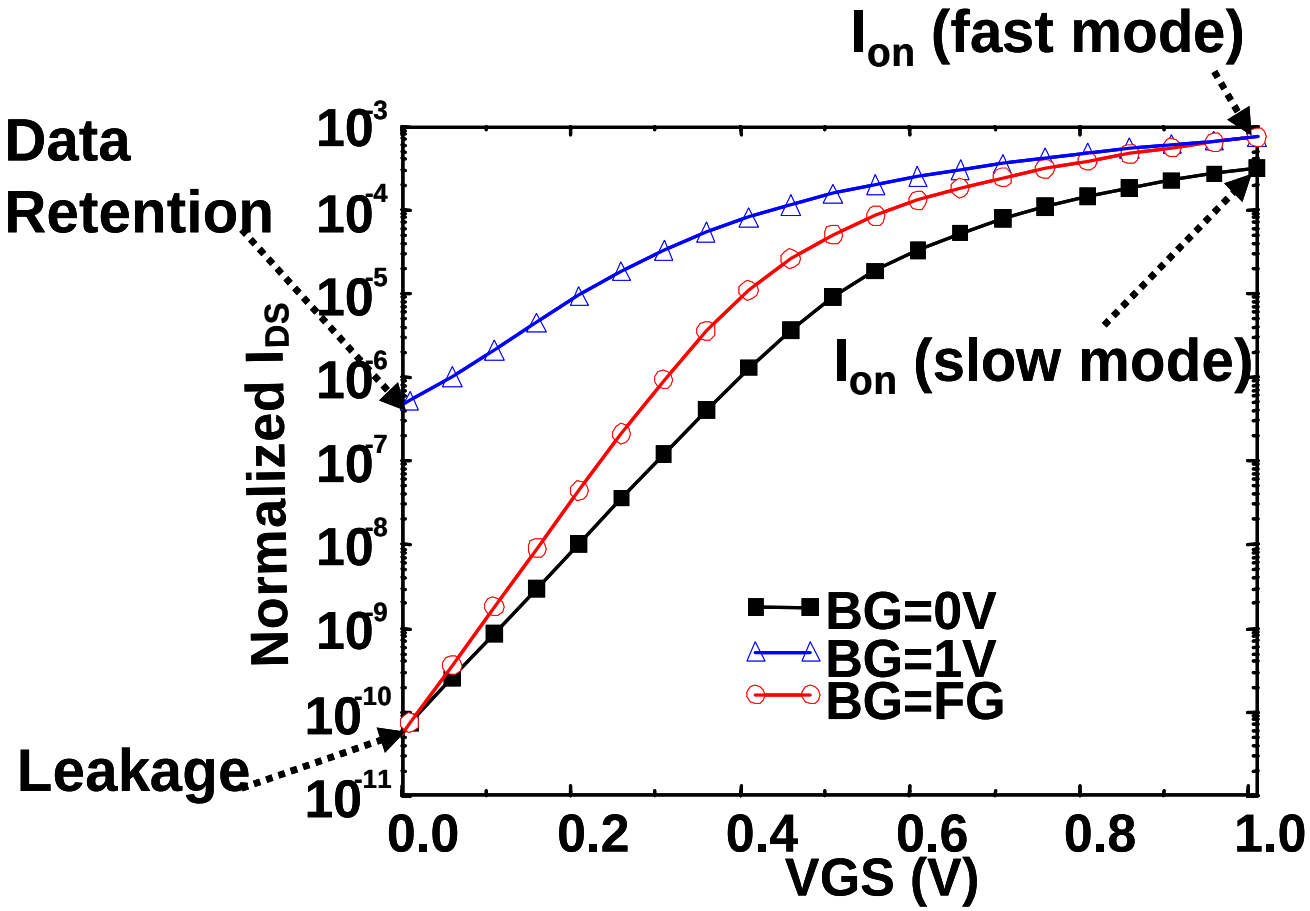

Ion (fast mode)
Data Retention
Ion (slow mode)
Leakage
Normalized IDS
10^3
10^4
10^5
10^6
10^7
10^8
10^9
10^10
10^11
0.0
0.2
0.4
0.6
0.8
1.0
VGS (V)
BG=0V
BG=1V
BG=FG

Fig. 8

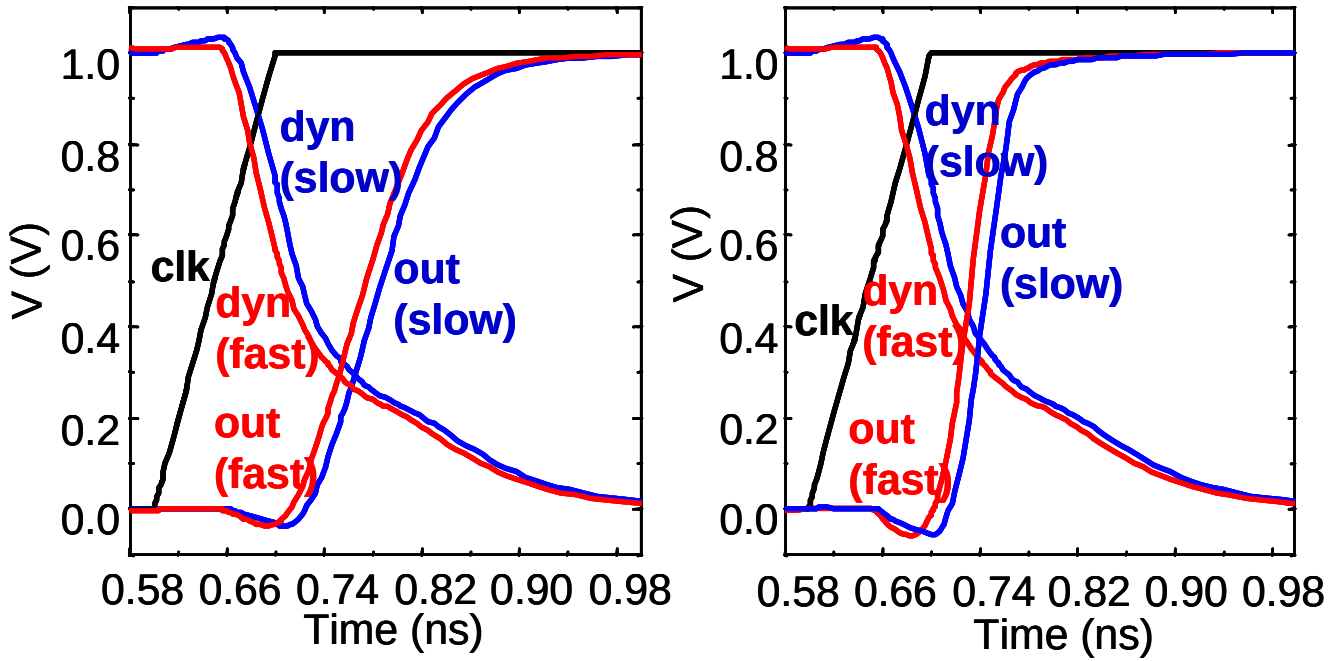

1.0
0.8
0.6
0.4
0.2
0.0
V (V)
clk
dyn
(slow)
dyn
(fast)
out
(slow)
out
(fast)
0.58 0.66 0.74 0.82 0.90 0.98
Time (ns)
(a)
1.0
0.8
0.6
0.4
0.2
0.0
V (V)
clk
dyn
(slow)
out
(slow)
dyn
(fast)
out
(fast)
0.58 0.66 0.74 0.82 0.90 0.98
Time (ns)
(b)

Fig. 10

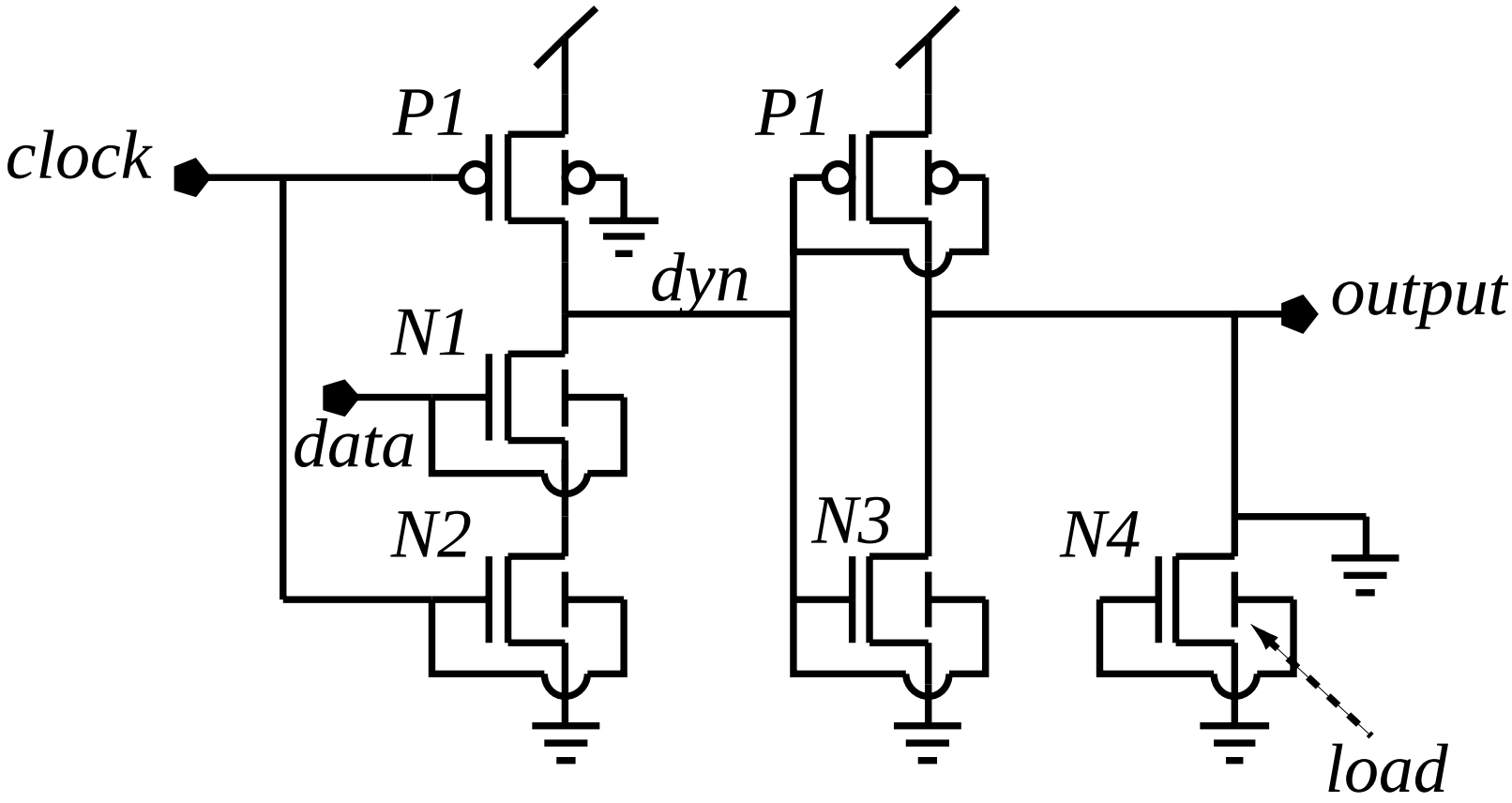


Fig. 11

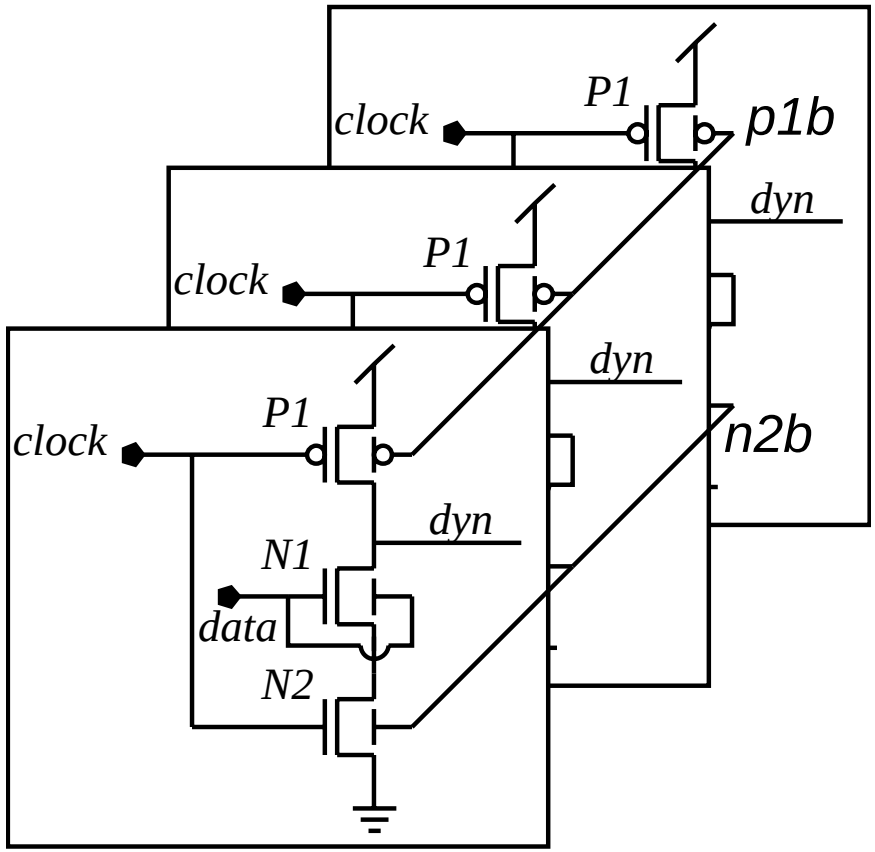


Fig. 12

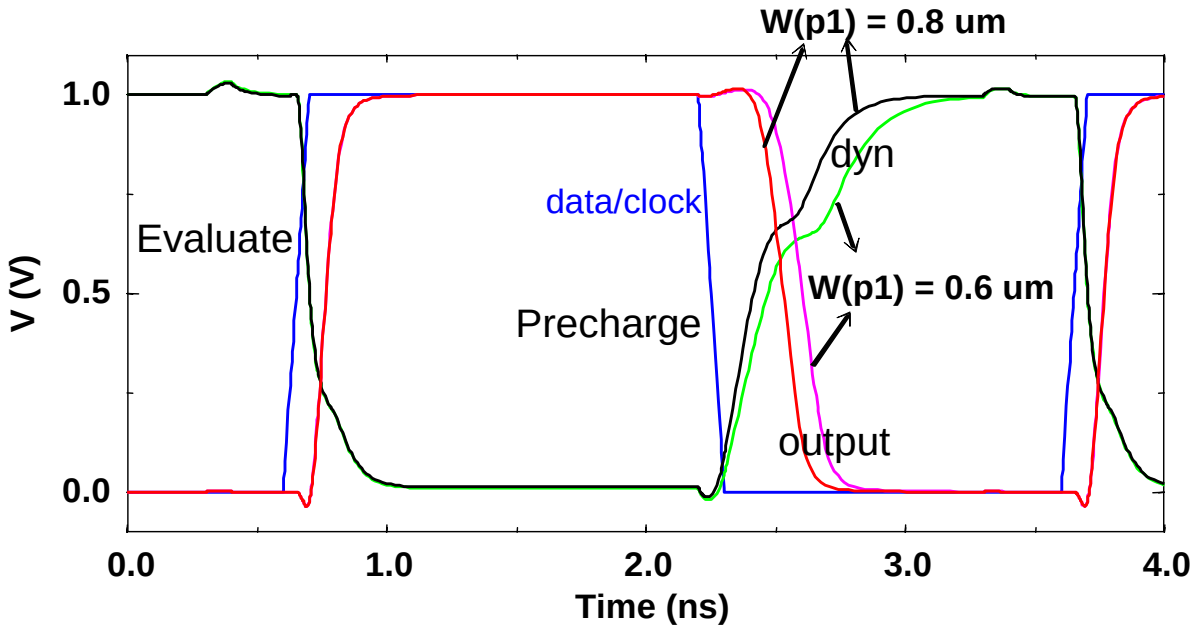

W(p1) = 0.8 um
1.0
0.5
0.0
V (V)
Evaluate
data/clock
dyn
W(p1) = 0.6 um
Precharge
output
0.0
1.0
2.0
3.0
4.0
Time (ns)

Fig. 13

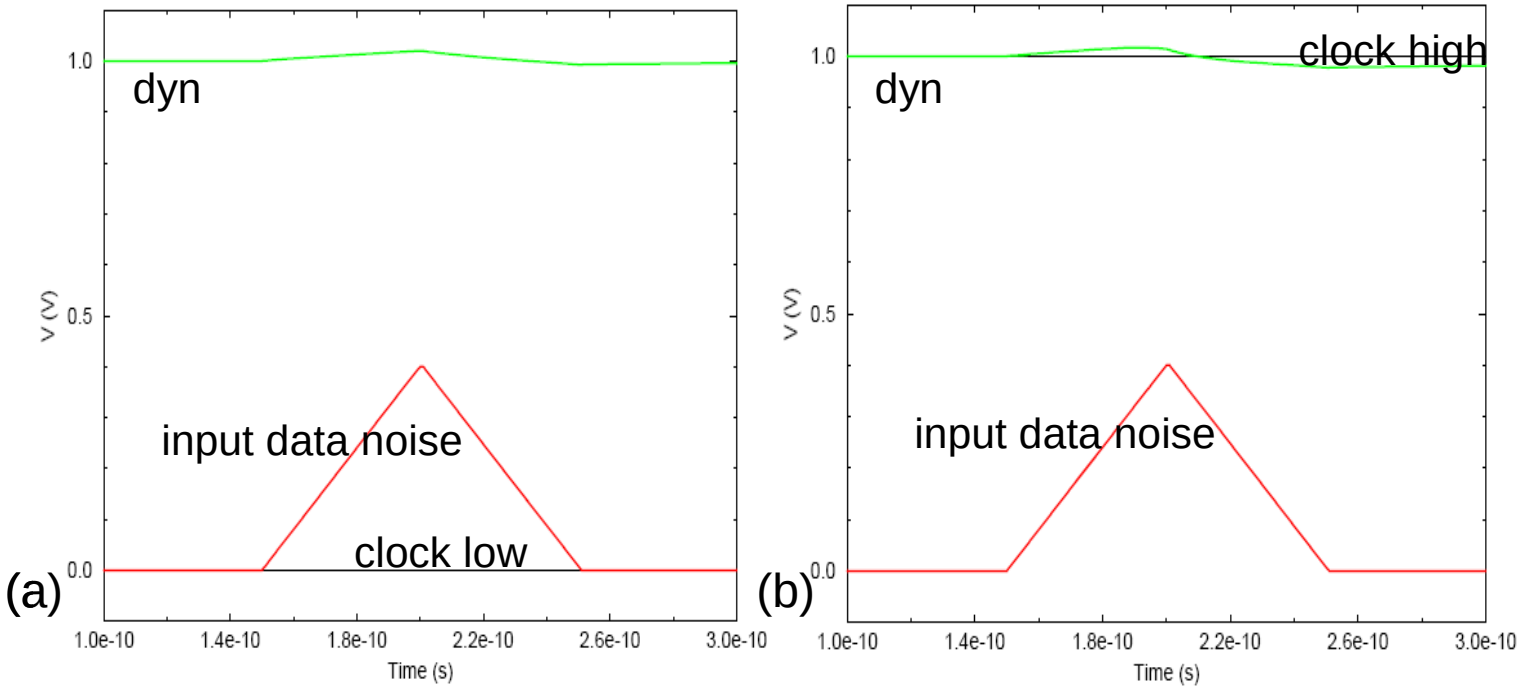

(a)
1.0
0.5
0.0
V (V)
dyn
input data noise
clock low
1.0e-10
1.4e-10
1.8e-10
2.2e-10
2.6e-10
3.0e-10
Time (s)
(b)
1.0
0.5
0.0
V (V)
clock high
dyn
input data noise
1.0e-10
1.4e-10
1.8e-10
2.2e-10
2.6e-10
3.0e-10
Time (s)

Fig. 14(a)

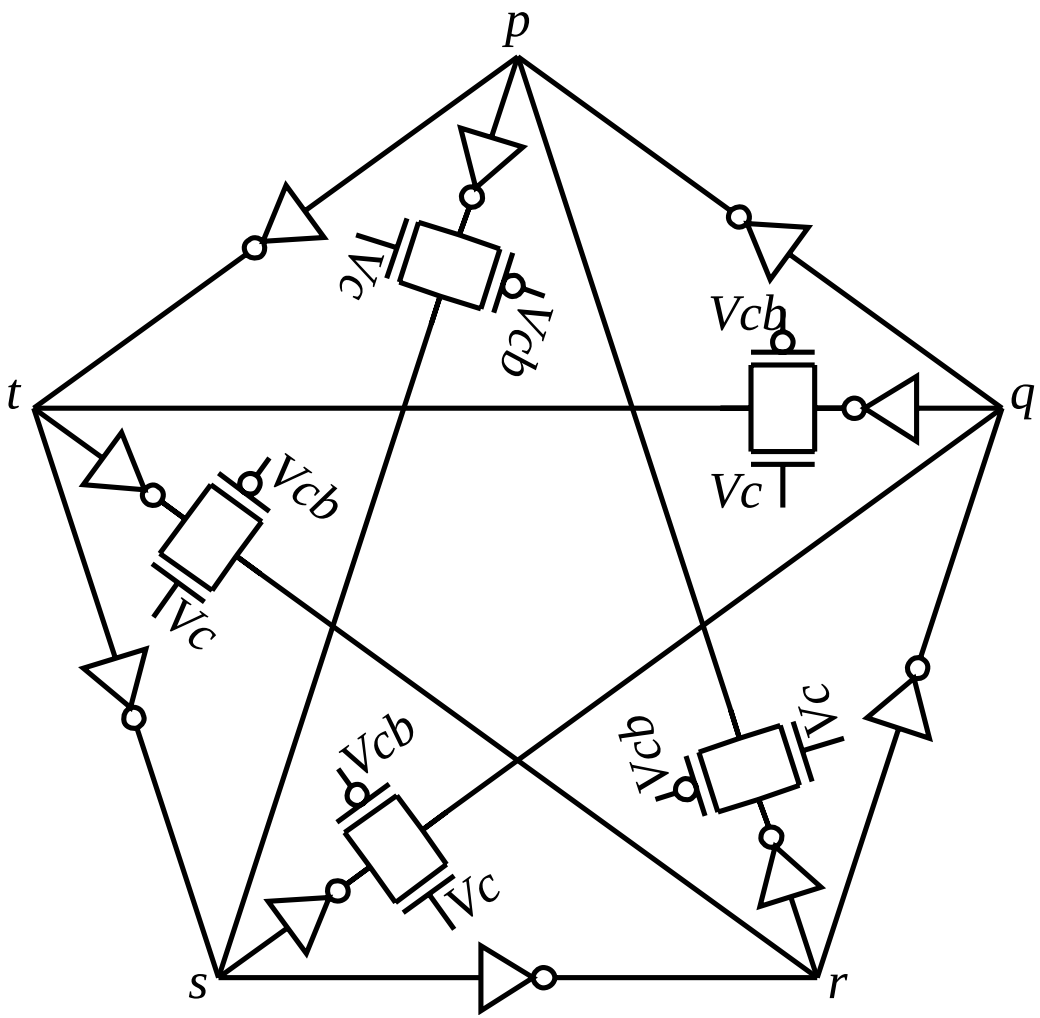


Fig. 14(b)

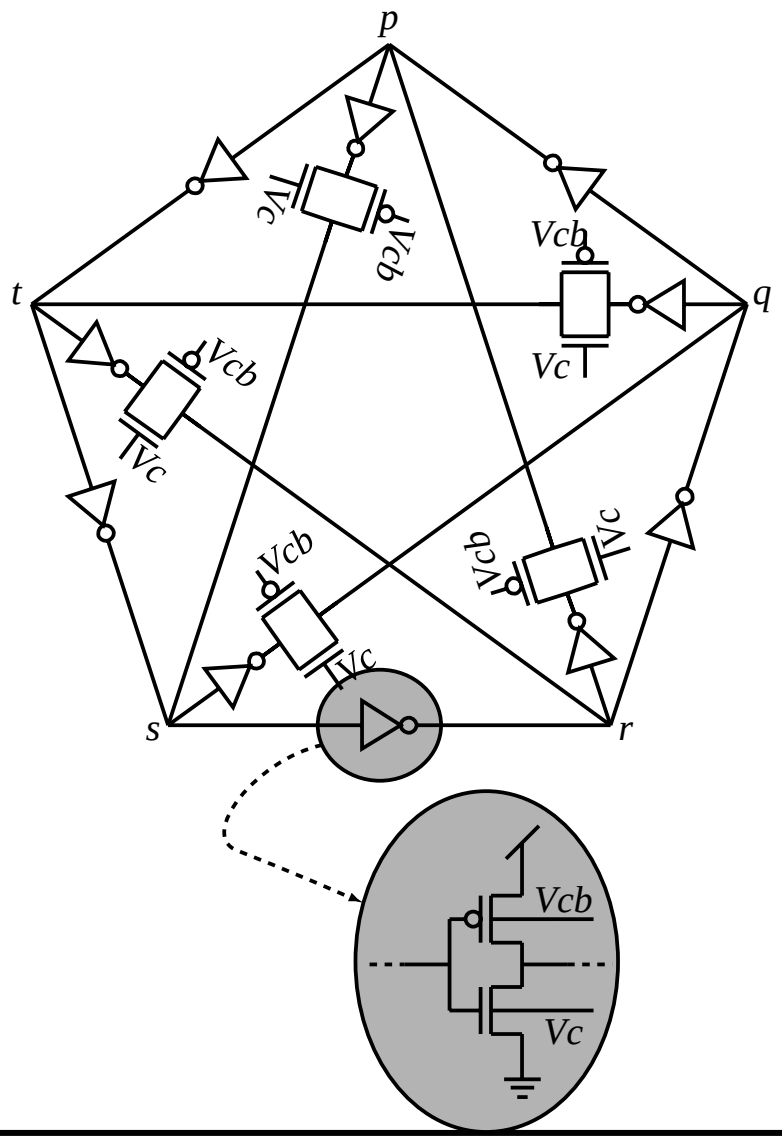


Fig. 14(c)

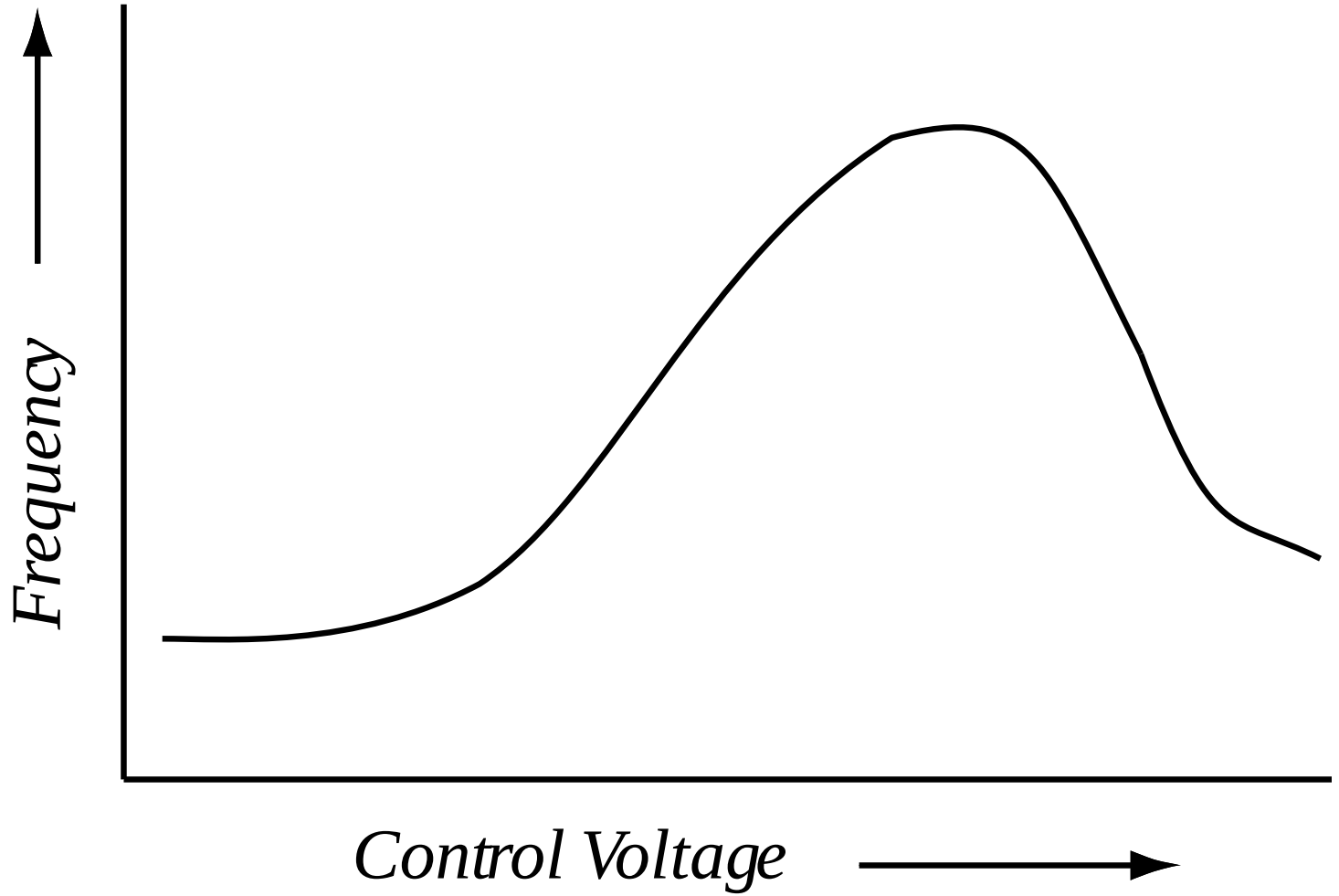


Fig. 15

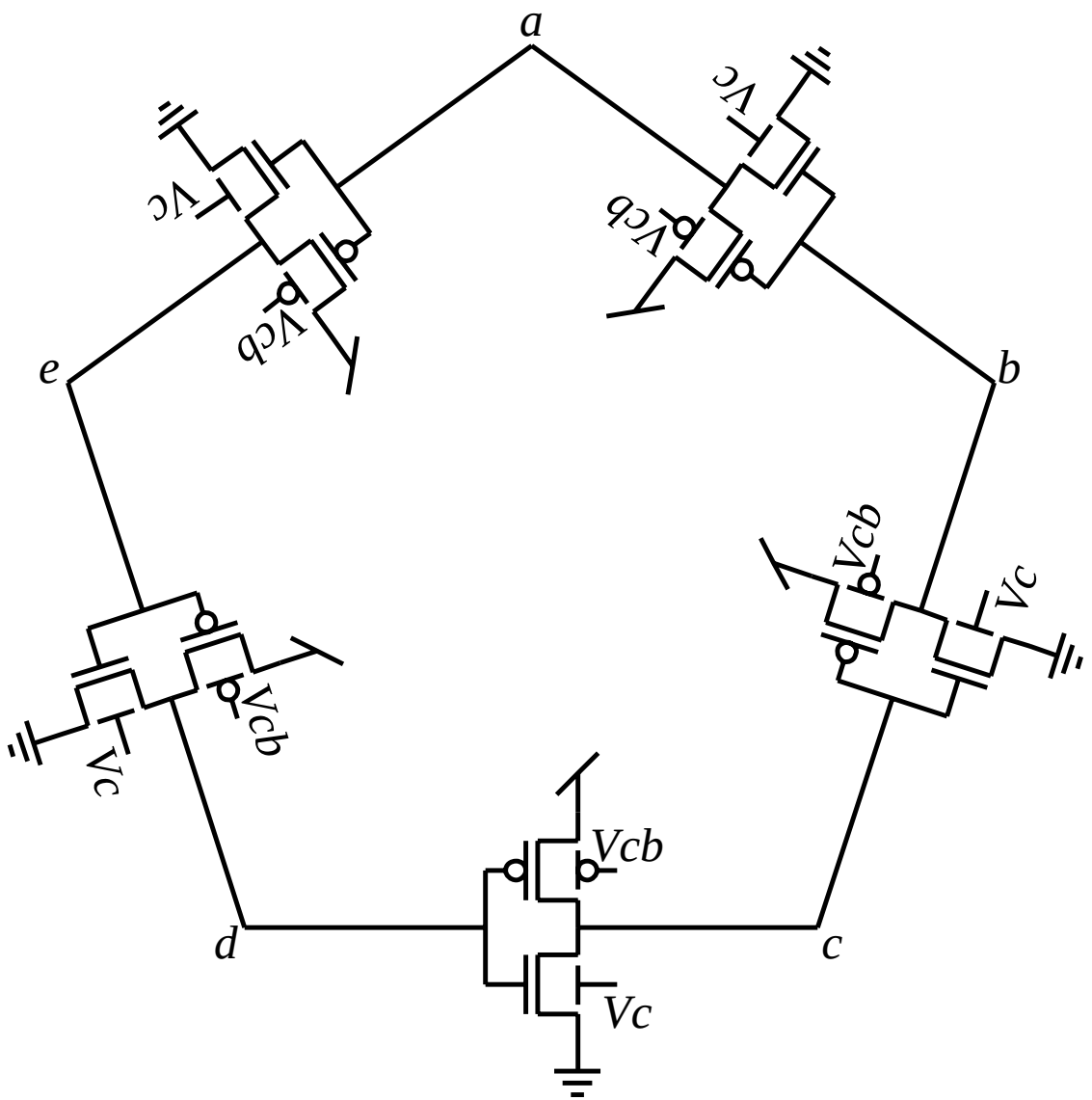


Fig. 16

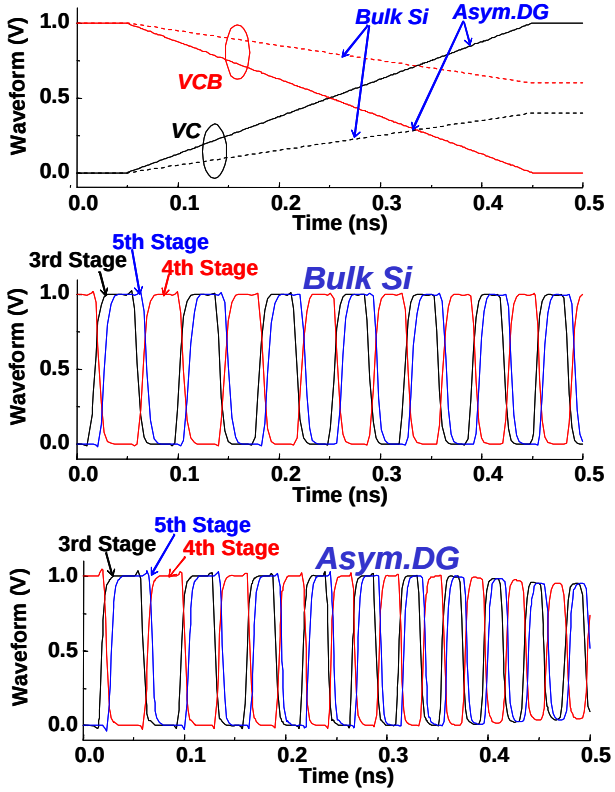

Bulk Si
Asym.DG
VCB
VC
Waveform (V)
1.0
0.5
0.0
0.0
0.1
0.2
0.3
0.4
0.5
Time (ns)
5th Stage
3rd Stage
4th Stage
Bulk Si
Asym.DG

Fig. 17

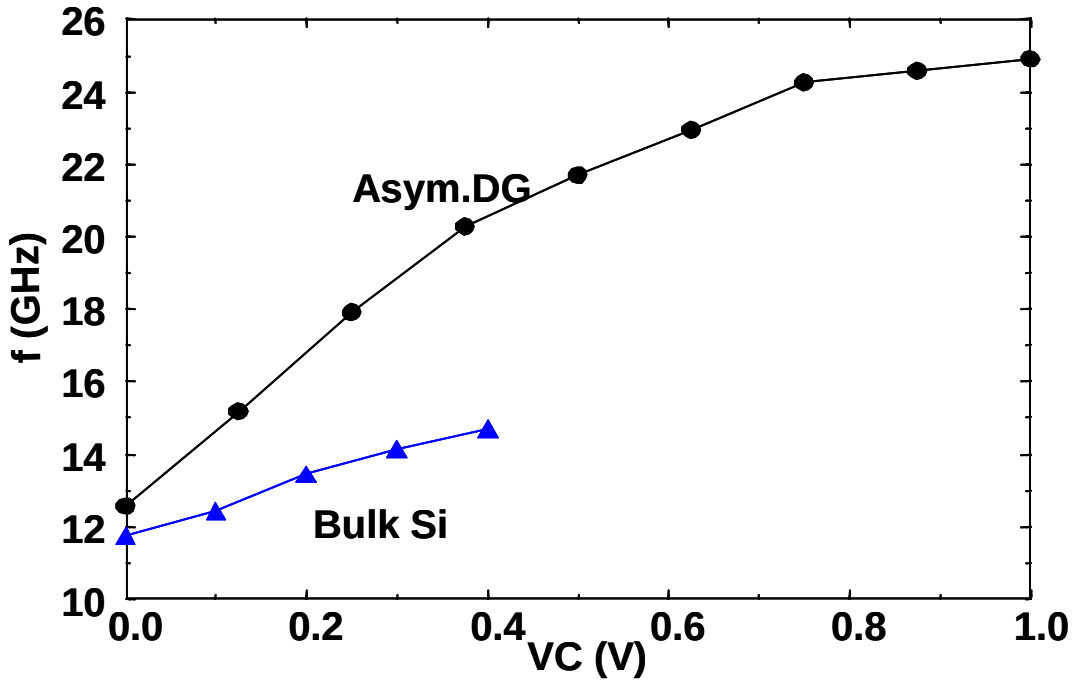


Fig. 18

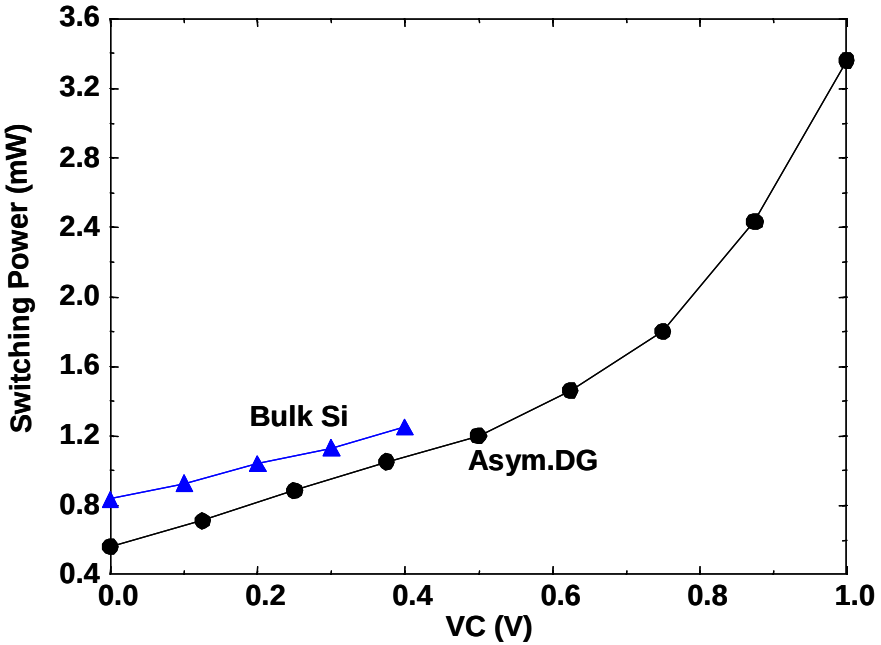
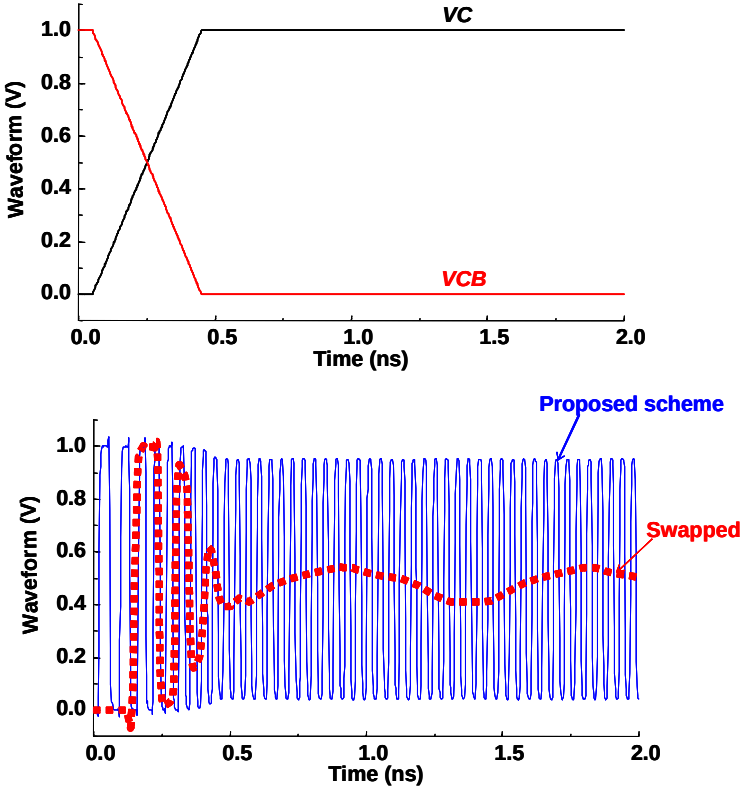

Switching Power (mW)
3.6
3.2
2.8
2.4
2.0
1.6
1.2
0.8
0.4
0.0
0.2
0.4
0.6
0.8
1.0
VC (V)
Bulk Si
Asym.DG

Fig. 19


VC
VCB
Waveform (V)
Time (ns)
1.0
0.8
0.6
0.4
0.2
0.0
0.0
0.5
1.0
1.5
2.0
Proposed scheme
Swapped