RC24325 (W0708-007) August 1, 2007
Materials Science

IBM Research Report

Material and Mobility Characteristics of Ultra-thin (110) Compressively-Strained SiGe pMOSFETs

K. K. Chan, M. Yang, K. Rim, N. Klymko, J. Ott, D. Canaperi, A. W. Topol, E. Sikorski, B. To, D. C. Boyd*, W. Price, J. Newbury, K. W. Guarini, M. Ieong*
IBM Research Division
Thomas J. Watson Research Center
P.O. Box 218
Yorktown Heights, NY 10598

*IBM Microelectronic Division
Hopewell Junction, NY 12533

Research Division
Almaden - Austin - Beijing - Haifa - India - T. J. Watson - Tokyo - Zurich

Material and Mobility Characteristics of Ultra-thin (110) Compressively-Strained SiGe pMOSFETs

K. K. Chan, M. Yang, K. Rim, N. Klymko, J. Ott, D. Canaperi, A. W. Topol,
E. Sikorski, B. To, D. C. Boyd,[1] W. Price, J. Newbury, K. W. Guarini, and M. Ieong,[1]

IBM Semiconductor Research and Development Center (SRDC)
Research Division, T. J. Watson Research Center, Yorktown Heights, NY 10598
[1] Microelectronic Division, Hopewell Junction, NY 12533; Phone: 914-945-3166; email : kkchan@us.ibm.com

Abstract

We report, for the first time, pMOSFETs fabricated on compressively-strained SiGe (110), combining the effects of both lower effective mass in (110) crystal orientation and biaxial strain-induced hole mobility enhancement. This abstract describes an extensive material characteristics study of SiGe growth on Si (110), and the hole mobility in pMOSFETs fabricated on (110) SiGe/Si hetero-layer, which is ~180% and ~10% higher than the reference mobility in (100) and (110) Si pMOSFETs respectively.

Introduction

The anisotropic nature of the electron and hole masses in silicon leads to vastly different carrier transport properties in MOSFETs with different silicon channel crystal orientation. Electron mobility is the highest on the conventional Si (100) surface, while hole mobility is the highest on the (110) surface (almost 2x higher than on the Si (100) surface [1]). Hybrid substrates composed of multiple surface orientations have been demonstrated—nFETs on Si (100) and pFETs on (110)—yielding pFET drive current that is 150% higher than the (100) devices [2]. Carrier mobility enhancement is also possible by introducing strain into the silicon channel. Electron mobility enhancement of 2x has been demonstrated in biaxial tensile-strained Si (100) on a relaxed silicon germanium (SiGe) buffer layer [3]. High hole mobility in compressively strained SiGe grown on (100) Si surface is well known ([4] for example). Recent reports have also demonstrated that uniaxial compressive stress enhances hole mobility significantly [5].

In order to maximize the hole carrier mobility and pMOSFET device performance, we propose applying biaxial compressive strain on the (110) surface orientation. In this paper, we report for the first time the material characteristics, device fabrication process, and mobility behavior of compressively-strained (110) surface SiGe p-channel MOSFETs and demonstrate that the hole mobility is ~10% and ~180% higher than (110) Si and (100) Si, respectively.

Material Properties

We performed an extensive material study of epitaxial SiGe on Si (110). We identified proper growth conditions, analyzed critical thickness and relaxation behavior, and measured the material thermal stability. Epitaxial SiGe was grown on Si (110) using chemical vapor deposition, followed by in situ formation of a thin Si cap. An AFM image of a thin (18 nm) SiGe 22% layer with a 5 nm Si cap on Si (110) shows the RMS surface roughness is less than 0.15nm (Fig. 1). A cross-sectional TEM of this same structure shows good crystalline quality of the layers and confirms the proper SiGe and Si thicknesses (Fig. 2). We characterized the material strain by UV Raman and detail here the relaxation behavior of a SiGe (110) film (Fig. 3). SiGe (22%) begins to relax for a much thinner film on Si (110) (~30 nm) than on Si (100) (~200 nm) (Fig. 4). Thickness-dependence of strain relaxation of SiGe grown on (110) Si is summarized in Fig. 5.

The thermal stability of this material is critical for device integration. Fig. 6 shows that the Raman spectra peaks maintain their shift in relation to the unannealed pseudomorphic SiGe (110) reference peak, indicating that the strained state of the SiGe is retained during thermal cycling up to 400 sec at 1000C. Both AFM and cross-sectional TEM images show that there is no defect formation or surface roughening to the 22% SiGe (110) film during this thermal cycling (Fig. 7,8).

Device Fabrication & Characterization

The starting substrate for pMOSFET device fabrication consisted of a 5 nm Si cap on 18 nm thick SiGe(22%) on Si (110). As the control device, we also fabricated devices on bulk Si (100) using identical process conditions. A conventional bulk device fabrication flow was adopted. The gate stack consisted of a 25A N_2O oxide and a p+ doped polysilicon gate. Most of the 5 nm-thick Si cap is consumed during the various cleaning and oxidation steps, as confirmed by TEM imaging of the final device structure (Fig. 9). A dual nitride spacer process was used, where extension and halo implants were performed after the first thin (8nm) spacer, and deep source/drain implants were performed after the second thick (54nm) spacer. Dopants were activated with a 1000C/5sec RTA. $CoSi_2$ was used as silicide contacts, and the fabrication process was completed with W plug and a single Cu metallization layer.

We measured electrical device characteristics and extracted channel carrier mobility. The thermal gate oxide was thicker on the SiGe (110) sample compared to the Si (100) control, as expected from difference in orientation-dependent oxidation rates. Good FET functionality is observed in the measured *I-V* characteristics (Fig. 10). This is, to our knowledge, the first demonstration of functional p-MOSFETs fabricated on strained (110) SiGe layer. After correcting for the gate oxide thickness difference, we find up to 180% higher hole mobility in compressively-strained SiGe (110) devices compared to the Si (100) control devices. Although the characteristics of the gate dielectric were non-ideal, as noted in the roll-off of mobility at low carrier concentration, the mobility is ~10% higher than the previously reported Si (110) PFET mobility value (Fig 11) at high carrier density. This may be the first experimental evidence that compressive strain enhances hole mobility of (110) SiGe channel.

Summary

We describe, for the first time, the presudomorphic-relaxation characteristics and the thermal stability for compressively-strained SiGe(110). The demonstrated p-MOSFETs on strained (110) SiGe exhibits 180% and 10% higher hole mobility over Si (100) and (110), respectively.

Acknowledgments

The authors acknowledge the technical support of MRL.

References

(1) T.Sato, et.al, J.J. Appl Phys, vol8, p588 (1969).
(2) M.Yang, et.al, IEDM Tech.Dig. p7803 (2003).
(3) K. Rim, et.al, IEDM Tec.Dig., p517 (1995).
(4) Yeo and Hu,
(5) K. Ota, et.al, IEDM Tech.Dig. p27 (2002)

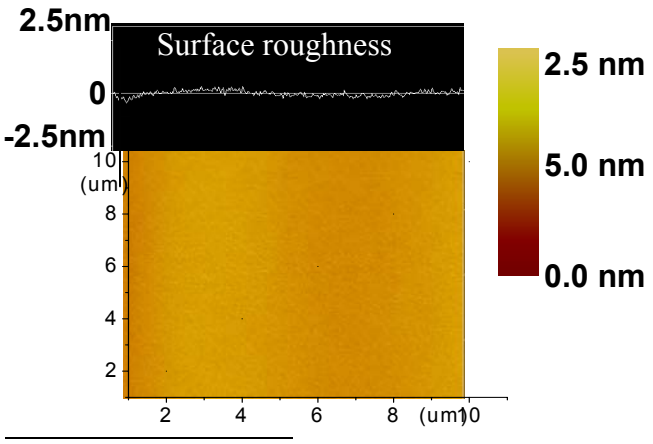

Fig. 1: Top-down SEM image showing 0.180μm^2 SRAM cell after ultra-narrow spacer etch

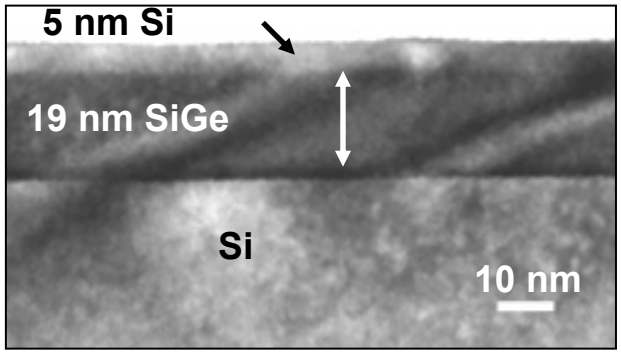

Fig 2. TEM micrograph shows 5 nm Si cap on 18 nm 22% SiGe on Si(110) substrate

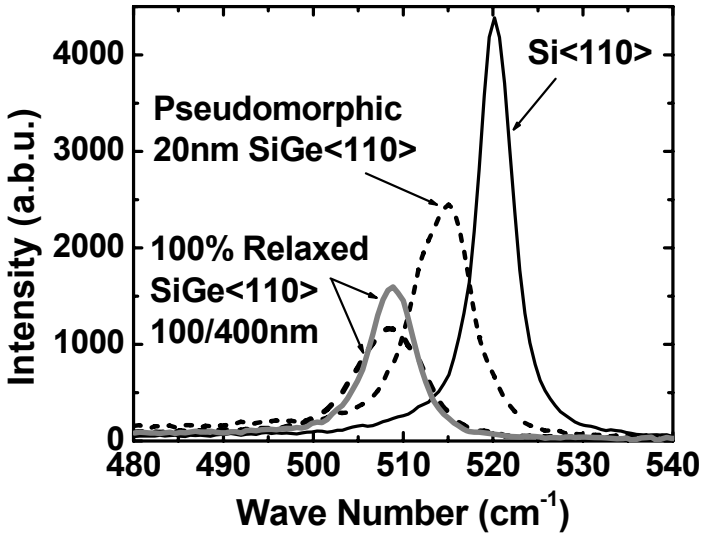

Fig. 3 Raman analysis on SiGe on Si (110) substrate to define strain characteristics

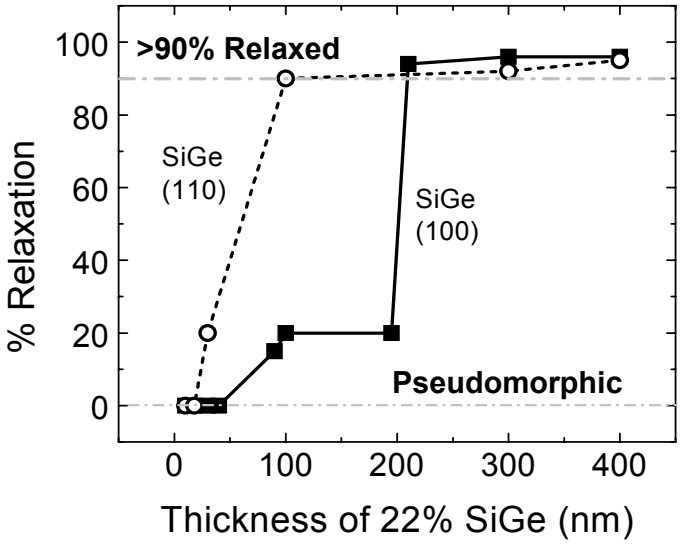

Fig. 4 : The Relaxation state of SiGe 22% on both (110) and (100) orientation substrates

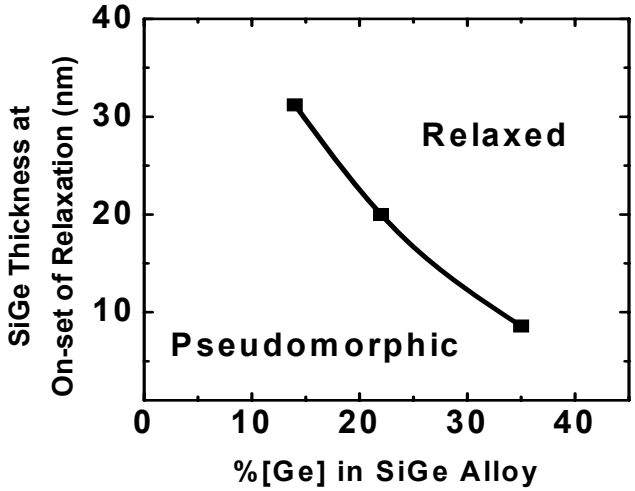

Fig. 5 : New Critical Thickness graph for SiGe on (110) Si orientation substrate

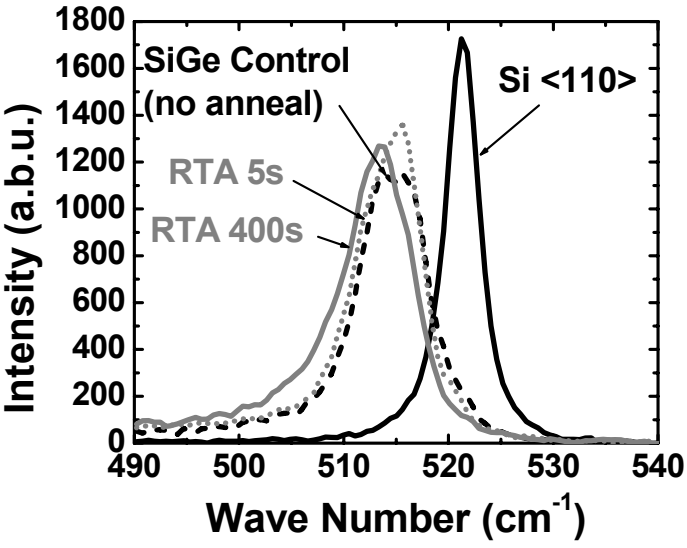

Fig. 6 : Raman analysis of p-SiGe 22% on (110) Si substrate post RTA annealing

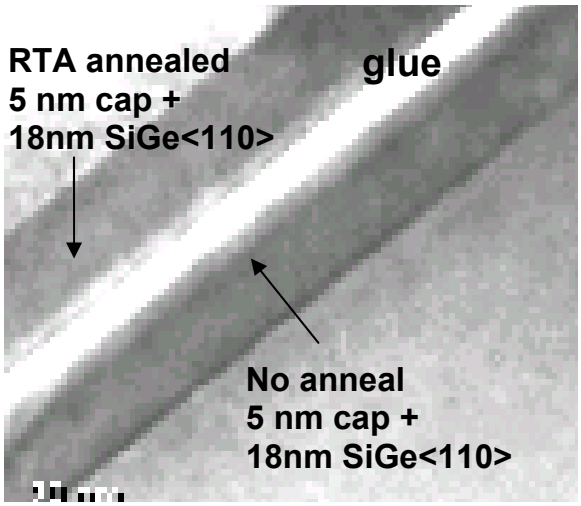

Fig. 7 : TEM micrograph shows no changes of 22% SiGe (110) structure post 1000C RTA annealing

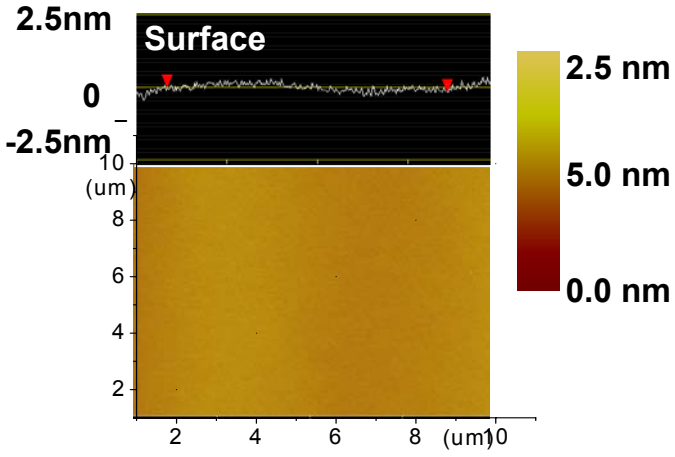

Fig. 8 AFM image of 22% SiGe (110) show no surface Damages was observed post 1000C, RTA annealing

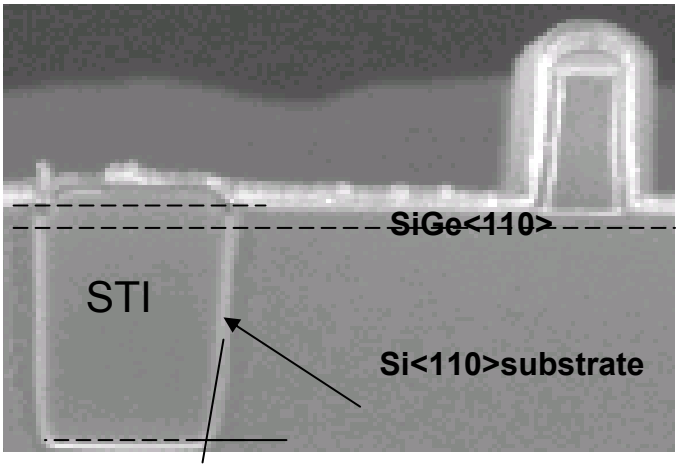

Fig. 9 : SEM micrograph of STI & Poly-Si gate stack on 22%SiGe (110) channel and Si(110) substrate

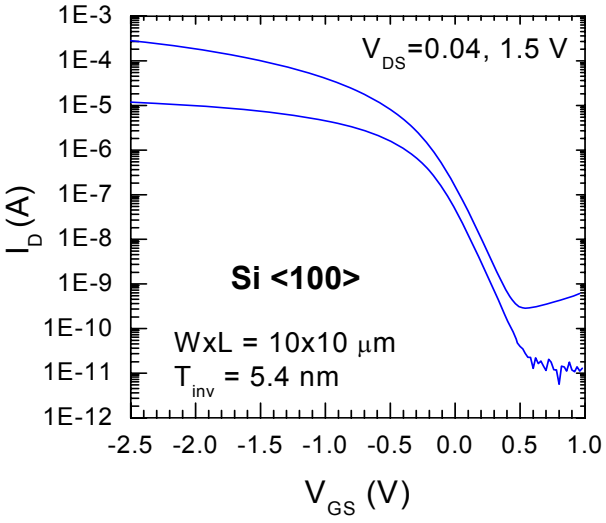

Fig. 10: IV characteristics of SiGe 22% on (110) and (100) Si substrate

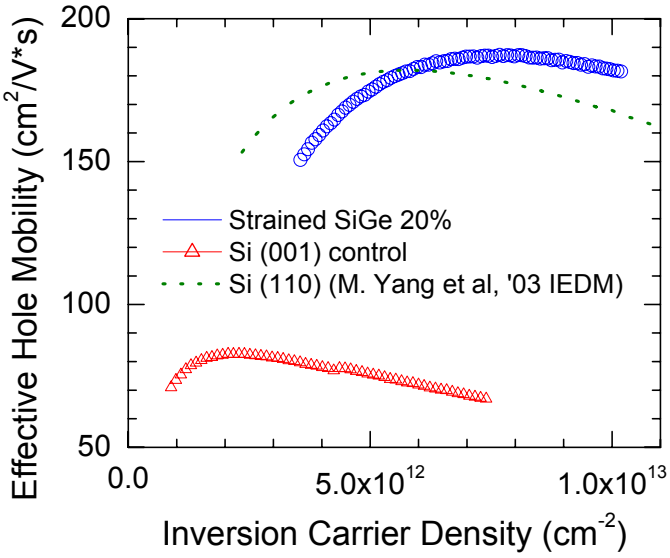

Fig. 11 : Comparison of Hole mobility of compressed 22% SiGe (110) channel FET to Si (100) & Si (110)