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MOSFET with a Silicon Nanowire Channel: Materials Science, Fabrication and Electrical Characterization

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MOSFET with a silicon nanowire channel: materials science, fabrication and electrical characterization

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We report on the fabrication and electrical characterization of n-FETs and p-FETs made with vapor-liquid-solid (VLS) grown silicon nanowires, exhibiting electrical characteristics approaching those of mainstream silicon devices. Near ideal subthreshold slope of 63 mV/decade was measured for top-gated n-FETs with a Si nanowire channel diameter down to 3.5 nm. A key feature of our devices was the low contact resistivity obtained by the fabrication of epitaxial silicon contacts to the nanowire.

Single-crystal silicon nanowires were grown by the VLS method in a UHV-CVD chamber with silane as the silicon precursor and gold as the catalyst. Following the catalyst removal, the nanowires were harvested into a suspension and were dispensed on a silicon-on-insulator (SOI) wafer.

A sacrificial gate line, formed of LPCVD oxide, was patterned over a segment of the nanowire to define the channel region. A wet clean including an HF-last dip was applied before epitaxial growth. Selective silicon growth was used to form the source and drain regions of the device. The epitaxy merged the SOI film with the exposed nanowire body extending from the sacrificial gate line. High resolution TEM confirmed a clean interface between the nanowire and the epitaxial silicon.

The sacrificial gate line was etched and thermal oxidation was used to thin the nanowire in the channel region. The initial SOI film thickness (typically 8 nm) was chosen such that the oxidation fully consumed the SOI film and electrical isolation was obtained between the epitaxially thickened source and drain regions. The channel region was masked and ion implantation was followed by a 1000°C/5 sec rapid thermal anneal (RTA) for dopant activation. The RTA also enabled solid phase re-growth of the amorphized-by-implantation regions in the source and drain by templating from the underlying silicon layer. Both n-FETs and p-FETs were fabricated on the same wafer. Self-aligned nickel silicide was used to form the source and drain contacts, and aluminum lift-off was used to form the top-gate. Fig. 1 illustrates the main components of the device.

Fig. 2 shows a TEM cross-section in a plane perpendicular to the nanowire, taken through the gate of the device. The nanowire orientation was found by lattice imaging to be [-112]. The evaporated Al top-gate does not fully wrap-around the nanowire, as evident by the voids seen in Fig. 2. The voids are the result of shadowing by the nanowire body during evaporation of Al. The thickness of the oxide grown was found to be dependent on the initial diameter of the nanowire, with thinner nanowires growing a thinner oxide. The oxidation was not self-limiting since complete oxidation of nanowires was also observed.

Fig. 3 shows an I_d-V_g characteristic of a nanowire n-FET. The nanowire has a diameter d=11.5 nm, a gate oxide thickness t_{ox}=12 nm, and a gate length L=234 nm. An estimate of the external resistance R_{ext} is obtained by plotting $R_{on}=R_{ch}+R_{ext}$ as a function of $1/(V_g-V_t)$. Subtracting the wiring resistance, and multiplying by the contact area A, gives a contact resistivity of $R \cdot A$=1.1-2.7×10^{-8} Ω-cm^2, similar to reported values for advanced SOI MOSFETs.

In conclusion, we fabricated n-FETs and p-FETs with VLS grown nanowires that exhibit electrical characteristics comparable to state-of-the-art silicon devices. The excellent R_{on} obtained was mostly due to the use of epitaxial contacts.

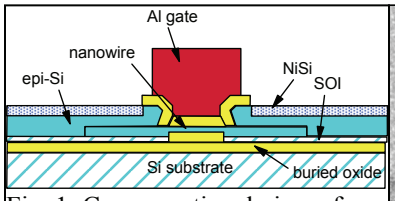

Fig. 1: Cross- sectional view of a nanowire FET with epitaxial contacts. The epitaxy merges the nanowire with the SOI film in the source and drain regions.

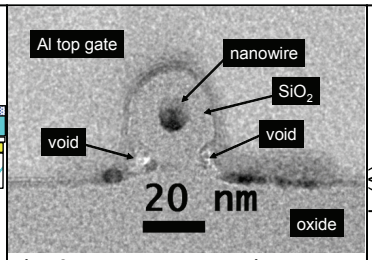

Fig. 2: TEM cross-section through the device gate. The gate does not fully warp around since evaporation was used to deposit aluminum.

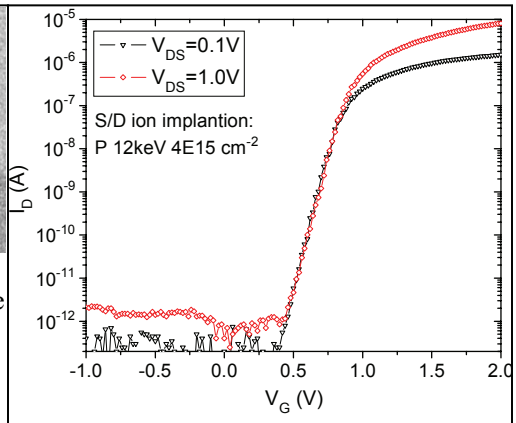

Fig. 3: I_d-V_g characteristics of an n-FET with a nanowire channel.