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SOI Series MOSFET for Embedded High Voltage Applications and Soft-Error Immunity

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ABSTRACT

We demonstrate a simple and novel scheme to achieve high drain breakdown voltage (BV) in a high-speed silicon-on-insulator (SOI) logic technology. In an SOI device with two FETs in series, the common floating node provides a negative feedback that limits the increase of avalanche current. This unique property of SOI provides a way to enhance the breakdown voltage by simply adding more devices in series. Data from 45nm SOI technology show BV>6.5V for two-NFET in series, and BV>10V for three and four-FET in series. Other benefits of SOI series device include >300× reduction in stand-by leakage current and soft-error immunity as compared to a single SOI device. Our result suggests the prospect of integrating high-voltage functions on SOI-based technologies with little or no additional cost.

INTRODUCTION

In advanced CMOS technologies optimized for circuit speed, the drain breakdown voltage in short channel MOSFET is usually quite low, due to heavily doped abrupt junction profiles. In particular, SOI technologies give even lower breakdown voltage than similar bulk technologies due to the parasitic bipolar effect [1]. A body-tied SOI can restore the breakdown voltage to the bulk value at the expense of high parasitic capacitance. For some ASIC applications, voltage handling capability of ~5V is desirable, which is becoming difficult to meet. Series devices on (semi-)insulating substrate have been used as high-voltage RF switches, but can not be used to handle high voltages at lower frequencies or in general logic [2]. For the first time, we show that SOI series device from a high-speed CMOS process can be used for high-voltage logic applications. In comparison, bulk devices in series can not offer the same breakdown voltage benefit due to drain-to-substrate breakdown. Measured results based on 52Å gate-oxide FETs from a 45nm SOI technology [3] are presented. Physical mechanism responsible for the high breakdown voltage is delineated. Since breakdown voltage is usually limited by NFETs rather than PFETs due to the higher impact ionization rate of electrons, only NFET series device results are shown. Other unique SOI series device properties such as low stand-by leakage current and soft-error immunity are also presented.

BREAKDOWN AND LEAKAGE CHARACTERISTICS

Fig. 1 shows schematics of SOI series devices. The diffusion regions from the two neighboring devices can be merged (Fig. 1a) or electrically-connected (Fig. 1b), and the number of devices in series can be more than two (Fig. 1c). The merged diffusion design offers higher density but requires heavy source/drain doping down to the buried oxide to be effective. All the measurement data reported here are from connected-diffusion structures. Fig. 2 compares subthreshold characteristics of a series SOI device and a single SOI device, at the nominal channel length (L_{NOM}) of ~0.22μm. The off current (I_{OFF}) in the series device is reduced by 350× to 10pA/μm at a V_{DS} of 2.5V, and DIBL is reduced by 230mV. A similar trend is observed in Fig. 3 where the gate length is scaled to L_{NOM} / 2=0.11μm. It should be noted that even two sub-nominal devices in series results in 35× lower I_{OFF} and lower DIBL than a single nominal device. The mechanism that is responsible for the series device property can be understood from the measured common floating node potential in Fig. 4. In the off-state, the floating node is charged up to ~1.5V under a drain voltage of 2.5V, by the hole current generated from the high field region near the drain. This effectively reduces V_{DS} across FET 2 and hence reduces I_{OFF} and DIBL. The output I_D-V_{DS} characteristic under V_{GS}=1.5V is shown in Fig. 5 for single SOI devices in both the regular floating-body design and the body-tied design. The breakdown voltage increases with gate length but is limited to about 4V in a long channel (2×L_{NOM}) body-tied design. The floating body devices show an abrupt increase in I_D near V_{DS} ≈1.5V, which is the well-known kink effect due to the onset of impact ionization near the drain.

The output characteristics of two-FET in series is shown in Fig. 6. The breakdown voltage is increased by 2× to >5V for the sub-nominal device and >6.5V for the nominal device. There are two 'kinks' in each I_D-V_{DS} curve, the first one at V_{DS}<2V comes from impact ionization in FET 2, and the second one at higher V_{DS} is from impact ionization in FET 1. The second kink can be eliminated by using a body-tied SOI design for FET 1 only, as shown by the line in Fig. 6. The increase of breakdown voltage in the series device is due to a negative feedback mechanism, which is confirmed by the measured common floating node potential (V_1) in Fig. 7. The calculated voltage drop across FET 2 (V_{DS2}= V_{DS} - V_1) is plotted along with measured V_1. The applied drain voltage is initially dropped across FET 2 until V_{DS2} reaches about 3.5V where avalanche multiplication starts. The avalanche multiplication in FET 2 is self-limited by the floating node which charges up and keeps V_{DS2} from rising further, thus avoiding a runaway breakdown. The additional drain terminal voltage is then dropped across FET 1. When V_1 increases, V_{GS2}=V_G - V_1 reduces and the current conduction mechanism in FET 2 changes from surface-channel FET current to lateral parasitic bipolar current. The family of I_D-V_D curves in Fig. 8 clearly shows the breakdown voltage advantage of the SOI series device over the best-case single SOI device. As more devices are added in the series, the drain voltage is dropped on each device sequentially from the one closest to the drain to the one closest to the source, enabling higher breakdown voltages. In Fig. 9, output characteristics of series devices with 3 FETs and 4 FETs are shown. No signs of runaway breakdown is seen up to V_{DS}=10V (limited by gate dielectric breakdown). Fig. 10 shows measured floating node potentials in a 4-FET series device. The successive rise of V_3 and V_2 with increasing V_{DS} indicates the saturation of voltage drops across FET 4 and FET 3 respectively. The breakdown voltage of the SOI series device is only limited by the number of devices in series, provided that the gate dielectric is thick enough. This is a unique property for SOI. Bulk devices in series are not suitable for high-voltage application due to drain-to-substrate breakdown concern.

SOFT-ERROR IMMUNITY

The SOI series device has built-in redundancy which makes it immune to single-event upsets. Fig. 11 and 12 compare the effect of 1MeV α-particle strike for a single SOI device and a merged-diffusion (Fig. 1a) series SOI device based on simulations. In the off state, when one FET is hit, the other FET keeps the series device off, thus avoiding upset. The total collected charge is reduced by 40× if the α-particle strikes FET 2 and by 400× if it strikes FET 1.

CONCLUSIONS

We showed that high-speed SOI CMOS logic devices can be simply connected in series to achieve arbitrarily large drain breakdown voltage. The only requirement is to add a thick gate oxide that is commensurate with the desired voltage. This unique property of SOI CMOS opens up possibilities for low-cost SoC applications.

REFERENCES

1. K. Young and J. Burns, IEEE Trans. Electron Devices, p. 426, 1988.
2. M. Shifrin, et.al., IEEE Trans. Microwave Theory and Technology, v37, p. 2134, 1989.
3. S. Narasimha, et.al., IEDM Tech. Dig., session 27.3, 2006.

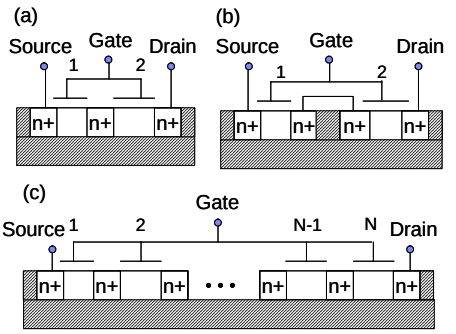

Fig. 1. Schematics of SOI series devices: (a) two NFETs in series with merged common diffusion, (b) two NFETs in series with an electrically-connected floating node, and (c) N devices in series.

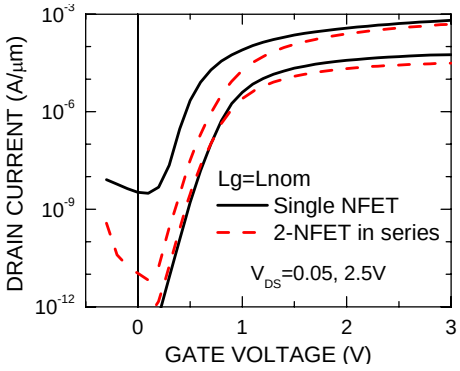

Fig. 2. I_D-V_G characteristics of a single device vs. a series SOI device, at nominal gate length. Series device shows significant I_{OFF} and DIBL reduction.

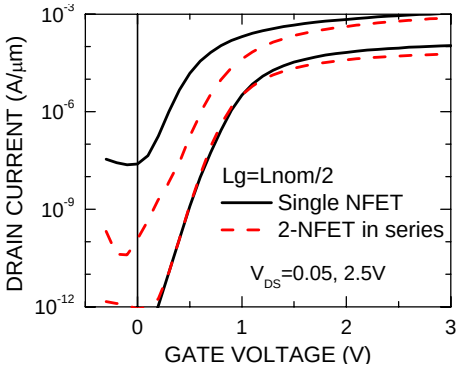

Fig. 3. I_D-V_G characteristics of a single device vs. a series SOI device, at half of the nominal gate length. Series device shows I_{OFF} and DIBL reduction.

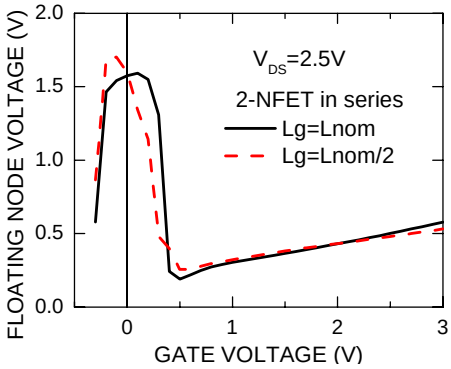

Fig. 4. The common floating node potential in SOI series devices measured by a voltage probe. The common node floats up in the off-state (near V_G~0V).

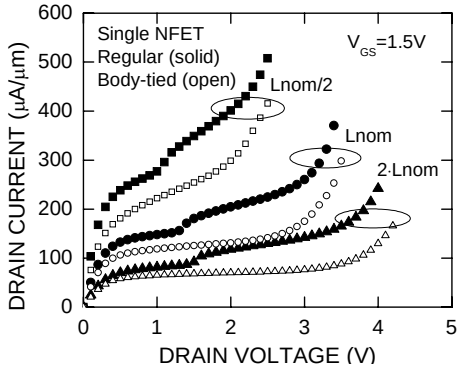

Fig. 5. Output characteristics of regular and body-tied SOI devices at various gate length (Lg). Breakdown voltage increases with Lg but is limited to about 4V.

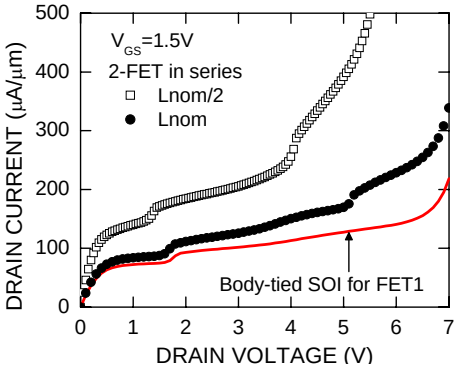

Fig. 6. Output characteristics of two NFETs in series. Breakdown voltage is improved to over 6.5V for two nominal gate length devices in series.

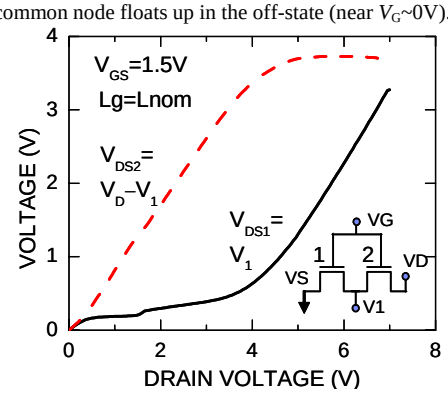

Fig. 7. Measured common floating-node potential (solid line) and extracted V_{DS} across the 2nd FET (dash line) as a function of drain voltage.

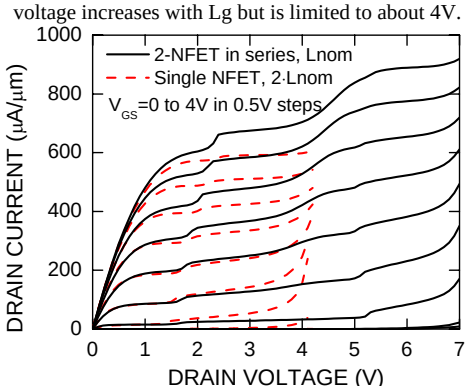

Fig. 8. Family of I_D-V_D curves from two nominal NFETs in series (solid lines, Lg=L_{NOM}) and a single long channel NFET (dash lines, Lg=2L_{NOM}).

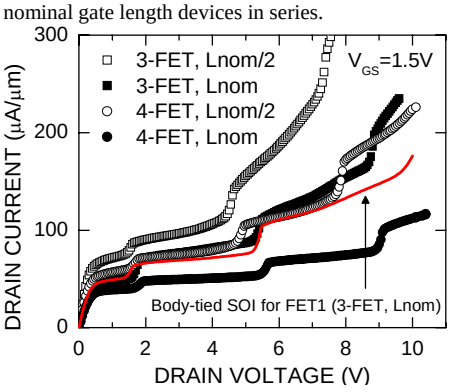

Fig. 9. Output Characteristics of three NFETs in series and four NFETs in series. The drain breakdown voltage can be increased to over 10V.

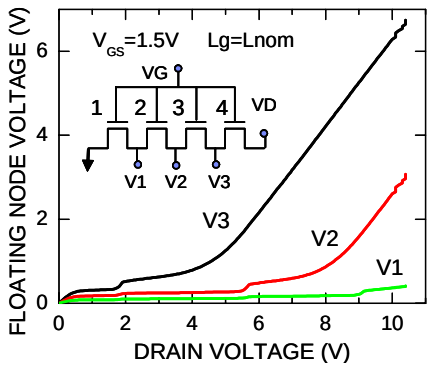

Fig. 10. Measured floating node potential in a 4-FET series device vs. drain voltage. Rise of V_3 and V_2 shows saturation of V_{DS} in FET 4 and 3 respectively.

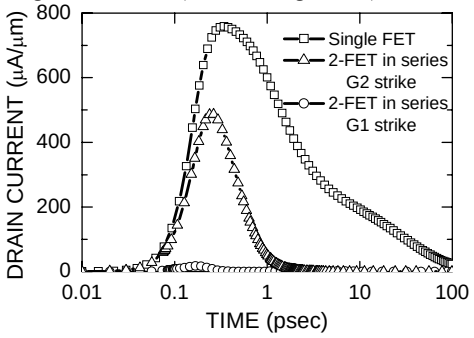

Fig. 11. Comparisons of simulated drain transient current after 1MeV α-particle strikes. SOI series devices show lower transient current over a much shorter time span than that of a single device.

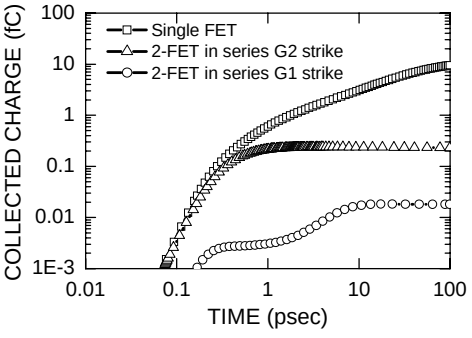

Fig. 12. Comparison of simulated collected charge after 1MeV α-particle strikes. SOI series devices show 40× to 400× reduction in collected charge than a single device.