RC24582 (W0806-039) June 11, 2008
Materials Science

IBM Research Report

An Overview of Pb-free, Flip-Chip Wafer Bumping Technologies

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(To be submitted for the special issue of JOM, June, 2008, on “Pb-free and Pb-bearing Solders”)

An Overview of Pb-free, Flip-Chip Wafer Bumping Technologies

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Abstract

To meet the European Union Restriction of Hazardous Substances (RoHS) requirements and the continuing demand for lower costs, finer pitch and high reliability flip chip packaging structures, considerable work is going on in electronic industry to develop Pb-free solutions for flip chip technology. In this paper, various solder bumping technologies developed for flip-chip applications are reviewed with an emphasis on a new wafer bumping technology called C4NP (Controlled-Collapse-Chip-Connect New Process). Several inherent advantages of C4NP technology are discussed over other technologies. This paper will also discuss the recent development and implementation of Pb-free C4 interconnections for 300 mm wafers demonstrated at IBM. In addition, some metallurgical issues associated with C4NP technology are discussed.

Introduction

The growth of flip-chip interconnect technology over the conventional wire-bonding scheme has been remarkable in recent years, owing to the ever-increasing demand for microelectronic packages with higher I/O counts, smaller form factor, enhanced electrical and thermal performance in all application spaces including consumer electronics. Since July, 2006, following the EU's RoHS legislation [1, 2], the consumer electronics industry is now offering "green" products by eliminating Pb-containing solders and other toxic materials. The flip-chip solder interconnections used in high performance electronic systems are also in transition to Pb-free solder technology. A key technical element in implementing Pb-free, flip-chip interconnection is the wafer bumping technology. In addition to the change from Pb-containing to Pb-free solders, the other important transitions in the wafer bumping industry include moving wafer processing to 300 mm wafers, reducing solder bump size and pitch, reducing bumping cost, and still achieving higher quality and reliability.

Several wafer bumping technologies have been developed since IBM first introduced "C4 (Controlled Collapse Chip Connect)" technology in 1960's for the first-level interconnect in multi-chip module packages used in mainframe computers [3, 4]. These include solder evaporation, electroplating, paste screening, ball placement methods and others. To address the ever-increasing demand for lower costs and improved quality, in September of 2004, IBM and Suss MicroTech announced a new wafer bumping technology called C4NP (C4 New Process), [5, 6]. SUSS has been developing the manufacturing infrastructure, while IBM has been rapidly qualifying the technology. Recently, IBM has announced the successful qualification and implementation of Pb-free, flip-chip bumping for all 300 mm wafers in high volume manufacturing production using C4NP technology with equipment partnership with Suss Micro Tech Inc [7, 8].

In this paper, we will first review the conventional wafer bumping technologies currently in practice, and then discuss the new emerging technology of C4NP with its inherent advantages and challenges as compared to other technologies. In addition, the fundamental metallurgical considerations associated with C4NP technology are also discussed.

Flip-Chip, Wafer Bumping Technologies

1) Solder Evaporation

This is the original C4 wafer bumping technology developed by IBM nearly 40 years ago. Both Under-Bump-Metallurgy (UBM) and high purity solders of Pb and Sn metals are sequentially evaporated through a metal mask in a vacuum system onto the entire surface of silicon wafers to form an area array of solder bumps. A typical composition of high Pb solder bumps is 97Pb-3Sn (in wt.%). A typical UBM structure consists of a multi-layer thin film stack of Cr/CrCu/Cu/Au [3, 4]. High purity Pb and Sn metals are usually co-evaporated by adjusting the parameters of the vapor pressure of each metal. After evaporation a reflow process in forming gas atmosphere (at about 350°C) is employed to melt the solders for a uniform composition and to bring the bumps into a spherical shape.

The metal mask technology is a critical component of the solder evaporation process. A metal mask is normally made of a thin foil of sintered Mo sheet, having openings aligned to the I/O pad locations on a silicon wafer. The metal mask also determines solder deposition area and volume. It is a batch process. Multiple wafers, each containing many chips, are mounted on a dome and simultaneously evaporated with UBM and solders, respectively. Since the evaporation process is performed at an elevated temperature, the significant thermal expansion mismatch between a Si wafer (2.6 ppm/^{o}C) and Mo mask (4.8 ppm/^{o}C) must be taken into account in the design and fabrication of a metal mask to maintain an accuracy in bump placement.

As the wafer size increases progressively from 125, 150, 200 to 300 mm, along with the continuing shrinkage of bump size and pitch, the metal mask technology has reached its limitation. Additionally, for Pb-free, flip-chip wafer bumping applications, switching the bump composition from high Pb to high Sn is another technical challenge, due to the low vapor pressure of Sn, and therefore the slow evaporation rate to produce a bump height to nearly 50-100 μm.

2) Electroplating of Solder Alloys

To migrate to 300 mm wafer bumping IBM has been electroplating C4 solder (97Pb-3Sn) since the early 1990 using a TiW/CrCu/Cu UBM structure [9]. This process starts with passivating a wafer to define the via structure of bond pads, followed by deposition of a blanket layer of UBM, which also serves as a ground connection for solder bump plating. Instead of using metal mask, a photo-resist, thick dry film is applied to silicon wafers, then

exposed/developed to define openings for solder bump plating. After electroplating, the resist mask is stripped and the sputtered UBM is selectively etched by using solder bumps as the etching mask. Solder bumps of a mesa structure are reflowed in a controlled atmosphere to form a spherical shape. This process has been proven to be very reliable and has been widely used in the industry for C4 solder bumps of high-Pb, Sn/Pb and, recently, Pb-free solder compositions.

In 2004, IBM has successfully developed the Pb-free C4 plating process by incorporating a maximum use of the existing production-line capital infrastructure and process for ease of manufacturing [10]. The two key components of the Pb-free C4 structure are the UBM and C4 metallurgy. It is well known that the Pb-free, Sn-rich solders are highly reactive and, therefore, require a more robust reaction barrier metallurgy in the UBM in order to withstand aggressive high-temperature-storage (HTS), multiple reflows and electromigration requirements. For this purpose, a Ni layer is commonly chosen as the barrier layer to be incorporated in the UBM structure for Pb-free C4 bumps. Using the TiW/CrCu/Cu/Ni UBM, both Sn-Cu and Sn-Ag solder metallurgy have been qualified and put into production for the current applications.

However, a major drawback of electroplated solder bumps for Pb-free, flip-chip applications is the limited choice in solder alloy compositions. By nature, the control of binary or ternary compositions of solder bumps is extremely difficult during electroplating. As of today, a ternary composition of Sn-Ag-Cu alloys is not yet able to be electroplated in a reliable fashion. Recently, to solve the interlayer-dielectic-delamination (IDL), improve electromigration (EM) performance and other properties, Pb-free solder alloys are sometimes modified by doping a minor amount alloying elements (such as Zn, Ni, Co, Fe, rare earths, and others) to Sn-rich solders. Electroplating of solder bumps is shown to be difficult to accommodate this trend. Furthermore, the growing need from wafer bumping manufacturers, to reduce bumping cost and to search for an environmentally-friendly solution in dealing with plating waste, has motivated IBM to develop a new, low-cost wafer bumping process for the future Pb-free, flip-chip applications, This new low-cost and environmentally-friendly bumping technology, C4NP, announced by IBM in 2004 [5, 6], uses raw solder ingots and reusable glass molds to fill and transfer solder to the wafer.

3) Solder Paste Screening

Solder paste screening process has been initially introduced in 1970's for surface mount technology (SMT) to replace the plated-through-hole (PTH) soldering used in the assembly of printed circuit boards (PCB). The solder paste technology has been further developed for flip-chip wafer bumping by Delphi Delco Electronic Systems and Flip Chip Technologies in the 1990's for automotive and consumer electronics applications [12]. Since solder paste material consists of fine solder power particles, flux, and other organic materials, there is about 50% volume reduction upon reflow. This is a serious limitation of using solder paste materials in fine-pitch wafer bumping. High void population in solder joints is another reliability concern for high performance applications. Since solder paste screening method is a relatively low cost process, it has been widely used in consumer electronics. However, there are severe limitations to extend this technology to either 300 mm wafer, particularly in fine pitch (≤ 150 μm) applications..

4) Solder Ball Placement

Solder ball placement (or ball mount) method has been widely used in BGA (ball grid array) and CSP (chip scale package) applications. The typical solder ball size is ~300 μm in diameter used for CSP and ~750 μm for BGA. Solder ball placement practiced with an automated machine is a two-stage process. A controlled amount of flux materials is dispensed onto the UBM pads of a silicon wafer or substrate using a precision screen printer as a first step. Then solder balls are placed by an automated solder transfer head onto the fluxed UBM pads. After inspection, the wafer or substrate is reflowed to form solder joints. Applying this technology for flip-chip applications is quite challenging since the flip-chip solder bump is normally about 100 μm in diameter or less.

In 2001, Nippon Steel Corporation demonstrated Micro-Ball wafer Bumping (MBB) technology capable of C4 size flip-chip application [13]. Recently, they constructed a mass production line for forming solder bumps of 120 or 150 μm in diameter for the applications of consumer electronics [14]. In addition, the reliability qualification of MBB technology has been also demonstrated with Pb-free solders of various compositions and Ti/NiV/Cu-UBM. Future extendibility of this technology to fine-pitch (< 150 μm) and still cost-effective has not been demonstrated yet.

C4NP for Pb-free Wafer Bumping

C4NP grew out of earlier work at IBM Research in which a new injection molded solder (IMS) process produced advanced thermal interfaces for chip cooling application [5]. It was quickly realized that IMS could readily be applied for making solder interconnect structures. As schematically shown in Fig.1, C4NP first fills molten solder into prefabricated cavities in a reusable glass mold, bump template that mirror-images the I/O footprint of a silicon wafer. After the solder is solidified, an inspection step assures that all the cavities are properly filled. Separately, while in parallel, wafers are prepared with patterning of the UBM which is compatible with the desired solder alloy. The last step is to transfer bumps from mold plate to wafer, namely aligning the filled glass mold and joining it in mirror image fashion to the silicon wafer above the solder reflow temperature. This transfers the solder volumes from the cavities to the wafer. The glass molds are reusable, thus keeping costs low. Fig.2 shows (a) an example of the cavity structure in a glass mold, (b) solder bumps filled in the cavities, and (c) solder bumps transferred onto a silicon wafer and reflowed to form solder bumps in a spherical shape (about 100 μm in diameter).

Several important advantages can be listed for C4NP:

- alloy flexibility including multi-component Pb-free alloys
- no volume change from deposition to final bump; extendible to fine bump size & pitch
- same tool set for both 200 and 300 mm wafers
- low material costs in comparison to paste, perform or chemical solution for plating
- optimal yields by bump mold inspection before transfer to wafer
- rapid turn-around time by pre-filling bump molds ahead of wafer completion
- efficient solder usage for environmental and economic benefits
- extendibility to finer pitch, 50 μm pitch has been demonstrated [19]
- process simplicity similar to stencil printing

Table I compares the salient features of each wafer bumping technology in terms of their advantages and limitations. The advantages of C4NP over other technologies are outstanding, providing high-end capabilities with low-end costs to meet present and future Pb-free wafer bumping needs. Recently, IBM have reported the development and implementation of C4NP technology for 300 mm wafers with Pb-free, flip-chip solder bumps jointly with SUSS Micro

Tech [7, 8]. As a part of C4NP technology development and product qualification, studies for both 150 and 200 μm pitch C4 bumps have been conducted with plated Ni/Cu UBM and Sn-Cu and Sn-Ag solders. All reliability tests including deep thermal cycling, accelerated thermal cycling, C4 electromigration, and others were passed to demonstrate the robustness of the C4NP process. IBM is currently ramping up manufacturing volume production of all 300 mm wafers for 200 μm pitch using C4NP, and is expanding its use to a finer pitch.

Metallurgical Issues of C4NP

1) Solidification and Undercooling

Melting and solidification of a small volume of solder is a key metallurgical process associated with C4NP. During the mold fill process, a molten metal is directly dispensed into the small cavities of a glass mold and then immediately solidified to minimize defect population and to ensure solder volume uniformity [6]. In the subsequent process of solder bump transfer, all solder bumps in a glass mold are again melted and transferred onto the UBM structure of a silicon wafer and then solidified. To provide a better understanding on the C4NP process as well as chip joining integrity, a systematic investigation was conducted to find critical factors affecting the undercooling of Pb-free, flip-chip solder bumps by DSC (differential scanning calorimetry) and the direct observation of individual solder bumps in a glass mold during melting and solidification [15, 16]. The amount of the undercooling of Sn-rich solders is found to be strongly affected by solder volume, inversely proportional to its volume (or effective diameter of solder balls). It is also found that the solder composition and UBM significantly affect, but not so strongly by other factors such as the cooling rate and holding temperature of a mold plate used in C4NP. Sn-0.7Cu C4NP solder bumps in a mold plate were under-cooled by as much as 90°C from its melting point, while a less amount of undercooling (40 to 60°C) was observed on a Si chip with Cu/Ni UBM [15]. The direct observation of individual flip-chip-size solder bumps on a glass mold during their solidification process revealed the random nature of molten solder nucleation process, and also confirmed the similar amount of the undercooling measured by DSC [16]. It was also found that some minor alloying elements such as Zn, Co, and Ni are quite effective in reducing the amount of undercooling in Sn-rich solders [16]. A large amount of the undercooling observed in Pb-free solder bumps would cause an unwanted situation such as "balled-up" of the solder bumps during the mold fill process of C4NP technology [6]. Hence,

minimizing the amount of the undercooling of Pb-free solder bumps is desirable and this can be readily achieved by the C4NP technology owing to its flexibility of solder alloy choice. As the size of solder bump continues to decrease in the future flip chip interconnect structure, controlling of the undercooling behavior of a very small solder volume would be a critical issue in the successful wafer bumping process, such as C4NP.

2) Microstructure and Mechanical Properties of C4NP Solder Bumps

The microstructure of as-reflowed C4NP solder bumps is determined by the complex interplays among several factors such as solidification conditions (such as reflow temperature, cooling rate, etc), solder composition, minor alloying elements, UBM, and others. Fig.3 shows a microstructure of as-reflowed C4NP solder bumps (Sn-1.8%Ag, TiW/Cu/Ni UBM). This is a cross-polarized optical image showing a fine microstructure. The fine microstructure shown here is not a general grain boundary structure. It is a result of cyclic twinning in β-Sn matrix occurred during the solidification of Sn dendrite cells [17]. More detailed discussion on the fine microstructure of Sn-rich solders is reported later at this Symposium [18].

The mechanical properties of C4NP solder bumps have been evaluated by micro-hardness measurements on their cross sections. An example of the micro-hardness indentation is shown in Fig.4, on a C4NP solder bump of Sn-1.8Ag-0.05Ni. Fig.5 compares the micro-hardness data of two kinds of C4NP solder bumps (Sn-1.8Ag-0.05Ni vs. Sn-0.7Cu-0.05Ge-0.05Ni) as a function of reflow cycles at 250°C. The Sn-Cu bumps are softer than Sn-Ag bumps, and the number of reflows does not affect much their micro-hardness, indicating the interfacial reactions occurring between the solders and UBM do not contribute to any increase in their hardness.

Further Applications of C4NP

The extendibility of C4NP technology has been continually demonstrated in several areas of microelectronic applications, such as ultra-fine pitch, micro-bumping for 3D packaging [19], Cu-cored flip-chip joints [20], micro-via fill, substrate bumping and others.

C4NP technology has been successfully extended to ultra-fine pitch, micro-bumping using a test vehicle with a full area of micro-bumps at 50 μm pitch for both 200 mm and 300 mm wafers in manufacturing environment [19]. Glass molds for ultra fine-pitch micro-bumping were fabricated using borofloat glass plates, which have a coefficient of thermal expansion closely matching to that of the silicon wafer. The micro-bump volume uniformity was achieved by patterning Cu/Cr film on the mold surface as an etch mask to fabricate cavities with a uniform volume. Pb-free, Sn-Ag solder bumps were first filled into the micro-cavities and then aligned and transferred to silicon wafers with the sputtered TiW/Ni/Cu UBM structure. Test chips with about 11,000 micro-bumps were also bonded to a silicon substrate to demonstrate the feasibility of chip assembly in 3D packaging applications [19]. The challenge and methodology in high-speed inspection for the large number of micro C4 bumps (about 9 million) are being resolved.

In another application of C4NP technology, to enhance thermal fatigue and electromigration resistance of the current flip-chip solder joints, a new structure has been demonstrated by combining C4NP technology with Cu spheres for high density interconnections [20]. Cu micro-spheres are placed in the cavities on a silicon mold and then transferred to C4NP solder bumps on the wafer using the same tool used in C4NP transfer process. After dicing, the chip with solder bumps plus Cu spheres is joined to a substrate which has been pre-soldered. The Cu spheres placed in the middle of each flip-chip joint serve as a stand-off structure, yielding a taller solder joint than the conventional solder bumps. Owing to the high electrical and thermal conductivity of Cu, this new structure is expected to have a better thermal fatigue and electromigration resistance [20].

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Table I. Comparison of Wafer Bumping Processes

	Evaporation	**Plating**	**Paste Screening**	**Ball Placement**	***C4NP***
Cost	Fair	Poor	Good	Fair	Good
Reliability	Good	Good	Poor	Good	Good
Yield	Fair	Good	Fair	Fair	Good
Alloy Flexibility	Fair	Poor	Good	Good	Good
Extendibility to 300mm	Poor	Good	Poor	Good	Good
Very fine bump	Poor	Good	Poor	Fair	Good
Process complexity	Fair	Poor	Good	Fair	Good
Industry proven	Good	Good	Good	Fair	Fair

C4NP Process

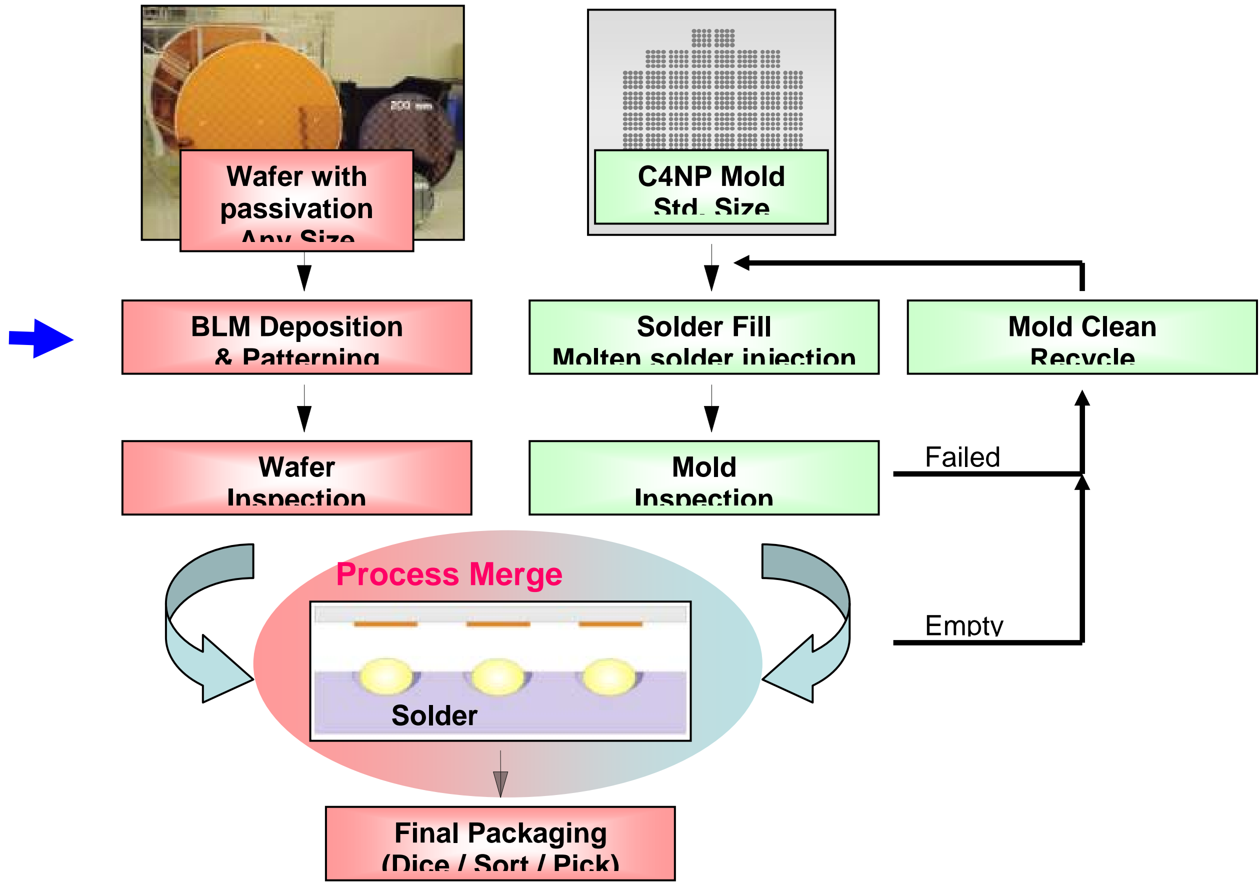

Fig.1. C4NP process flow showing two parallel processing of UBM preparation on wafers and solder fill in a mold and then solder bump transfer to the wafer.

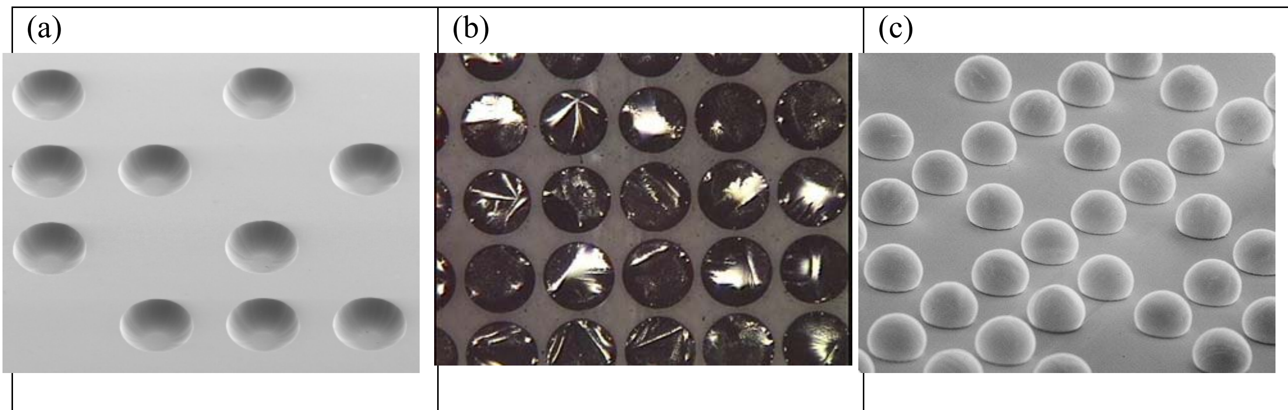

Fig.2. Micrographs showing (a) typical cavity structure in a glass mold used in C4NP, (b) solder bumps filled in the cavities, and (c) solder bumps transferred onto a silicon wafer and reflowed to form solder bumps in a spherical shape (about 100 μm in diameter).

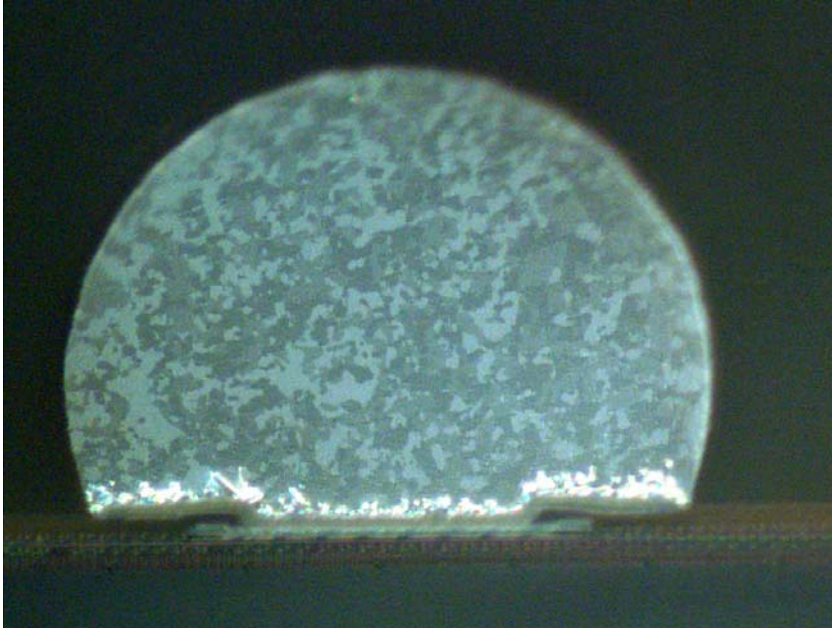

Fig.3. A typical cross-polarizing optical image of a C4NP solder bump (in cross section), showing a fine microstructure of cyclic twinning in β-Sn matrix and the IMC formation at the interface (Courtesy of C. Goldsmith, IBM).

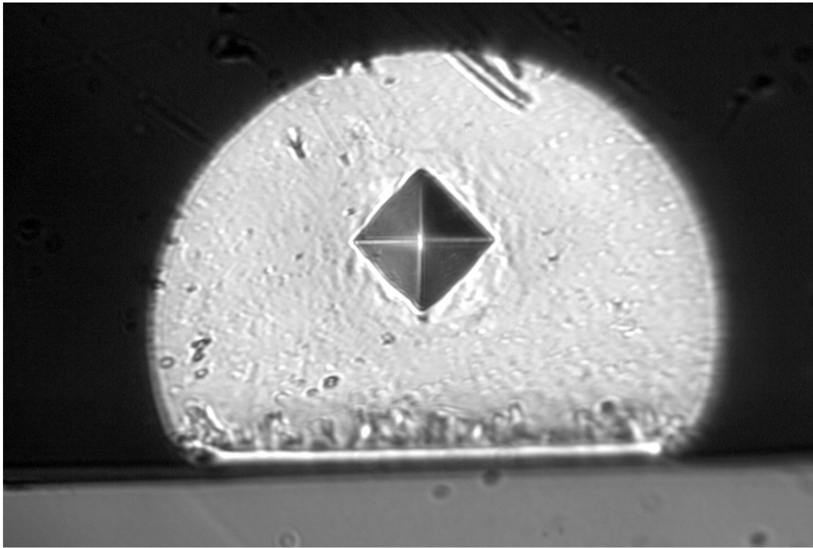

Fig.4. An example of a micro-hardness indentation of C4NP solder bump of Sn-1.8Ag-0.05Ni (reflowed at 250°C)

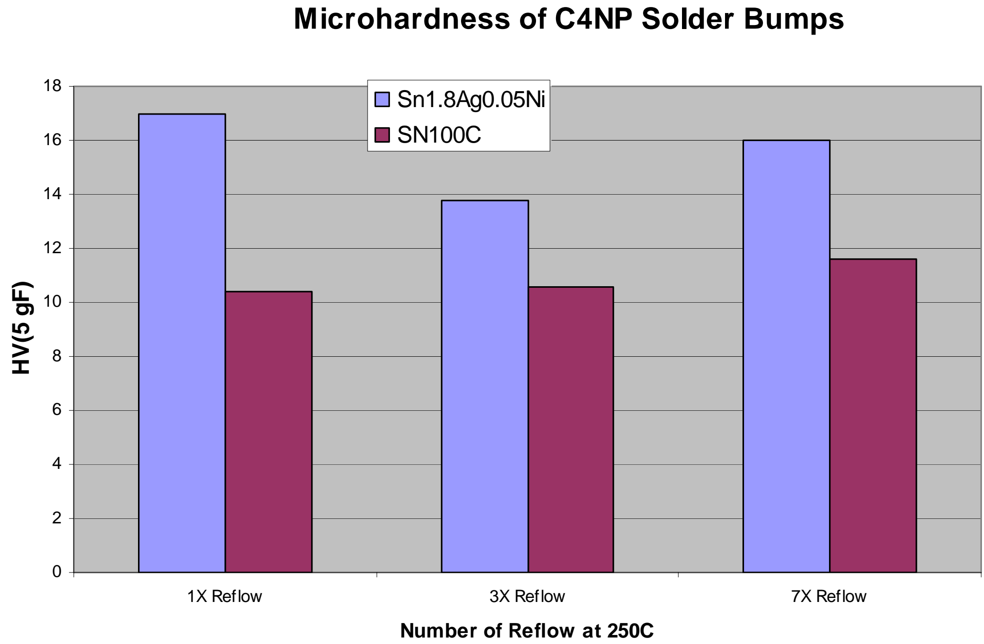

Fig.5. The micro-hardness data of two C4NP solder bumps (Sn-1.8Ag-0.05Ni vs. Sn-0.7Cu-0.01Ge-0.01Ni) as a function of reflow cycles at 250°C.