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The Over-Bump Applied Resin Wafer-Level Underfill Process: Process, Material and Reliability

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Abstract

The over bump applied resin (OBAR) process is a wafer-level underfill (WLUF) process in which a filled resin is applied over the bumps of a wafer, dried, diced into coated chip which are aligned and joined through a substrate resulting in an underfilled flip chip package. This process has been evaluated by IBM on several test vehicles in close cooperation with Henkel (formerly Abelstik) which developed a material specifically to fit this process. The critical steps to make this technology work are alignment of OBAR coated chip to a substrate, elimination of significant voids and formation of a fillet with appropriate shape and size. The reliability of the material was evaluated after capping and BGA ball mount through JEDEC level 3 pre-con followed by DTC (deep thermal cycling), T&H (temperature and humidity), and HTS (high temperature storage). While some difficulties still exist, the OBAR process has been shown to be a viable alternative to capillary underfill application.

Introduction

While capillary underfill technology has been successfully used for flip-chip (FC) packages, alternatives such as no-flow [1-3] and wafer-level underfill (WLUF) [4-7] processes have been investigated vigorously in the past years. There are several drivers for this search for alternatives among them the high stress placed on peripheral solder bumps in large chips which can lead to the formation of so-called white bumps after chip joining and before the underfill is present to provide stress mitigation between chip and substrate; the elimination of processing steps such as flux application and flux residue cleaning which is becoming increasingly difficult with shrinking size of the gap between chip and substrate particularly in large FC applications; the increased number of solder bumps with ever tighter pitch which make it difficult to eliminate voids in the center of large chips; the longer time to underfill large chips; the trend to smaller ball pitch (e.g., from 50 μm to 30 μm) in consumer electronic applications and the need for smaller fillets to save space.

No-flow processes held much promise but it seems to be impossible to avoid inclusions of filler particles in the solder joint affecting reliability of these connections.

WLUF processes seem to suffer additionally from the difficulty to align the WLUF material covered chip to the substrate. This is one of the reasons why most WLUF processes either use chips in which the top of the C4 solder bumps are kept free of the WLUF resin or are exposed subsequent to the application of the WLUF layer or use a WLUF material that is unfilled. The first approach suffers from poor fillet shape (see Fig. 1), the second from the high CTE of unfilled underfills which limits the application space for these processes.

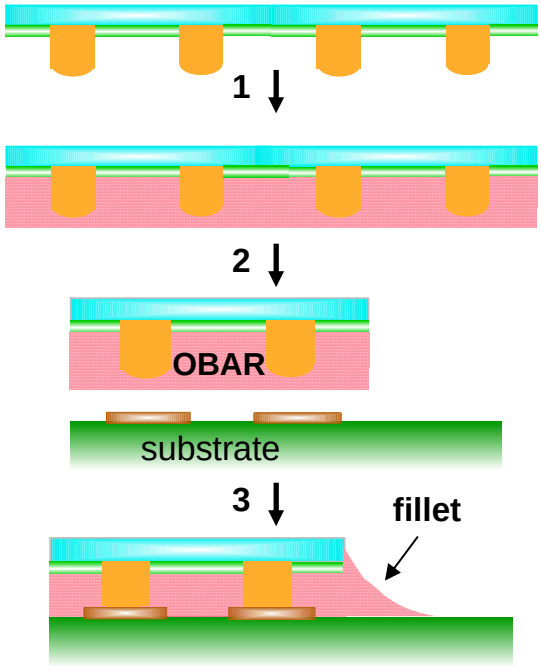

Fig. 1. Schematic OBAR WLUF process with 3 steps

Starting in 2000 as part of a NIST ATP program, IBM developed a process [Fig. 1, 1a] which we now call over bump applied resin (OBAR) process, in which a filled resin is applied over the bumps of a wafer and dried or b-staged, the b-staged wafer is diced, a singulated, OBAR coated chip is aligned to a substrate and joined by melting the solder bumps. This process has been evaluated in close cooperation with first Natl. Starch & Chemical [8] and then Henkel (formerly Abelstik) that developed a material [9] specifically to fit this process.

Since the first publication of this process [7] both OBAR process and material have been optimized and exercised on several test vehicles and the reliability of the joined packages has been evaluated.

Material

The OBAR material consists of an epoxy based thermoset that is filled with silica particles at a filler loading of 43%. It exhibits a solution viscosity of 6700 cps and can be spun with high thickness control onto a bumped wafer (Fig. 1 step 1).

After b-staging the material is tack free and exhibits excellent dicing (Fig.1 step 2) behavior without delamination, chipping or cracking. Joining (Fig. 1 step 3) was accomplished in a Toray flip chip bonder. This process involves alignment, heating of the dried substrate and chip to about 100 C, followed by bringing chip and substrate together and applying some force to press the solder bumps through the OBAR material until they contact the substrate solder pads. The assembly is then heated rapidly through the chip holder until the solder melts. The force is reduced and z-control in the joining head is used to achieve the required gap size. Subsequently the assembly is cooled. A typical joining profile is shown in Fig. 2.

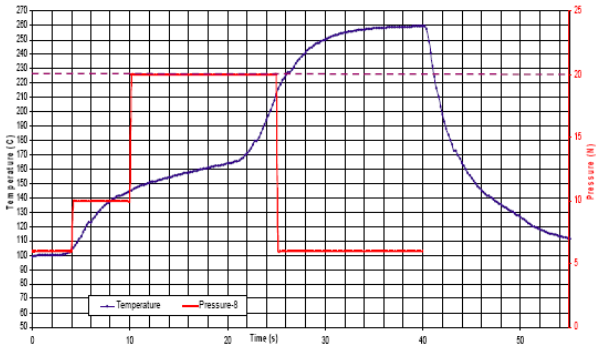

Fig. 2. Typical joining profile

While significant cure occurs during the chip join process, a post-cure process may be necessary. The fully cured OBAR material results in an underfill with a glass transition temperature (Tg) of 105 C, a CTE of 32 ppm/C, and a modulus of 6.4 GPa at RT.

Alignment Process

Aligning a chip that is covered with a glossy white, opaque material such as the OBAR poses a challenge to conventional alignment systems, since the reflective surface makes it difficult to obtain contrast on the surface and once that is overcome the picture of the solder bumps is diffuse and irregular (Fig. 3 a). In a sequence of automated steps the outline of the solder bumps is identified (Fig. 3 b) and used for aligning an OBAR coated chip to a substrate.

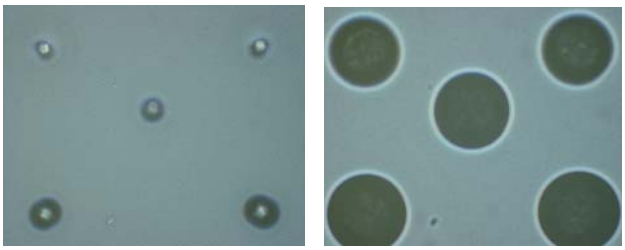

Fig. 3. a: Solder ball image visible through focus on surface; b: after moving focus below the surface

Test Vehicles

Process and material were evaluated using several test vehicles (TVs). The first TV was a 14.7 mm x 14.7 mm CMOS 11S chip with ~ 4,000 SnCu C4 solder balls produced using IBM's C4NP process. The substrate was a 42.5 mm organic substrate of 3-6-3 construction built with state of the art materials. Several other TVs were tested, the last of which was a 9.2 mm x 12.7 mm TV with ~1800 SnCu solder balls. Solder joining in the 14.7 mm x 14.7 mm TV was incomplete for several solder joints in each corner. However, we found that this was due to the bonding head of the flip chip bonder which was too small to heat the corners in this TV. When the smaller TV was used all C4s were joined well. Typical cross sections of the outer C4 connections for this latter TV are shown in Fig. 4.

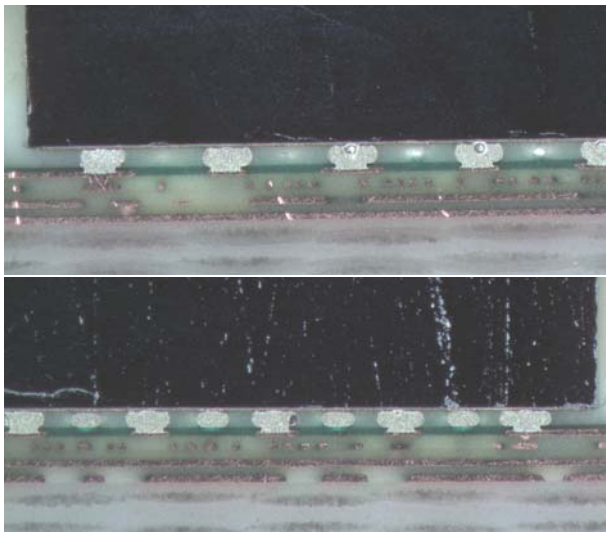

Fig. 4. Left (top) and right (bottom) side of cross sections through the outer C4 connection row of a TV.

Solder Joint Quality

None of the solder joints produced by this process seem to have any filler inclusions as is common in no-flow processes [10, 11] and no fillers were found in any of the cross sectioned joints. Further most of the bumps also did not show any voids. However, as figure 4 shows solder voids are found in some of the solder joints. Initially this was puzzling, since the C4s were made by IBM's C4NP process which has the lowest amount of solder voids of any bumping process. However, the substrate solder pads were made using solder paste which contains significant amount of flux which creates volatiles during solder melting. Since the OBAR resin does not allow any volatiles to escape, volatiles are either caught in the bumps or right next to it as shown in Fig. 5.

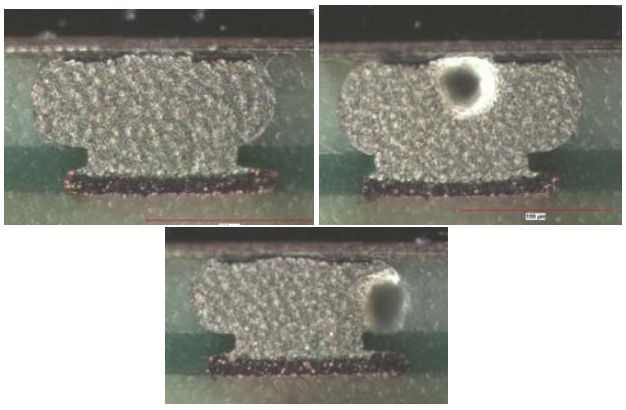

Fig. 5. Defect free (top left) and voided (top right) solder bump; void next to solder bump (bottom)

Solder joint voids and voids near solder joints are an issue faced by all pre-applied underfill processes. This issue can be avoided entirely by IBM's Substrate Injection Molded Solder (Substrate IMS) process [12]. We are in the process of demonstrating the advantage of combining substrate IMS with the OBAR process.

White Bump Protection

White bumps [13] defined as appearance of white spots in ultrasonic images where C4s are expected are an indication of solder joint fails in the interlayer dielectric (ILD). They are an indication that the stresses between chip and substrate are so high that a fracture in the ILD in the vicinity of the solder ball has occurred. White bumps are created during joining of a flip chip before underfilling as evidenced by underfill in the ILD cracks (Fig. 6). Such white bumps can be eliminated completely by the OBAR WLUF process (Fig. 7). We have not seen any white bumps on any test vehicle that uses OBAR technology.

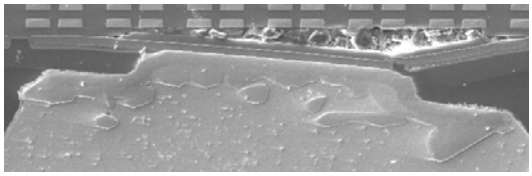

Fig. 6: Structure of a white bump.

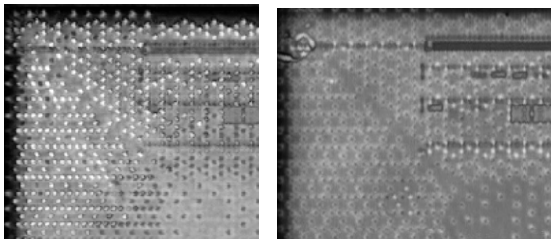

Fig. 7: White bumps are visible (left) in capillary underfilled chip and same corner of this chip (right) using OBAR technology

Reliability Testing

After capping and SAC alloy BGA bumping the packages were electrically tested using JEDEC level 3 preconditioning. No opens were found in either TV, although as pointed out above the corner C4s of the 14.7 mm x 14.7 mm TV were poorly joined. This became apparent after 250 deep thermal cycles (DTC) of -55 to 125 C during which these C4s showed opens (Fig. 8). However, all other C4s were not affected by DTC stressing. 96 hours of highly accelerated stress testing (HAST) at 130C and 85 % relative humidity (RH) did not lead to fails.

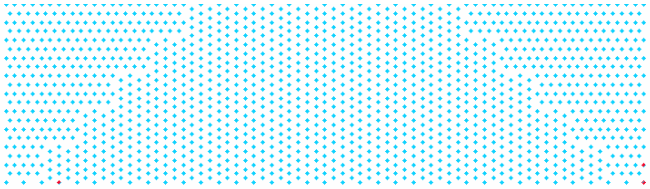

Fig. 8: Locations (red dots) of 3 opens after 250 DTC cycles at lower corners of 14.7 mm x 14.7 mm TV.

Reliability testing results of the small TV are being collected.

Packages were found to have higher planarization compared to conventionally joined flip chip packages. This is a result of the fact that chip and substrate are being held flat during heating in the thermal compression joining tool.

Conclusions

A wafer-level underfill process in which the pre-applied material is deliberately applied over the bumps of a wafer (over-bump applied resin or OBAR process) is described. Steps to overcome the two major obstacles, alignment and void management, are discussed. Advantages of this process include protection against fracture of the ILD caused by excessive stress on unprotected solder bumps ("white bumps"). Other advantages include increased package planarization achieved during the joining step and the standard advantages of WLUF processes such as fewer process steps.

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