RC24940 (W1001-100) January 29, 2010
Electronic Packaging

IBM Research Report

Flip-Chip Interconnections - Past, Present and Future

Sung-Kwon Kang, Da-Yuan Shih
IBM Research Division
Thomas J. Watson Research Center
P.O. Box 218
Yorktown Heights, NY 10598

William E. Bernier
IBM Systems & Technology Group
Hopewell Junction, NY

Research Division
Almaden - Austin - Beijing - Cambridge - Haifa - India - T. J. Watson - Tokyo - Zurich

LIMITED DISTRIBUTION NOTICE: This report has been submitted for publication outside of IBM and will probably be copyrighted if accepted for publication. It has been issued as a Research Report for early dissemination of its contents. In view of the transfer of copyright to the outside publisher, its distribution outside of IBM prior to publication should be limited to peer communications and specific requests. After outside publication, requests should be filled only by reprints or legally obtained copies of the article (e.g., payment of royalties). Copies may be requested from IBM T. J. Watson Research Center , P. O. Box 218, Yorktown Heights, NY 10598 USA (email: reports@us.ibm.com). Some reports are available on the internet at http://domino.watson.ibm.com/library/CyberDig.nsf/home .

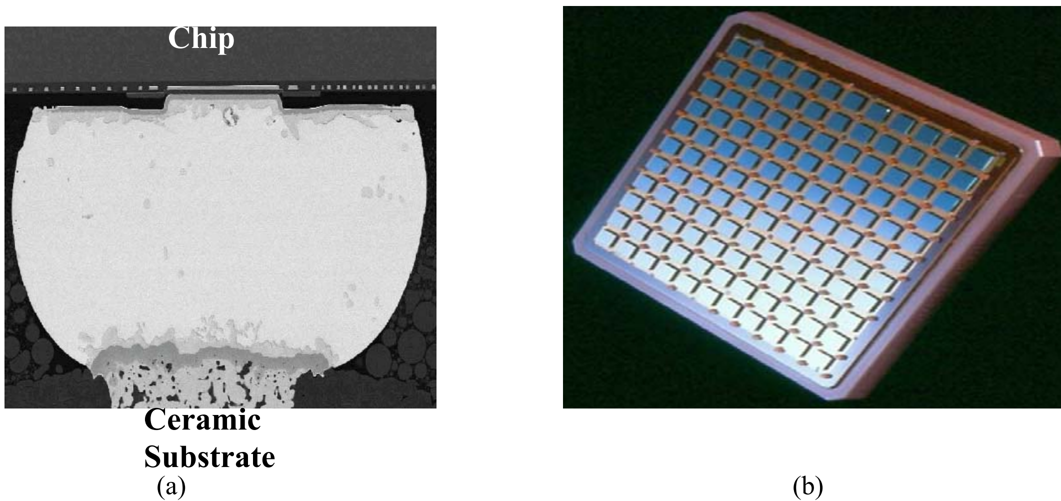
4.1. Evolution of Flip-Chip Interconnection Technologies

Flip-chip interconnection technologies have been extensively used in many microelectronic applications for high performance systems as well as consumer electronics in recent years. There are several types of flip-chip interconnects being used today in the industry, which include high-Pb solder bumps joined to a ceramic substrate, high-Pb bumps on chip joined to eutectic PbSn on a laminate substrate, all eutectic PbSn bumps, Pb-free bumps, Cu pillar bumps, and Au-stud bumps. Steady improvements have been made in high performance packages, such as having interconnects greater than 10,000 I/O's with a pitch less than 200 μm, migrating from ceramic to low-cost organic substrates, replacing high-Pb with Pb-free interconnects, and others. Fundamental reliability issues, especially with the Pb-free solder bumps, remain to be solved. As the expiration of European Union (EU) Reduction of Hazardous Substance (RoHS) exemption approaches soon, Pb-containing solder bumps for flip-chip interconnects are expected to be phased out by 2014. However, the recent introduction of fragile low-k, or very fragile ultra low-k interlayer dielectrics (ILD) into the back-end interconnect architectures in the advanced semiconductor devices has imposed serious technical challenges in integrating Pb-free technologies for high-performance systems. The hard or less compliant Pb-free solder bumps coupled with the fragile ILD layers in a large chip can cause cracking in the ILD structure, which often leads to mechanical/electrical failures of the chip. How to control the cracking of low–k ILD layers during chip joining has become an urgent issue to be resolved together by the semiconductor and packaging industries. Another reliability challenge associated with the implementation of Pb-free solder in flip-chip packages is the poor electromigration (EM) performance of Sn-rich solders. This is mainly due to the highly anisotropic crystal structure of Sn, causing the fast solute diffusion along its c-axis, combined with the aggressive interfacial reactions with under-bump metallurgy (UBM) and laminate pads.

In this Chapter, the recent progress of flip-chip assembly processes is presented with ceramic substrates and organic laminates, including the new bumping technologies such as C4NP and Cu pillar bumping. In the following, various reliability challenges of Pb-free, flip-chip applications are extensively discussed along with possible solutions for specific applications.

High-Pb-based Solder Joint

The first, and the original type of flip chip interconnect structure, was introduced by IBM in 1964 [1], which is based on bumping high-melting temperature, high Pb-Sn solder (3-5% Sn and 97-95% Pb) on chip and subsequently joined to a ceramic carrier at a temperature greater than 320°C. This is a fully melting Controlled-Collapse-Chip-Connection (C4) solder joint as shown in Figure 1. The standoff gap between the chip and substrate is determined by the surface tension of the solder, solder volume and pad sizes on the chip and substrate. The C4 bump height, Sn content and size of a chip are the major factors determining the fatigue life of the C4 joints during the power-on and -off machine cycles [2]. Due to the close CTE match between the chip (CTE, ~3 ppm/^{o}C) and ceramic substrate (CTE, 3-6 ppm/^{o}C), along with the highly compliant high-Pb soft solder, no underfill is needed to meet the reliability requirements. In this structure, a simple UBM consisting of a multi-layer structure of Cr/CrCu/Cu/Au along with the high Pb solder, has been successfully used for several decades and demonstrated excellent reliability [3-5].



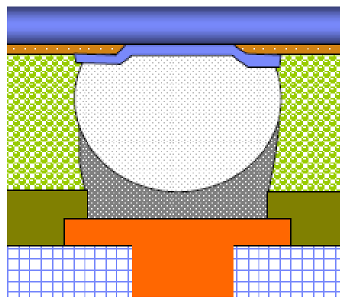
(a) (b)

Figure 1; (a) Flip-chip solder joint (97Pb/3Sn) formed between a chip and a ceramic carrier. (b) Multi-chip module containing 121 flip chips mounted on a glass ceramic substrate (CTE ~3ppm/^{o}C) without underfill [5].

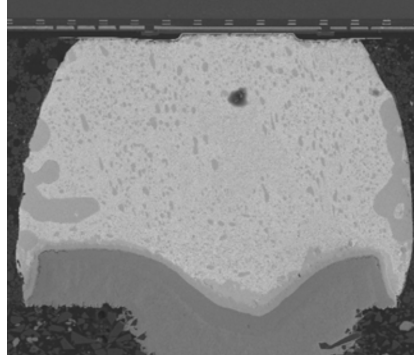
High-Pb Solder on Chip Joined to Eutectic Solder on Laminate carrier

The move to organic substrates drives the need for a lower-melting-temperature solder to replace the high-Pb solder. The organic materials are typically epoxy-based and are not stable at temperatures in excess of 250°C for a prolonged time. One way to circumvent this problem

is to deposit low-melting-temperature eutectic PbSn solder on laminate pads, or on the high-melting bumps on the chip. As shown in Figure 2, a high-Pb solder bump on chip is joined to a low-melting-point solder on a laminate pad. This combination allows the assembly of chip and laminate at temperatures compatible with a low-cost organic laminate. This is a huge breakthrough that IBM (Japan) pioneered to allow direct chip attachment (DCA) to low cost organic laminate carrier [6, 7]. To ensure that the solder joint can survive the large strain generated from the global thermal expansion mismatch between the laminate (~17 ppm/^{o}C) and the chip (~3ppm/^{o}C), a thermally compatible underfill material was developed. When the chip/underfill/laminate is bonded into one entity, it deforms simultaneously and the relative movement between the chip and laminate and, therefore, the strain on solder bumps is greatly reduced [8]. Figure 2 shows the package assembly with a high-Pb solder bump on a chip joined to eutectic solder on the laminate, followed by flux residue cleaning and then underfilled. The same UBM, Cr/CuCu/Cu, which has been successfully used for high-Pb C4 bumps for decades, can not survive multiple reflows and high temperature storage tests. When the dual solder layers are reflowed for multiple times (up to 7 times), the Sn content in the solder matrix near UBM continues to increase with each reflow, accelerating the reaction with UBM and eventually leading to complete separation of the Sn-Cu intermetallics from the base of UBM, as shown in Figure 3. The solution to the problem is either the use of a more robust reaction barrier layer, such as Ni, or to increase the Cu thickness. NiV and NiFe barrier layers [9] are also reported to have good interface stability when joined to high-Sn solders, such as full-melt eutectic 37Pb/63Sn or Pb-free (Sn>95%) solder C4 bumps. After joining a chip to laminate, the flux residues need to be thoroughly cleaned and the assembled module must be underfilled and cured to overcome the CTE mismatch between the chip and organic laminate. With underfill, even large chips with dimensions up to 15 mm, survive the thermal cycling tests (-45 to 100°C, one cycle per hour). On the other hand, without underfill, even a small chip failed before 300 cycles [10, 11].



(a)



(b)

Figure 2. The package assembly showing a high-Pb solder bump on chip joined to eutectic solder on the laminate and then underfilled; (a) schematic drawing and (b) a cross-sectional view of an actual solder joint.

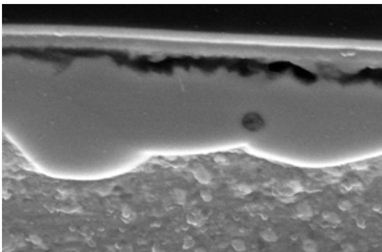


Figure 3. Open failure caused by separation of solder/IMC from UBM.

Pb-free Solder Joint

Although the amount of solder volume used in flip-chip interconnects is much smaller than used in BGA or surface mount solder joints, the environmental legislation required to replace Pb-containing solders with Pb-free solders in flip-chip applications. Pb-free solders, such as popular SnCu, SnAg and SnAgCu, all contain more than 95 wt.% of Sn, which not only have higher melting temperatures than eutectic PbSn, but are highly reactive with UBM and substrate pads. This necessitates a thicker UBM and/or more robust reaction barrier layer, such as Ni or NiFe [9] to survive multiple reflows and various reliability tests without being totally consumed.

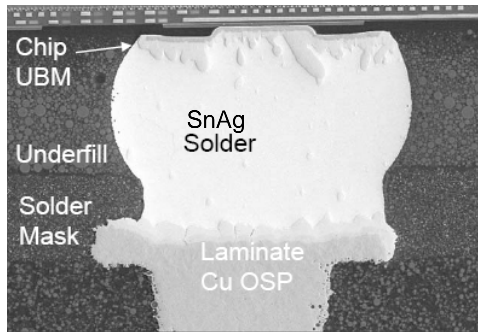


Figure 4. SnAg solder bump joined between Ni UBM and Cu OSP, and tested for high temperature storage.

For Pb-free solder applications, Ni UBM is a popular choice as a reaction barrier layer because it reacts much slowly and wet well with Pb-free solders. As shown in Figure 4, SnAg solder is joined between Ni UBM on the chip and Cu-OSP laminate pad, and subsequently subjected to high temperature storage at 170 ^{o}C for 1000 hours. The solder joint remains intact with controlled growth of intermetallic compounds at the interface between UBM and solder, as shown in Figure 5. Another popular UBM choice for Pb-free solders is thick Cu UBM. On Cu, SnAg or SnAgCu solder forms two intermetallic phases; Cu_6Sn_5 adjacent to the solder and Cu_3Sn adjacent to the Cu [12-14]. The interfacial reactions between Cu, Ni and Pb-free solders are further discussed later in other sections.

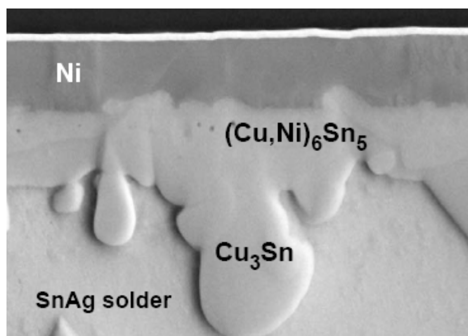


Figure 5. Controlled IMC growth of Ni UBM with SnAg solder.

Cu Pillar Joint

Cu pillar bump is another flip-chip structure [15]. It takes an advantage of the mature Cu electroplating technology commonly used in BEOL structure. There are two versions; one with solder cap plated on top of Cu pillar, and another with solder totally applied on the laminate pad. Figure 6 is a SEM image of an area array of electroplated Cu pillars with Sn cap on top at 100 μm pitch [16]. The cross-sectional view is shown in Figure 7, as used by Intel on the micro-processor chips [17]. Its superior EM

performance, along with the other advantages, makes it an attractive flip-chip interconnects technology. However, the stiff Cu pillar along with a thin solder joint is less compliant and, thus, makes it more difficult to integrate on the chip BEOL structure without cracking the fragile low-k ILD materials. The stress mitigation methods and its bumping process will be further discussed in the later sections.

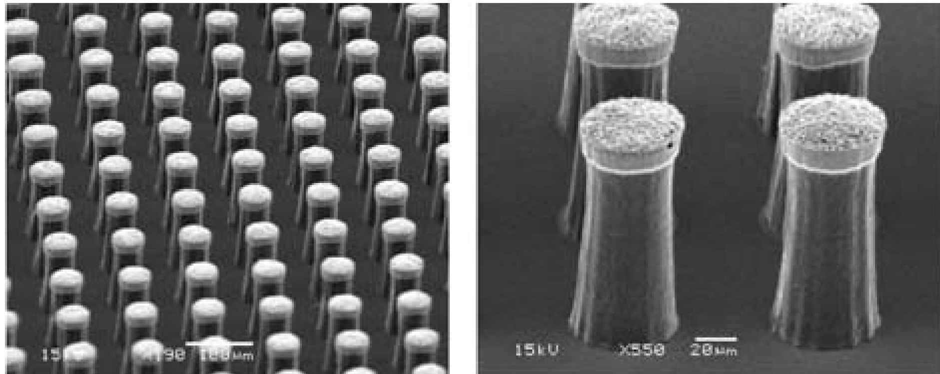


Figure 6. An area array of electroplated Cu pillar bumps with Sn cap at 100 micron pitch and 80 micron height [16].

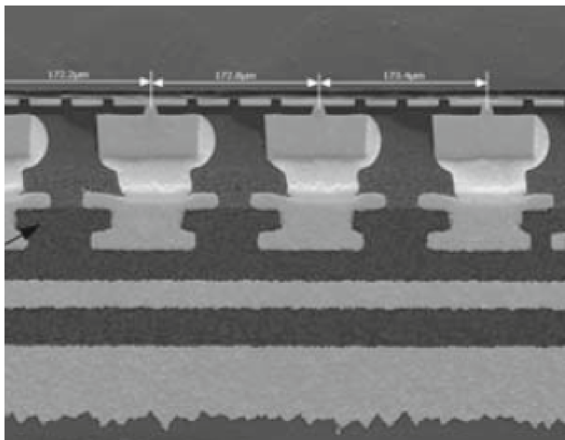


Figure 7. Cross-section SEM image of Cu bumps joined to laminate substrate [17].

4.2. Evolution of Enabling Assembly Technologies

Wafer Thinning and Wafer Dicing (covering Cu/low k devices)

Wafer thinning is practiced widely today for a variety of applications. Processing consists of placing a bumped wafer with bumps down onto a backer sheet. The wafer is immersed in de-ionized water and then ground with a rough grit polish or so-called kiss polish to complete the operation. Typically, 300 mm wafer have thickness of 780 um, while 200 mm wafers or smaller wafers have 730 um in thickness. Wafers may be ground with the kiss polish to remove as little as 50 um of material. Combined with the rough grit polish, wafers as thin as 50 um thick may be produced.

Wafer dicing today is practiced using two general processes – saw dicing and laser dicing. In dicing the wafer has already been bumped and is attached to a backer tape on the back side of the wafer. In saw dicing the diamond saw disk is selected in thickness depending on the width of the kerf and the thickness of the wafer. The wafer is typically immersed in de-ionized water and a stream of de-ionized water is directed on the active cut area. One or more passes may be used with the saw to separate individual devices which are held in place by the backer tape prior to picking. Saw blades may be beveled or straight depending on the width of the cut and the cut finish desired. Laser dicing is similar in initial preparation. In addition, a protective coating material is applied to the bumped wafer surface to guard against ablated material from the laser action depositing on the bumps or passivation surface. One or more passes by the laser may be needed to dice the wafer. A combined process is also often used wherein initial laser passes are used followed by completion with saw dicing. The laser dicing protective coating is removed promptly after processing. Saw dicing has been used effective for years in manufacturing and can leave scallops and chipped silicon areas at the edge of the singulated devices. Laser dicing may leave a much rougher surface from the ablating action of the laser, but is much less likely to result in scalloping and edge chipping. The rough edge area on the singulated devices provides an excellent avenue for mechanical interlock of the underfill encapsulant in subsequent processing.

Wafer Bumping

There are a number of wafer bumping technologies available for flip-chip interconnects, which provide mechanical support for and electrical path to the device. The wafer bumping technologies currently used include; electro-plating of solder bumps on the UBM on a wafer, screen printing of solder paste on a wafer, direct deposition of molten solder on the UBM using the C4NP (Controlled Collapse Chip Connection New Process), Cu pillar bumping, and conductive adhesives including both isotropic and anisotropic materials. Each has its own niche in the application space based on the consideration of cost, application suitability and flexibility.

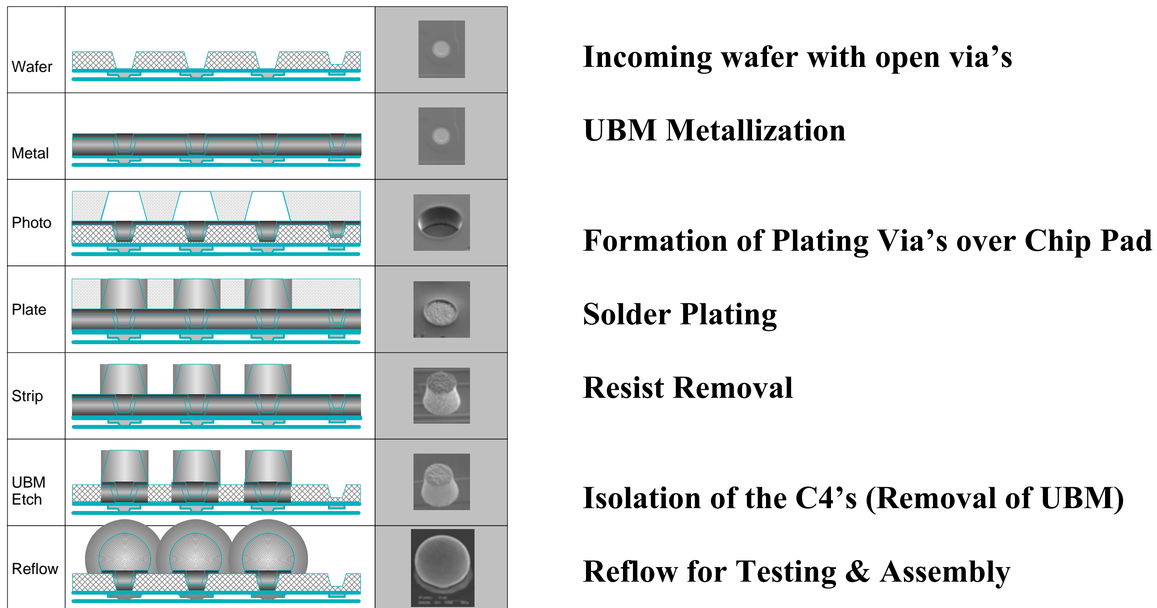
In each bumping process, the UBM structure is used to establish the wetting area of the solder on the device and provide a base for chip joining through the formation of intermetallic compounds at the interface during solder reflow cycles. Common UBM types include TiWCrCuCu, TiWNiV, TiWNi, TiWNiCu and others (more discussion in the later sections). Typical solders used with these UBM types are PbSn, SnAg, SnAgCu, and SnCu of various compositions (refer to Pb-free solders section).

Plating processes for solder bumping include a series of steps outlined in Figure 8. Incoming wafers must have interconnection via's available to process. The UBM metallization as described above is applied by plating or an appropriate alternate technique. A photo-resist is deposited and patterned on the wafer over the device pads for bumping. The solder metallurgy is then plated in one or more steps to deposit the appropriate solder composition on the chip pads. The photo-resist is then stripped from the wafer. The UBM metallization is then removed by etching in areas where solder has not been deposited. The solder bumps are then reflowed to form characteristic truncated sphere shapes.

Plating is widely used for wafer bump processing because plating tools are widely available and plating solution chemistry is abundant and economical. There are some inherent challenges to the processing that can affect yield of the process. Undercut can occur during the UBM etch process; not only removing the excess UBM metallurgy but also undermining the UBM at the edges of the solder bump areas. Careful process control is required. Plating is also subjective to the current density in the plating process, causing significant variations in solder volume and height unless appropriate process control such as thieving is implemented. Photo-

resist stripping can leave residues if solvent selection, stripping solution agitation, and duration are not carefully controlled. Residues can result in metal contamination or electrical bridging to occur if the contamination extends between two or more solder bumps. Proper care in process set up and process control would facilitate excellent production results.

Figure 8. Process outline for wafer bumping formed by electroplating



(W.E. Bernier & F Pompeo, "IC FCPBGA Packaging: A Tutorial", presented at Georgia Institute of Technology Packaging Research Center, Atlanta, GA, Sept,18, 2007)

Solder paste screening has been widely used as a relatively inexpensive technique for applying bumps to wafers. The UBM metallurgy is initially applied to the wafer forming the appropriate metallization over the device pads. A screening mask can be formed from etched and/or laser processed metal sheets with holes formed in the pattern of the wafer bumps or, alternatively, photo-resist can be applied to the wafer to provide the function of the mask and subsequently be removed after bump deposition. The solder paste contains very fine particles of

solder balls, which are mixed with flux, solvent, and thixotropic agents. The solder paste is screened through the mask which is patterned with openings where the bumps are desired. After screening the solder paste is reflowed to form solder bumps. If solder resist were used for the mask it would subsequently be removed.

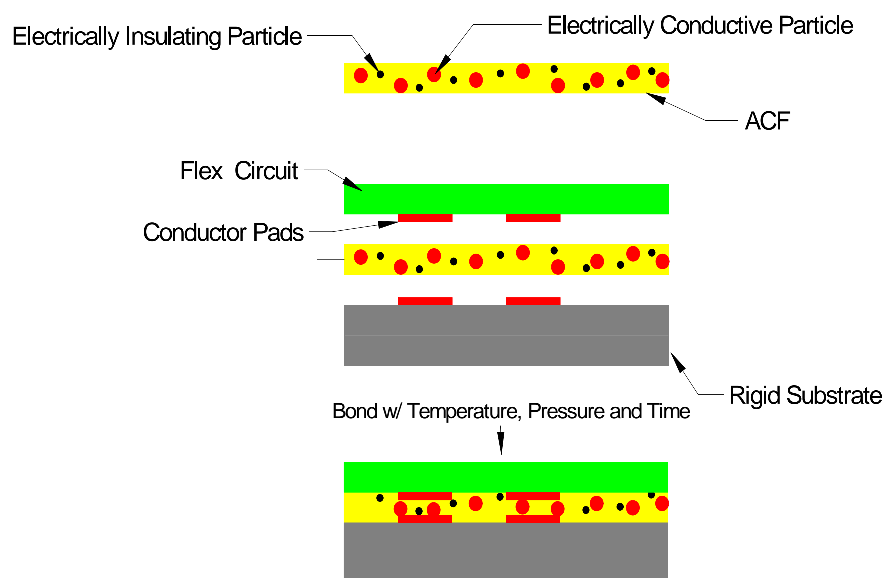
There are some key challenges with using solder paste screening which may limit its use and extendibility in manufacturing application. Solder pastes are well known to form voids interior to the solder bumps. Large voids can result in low solder volume which may have yield or reliability concerns. The openings of solder mask screens can be easily blocked, which may prevent adequate solder deposition, resulting in yield loss or rework.

With anisotropic conductive adhesives an electrical connection is made by a monolayer of electrically conductive particles that are deformed in a compressive manner during the bonding process. The particle volume fraction in the adhesive film is below the percolation in order to ensure that the insulation resistance in the x-y plane is maintained over distance greater than the conductor spacing. The conductive particles which are used are typically either solid metal or metal plated polymer spheres. The particles can be coated with an electrical insulating layer that ruptures during bonding. In the bonding process, either the device or the carrier used should be adequately flexible – as noted in Figure 9, where a flexible circuit carrier is used in assembly. If both connections on either side of the anisotropic film are rigid, then any lack of planarity between them will drive elastic recovery after bonding, which can result in increased contact resistance or electrical opens. During the bonding process it is essential to maintain electrical contact, alignment, parallelism, and uniform pressure across the anisotropic film. Typically the formed bond line is between 3um and 10 um in thickness. A minimum level of 15 to 20 conductive particles is generally required in the bond area to provide reliable contact resistance to be maintained through the life of the application. The anisotropic electrically conductive film thickness selection is routinely based on the circuit line width and the pitch of the electrical contacts. There needs to be sufficient adhesive between the contacts to fill the space. The circuit line height is typically less that 14 um to accommodate the anisotropic electrically conductive film thickness used. The adhesive material properties are important to control based on several factors. The coefficient of thermal expansion of the particles should be matched to the adhesive. The glass transition temperature, adhesion strength, modulus of the

adhesive and its resistance to moisture are all important to maintain processing capability and reliability.

C4NP solder bumping process, a novel wafer bumping technology, is described separately in the following section. In addition, the fabrication process of Cu pillar bumps is also discussed in a separate section.

Figure 9. A typical bonding process using anisotropic conductive film.



(W.E. Bernier & F Pompeo, "IC FCPBGA Packaging: A Tutorial", presented at Georgia Institute of Technology Packaging Research Center, Atlanta, GA, Sept,18, 2007)

Flux and Flux Cleaning

Fluxes used in electronic packaging are formulated to react with stannous oxide and related species on the surface of solder bumps or pre-solder on the laminate bond pads. Species used in the flux system often include tertiary amines and carboxylic, dicarboxylic or related organic acids. These species form complexes or chelates with the stannous oxide and related Sn(II) compounds. This reaction is important to provide wettable surfaces for joining at solder reflow temperatures. Typically, fluxes are not designed to react with stannic oxide or Sn (IV) compounds, which if formed, are customarily difficult to remove and thus may significantly inhibit solder wetting under reflow conditions. Commercially available fluxes have been classified into no-clean and solvent-clean categories. Solvent cleaning consists of two types: aqueous cleaning and non-aqueous cleaning fluxes. The no-clean flux provides the necessary chemical activity to sequester stannous oxide. The fact that the flux does not need cleaning does not mean there are no residues. Residues of the flux reaction products may indeed be present, but they satisfy insulation resistance requirements so the flux residues are not detrimental to the reliability of assembled products in temperature, humidity and bias testing. However, if they form a barrier to interfacial adhesion of underfill in subsequent processing, they may introduce additional concerns in other environmental stress testing for reliability. Therefore, the flux residues may need to be cleaned if possible. The alternative is to use a solvent-clean flux. For eutectic PbSn solder and many Pb-Free solders, water-soluble fluxes are preferred since their residues may be removed by de-ionized water rinsing at elevated temperatures or by aqueous solutions of surfactants or saponifiers washing and de-ionized water rinsing at elevated temperatures. The water-soluble flux is principally used in manufacturing and consists of an organic acid, surfactant, and a vehicle such as an alcohol based compound. It is preferable that the flux has a tacky nature to provide and maintain proper solder bump to pre-solder alignment. There are a variety of ways to apply flux for chip joining to a laminate chip carrier. The bumps of the chip can be dipped in flux, placed on the chip carrier and reflowed. Alternatively, flux can be dispensed or sprayed on the laminate chip carrier; the chip placed on the pre-solder pads of the laminate chip carrier and then reflowed. Finally, a combination of dip, dispense or spray may also be employed. In the case of dipping, at least 50% of the bump should be coated with flux. In the case of the spray or dispensed flux on the laminate chip carrier, the complete chip footprint should be covered and the amount applied should be verified by weight. Time from

dispense of the flux until reflow should be minimized to avoid excess contact time regardless of the flux used. Once flux application and reflow are completed using water-soluble flux, the flux residues must be removed within a limited process time window. The flux residues with water-soluble flux would be reactive and somewhat corrosive if left in contact indefinitely with the device joined to the laminate chip carrier. Various types of cleaning may be used including aqueous immersion and spraying. The cleaning action of spray is particularly amenable to inline processing through wash, rinse and drying stages. Spray nozzle angle, pressure, temperature, and conveyor belt speed are all key parameters in setting up the cleaning profile. Other key mechanical parameters are the gap between chip device and laminate chip carrier, the size of chip and laminate chip carrier, and the pitch and density of solder interconnections.

Reflow Soldering, Thermo-compression Bonding

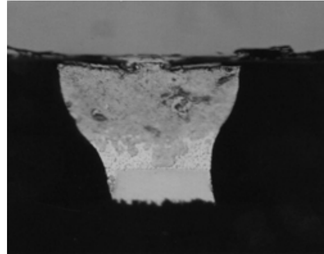
There are a variety of ways to connect conductive bumps electrically to laminate chip carriers. When solder bumping is employed on the device, solder reflow interconnection is often used. The purpose of solder reflow is to melt solder and to allow metallurgical reaction with tin and other constituents of the solder to form modest controlled amounts of intermetallic compounds to establish a solder joint with the laminate chip carrier. In order to carry out the solder reflow a thermal profile must be established; raising the temperature above the melting points of the solder bump and any pre-solder present on the laminate chip carrier. A time above liquidus is routinely established in the range of 40 to 220 seconds or longer. A range of peak temperature is established depending on solder type. For PbSn eutectic solders this peak temperature can range from 195 C to 250 C. For Pb-free solder the peak temperature can range from 230 C to as high as 260 C. Such thermal profiles are usually established by a thermocouple placed in the center of a chip footprint between the chip and the laminate chip carrier. Generally, a forced convection nitrogen oven is used although other furnace types such as infrared furnace and others may be used. Prior to chip joining a variety of perimeter visual inspections are performed when the device is placed on the laminate chip carrier. Rotational and x-y alignment are grouped as chip skew and are important for proper chip joining. After chip join reflow, additional perimeter visual inspections are performed. Chip skew is checked once again to verify that mechanical motion and vibration have not disturbed the initial bump alignment. Non contact of a solder bump with solder on the laminate chip pad can occur, particularly in the

perimeter and corner locations of the device. This is highly dependent on product configuration such as chip size, chip construction, laminate carrier size as well as appropriate set-up parameters for inspection, e.g., lighting or fixturing. Non-wetting joints are produced during the reflow when two solder surfaces come in contact, but due to a variety of factors may not be successfully joined together. Potential causes of non-wet joins include foreign materials or contamination on the joining surfaces, intractable oxides or inadequate flux on the chip bump or laminate pad, or laminate warpage in the chip site, or placement damage of a cracked device or tilted chip on the chip carrier. Non-wetting joints can be not only a yield detractor, but occasionally will form contact opens which may be missed in the final test and can fail in the field. A few examples of solder joints formed in FCPBGA packages are shown in Figure 10.

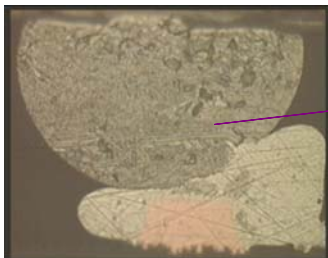
As the visual inspection can only inspect the perimeter rows and maybe the second row of the solder joint array, nondestructive process control is commonly employed, such as X-ray and ultrasonic techniques. X-ray can sometimes be used, but resolving fine pitch solder joints can be challenging. Destructive analysis such as chip pull test is often performed to verify the integrity of solder joints. Taffy pull separation with PbSn solder is acceptable. For Pb-free solders, various failure modes in chip pull tests are observed; taffy pull in solder, interfacial separation at the intermetallics, via separation in the chip device, UBM metal separation, or solder separation from the UBM. Chip pull test can be used to confirm non-contact failures in solder joints. However, due to the variety of separation modes with Pb-free solder joints, the tensile force data collected from chip pull test may not be consistent indicators.

Figure 10. Examples of flip-chip solder joints in FCPBGA packages.

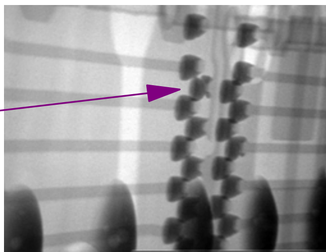
FCPBGA Chip Attach Solder Joint Examples



Good Solder Joint



Non Wet Solder Joint



Transmission X-ray of Defective Solder Joint

(W.E. Bernier & F Pompeo, "IC FCPBGA Packaging: A Tutorial", presented at Georgia Institute of Technology Packaging Research Center, Atlanta, GA, Sept,18, 2007)

Thermo-compression bonding is an alternate technique for joining bumped-chip devices to laminate chip carriers. It provides a combination of temperature and pressure over a specified duration of time to form solder joints. Techniques such as Tape Automated Bonding (TAB), anisotropic conductive adhesives reviewed earlier as well as isotropic conductive adhesive bonding, and wafer-level underfill device bonding all may use such a method. The combination of time and temperature provides the necessary energy to bond bumps to pads using appropriate joining metals (TAB), to promote chemical reaction and mechanical interlock (anisotropic conductive adhesive), to facilitate thermoplastic and thermosetting reactions (isotropic conductive adhesive), or to complete solder joining, flow and cure of underfill for wafer level underfill.

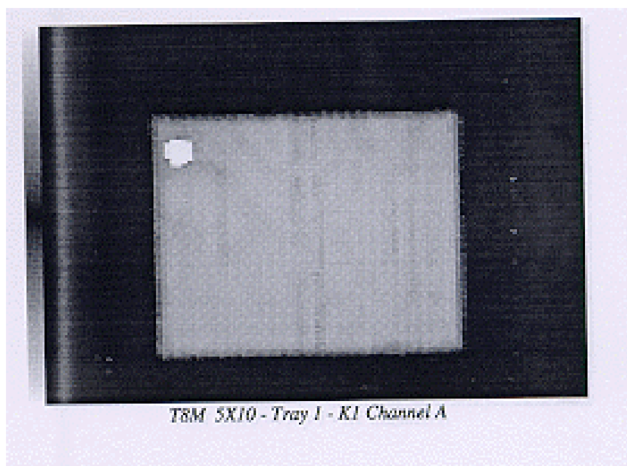
Underfill and Over-mold

Careful selection of underfill encapsulant is important to maintain the integrity of the chip joint through mechanical handling and to minimize stresses associated with circuit package processing. Underfill encapsulation process consists of three stages: pretreatment, dispense, and cure. In pretreatment, the laminate chip carrier is subjected to a moisture bake out to minimize the residual content during processing and cure. Often the bake out is performed in nitrogen atmosphere to prevent oxidation of metal surfaces, particularly copper metal surfaces. Surface adhesion enhancements may be applied to key interfaces to promote underfill adhesion to the laminate chip carrier solder mask, chip passivation, and chip device sides and edges. The interfacial adhesion is particularly critical at the corners and perimeter of the device where mechanical stresses tend to be highest. The dispense pass requires control of the underfill encapsulant shot size customized to the chip dimensions. Bias heating of the laminate chip carrier and the underfill encapsulant is commonly used, and once again this is customized to both the chip device and the laminate chip carrier to promote the capillary flow of encapsulant. Various fill dispense patterns can be used such as a dot, line, of "L" pattern for optimum throughput while minimizing void occurrence. The dot fill consists of a single dot of material placed next to the chip and after a control time to allow for capillary flow another identical dot of material is placed in exactly the same place in the same manner. This sequence is repeated as necessary until the underfill encapsulant flows out from underneath all sides of the chip. This must occur before dispensing the fillet pass. In line dispense, the encapsulant is dispensed once along the long side of the chip device. The material must flow underneath the chip through to all four sides prior to dispensing the fillet pass. In the "L–shaped" dispense, a continuous line dispense is performed along a long side and a short side of the chip device. Once again the underfill encapsulant must flow underneath the chip through all sides prior to the dispensing the fillet pass. With each dispense procedure the two key factors in consideration are the throughput and void population, which must be optimized for fastest throughput and highest yield. After under-chip dispense is completed, a final fillet pass is performed to provide adequate protection for edge and corner, high mechanical stress areas as determined by fillet height and shape requirements for the particular application. Normally the final fillet dispense avoids the areas involved in the initial fill dispense areas. The final stage is to cure the underfill

encapsulant. The cure profile is established to achieve full underfill polymerization for proper time and temperature. The final cure temperature is also selected to minimize the induced warpage of the cured assembly at room temperature. By monitoring chip bending after cure and room temperature stabilization, the highest level of bending in the assembly is known to occur during the cure processing, and it is particularly high for Pb-free solders.

After the three process stages are complete, there is customarily post underfill encapsulation inspection. Visual criteria typically specify that a continuous fillet must be present around the chip device. The height of the fillet must meet minimum coverage of the chip height at the midpoints of the side. The fillet may be lower at the chip corners, but the lower portion of chip corners must not be exposed. The fillet extends from the edge of the chip to the minimum geometry onto the laminate surface. Underfill material on the back of the chip is allowed, provided it does not interfere with lid bond line requirements. Missing fillets are not allowed. Bubbles in the fillet that exposed on the laminate or chip surface or sides are not allowed. The maximum size of any bubbles should be limited regardless of whether the laminate or chip is covered. No foreign material may be embedded in the cured underfill material. No vertical corner cracks are allowed in the underfill fillet. Horizontal edge cracks may be allowed depending on application requirements. A non-destructive inspection by CSAM (Computerized Scanning Acoustic Microscopy) is routinely performed to confirm the void criteria under the chip and others. Figure 11 highlights a large void in the underfill to chip device passivation interface which would fail typical inspection criteria. Figure 12 shows extensive delamination at the underfill to solder mask interface of the laminate chip carrier.

Figure 11. Underfill void found with CSAM. Underfill encapsulant voids can be caused by dispense processing, dispense pattern, and surface contamination.



(W.E. Bernier, “Flip Chip PBGA Assembly – Quality and Reliability Challenges”, presented at IMAPS Upstate NY and Garden State Chapter Fall 2008 Packaging Symposium, Endicott, NY, Oct. 2, 2008)

Figure 12. Delamination between underfill and solder mask found with CSAM. Delamination can be caused by underfill cure problems and surface contamination

(W.E. Bernier, “Flip Chip PBGA Assembly – Quality and Reliability Challenges”, presented at IMAPS Upstate NY and Garden State Chapter Fall 2008 Packaging Symposium, Endicott, NY, Oct. 2, 2008)

Over-mold processing consists of two general techniques: dispensed dam and fill material, and injection molding processing. Similar stages of processing are used for over-mold processing as for underfill encapsulation: pretreatment, dispense, and cure. Pretreatment requires laminate chip carrier bake out often in nitrogen environment to remove residual moisture. In the dam and fill dispense technique the under-chip dispense has already been completed. A high viscosity dam material is dispensed at the outline of the over-mold area. A separate lower viscosity fill material is then dispensed within the dam outline to fill the volume to adequate height in order to meet application requirements. Bias heating may be used for the laminate chip carrier as well as the dispensed dam and fill materials. Cure of the dispense materials is usually performed together. Injection mold processing requires special tooling to generate a mold representing the desired shape and size of the over-mold area. The over-mold material is injected into the mold to fill the mold cavity. The over-mold resin is then cured at controlled time, temperature and pressure to yield an encapsulated chip device with low warpage. As with underfill encapsulation, similar care must be exercised in set up and dispense so yield issues with voids do not occur.

Quality Assurance Methodologies

Several examples of typical quality assurance stress tests are listed in Table 1. These tests are industry standard procedures commonly used for qualification of FCPBGA applications. Normally, there are initial pre-conditioning tests including moisture soak and exposures to three reflow cycles. After this base test, other stress tests are performed such as thermal cycling, temperature / humidity / bias testing, extended temperature storage testing, shock and vibration testing, and tin whisker testing for new Pb-free solders. Various failure modes may result from these tests if the technology is not adequately robust. These failure modes include solder joint cracking, device cracking; solder bridging, electrical shorting due to electromigration, and others.

Table 1. Typical standardized stress testing performed for qualification

TEST	CONDITIONS	SPECIFICATION	DURATION	Note
Temp/Humidity/Bias	85 C / 85% RH / 3.6 V	JEDEC A101	1000 hours	1
Deep Thermal Cycle	-55 C to 125 C	JESD22-A104-B	700 cycles	1
Thermal Cycle	-25 C to 125 C	JESD22-A104-B	1000 cycles	1
Thermal Cycle	0 C to 100 C	JESD22-A104-B	3000 cycles	1
Power Cycle	25C to 125 C	JEDEC Draft	1000 cycles	1
Card Level Shock	100g, 200g, 340 g	JESD22-B-110	2/1.5/1.2 ms	1
Low Temp Storage	-65 C	JESD22-A119	1000 hours	1
High Temp Storage	150 C	JESD22-A103-C	1000 hours	1
Highly Accelerated Stress Test (HAST)	130 C / 85% RH / 3.6 V	JEDEC A110-B	96 hours	1
Vibration on Card	1.04G, 0 – 500 Hz, 3 axis	MIL STD 810F	3 hours	1
Electromigration	150 C / 0.7A	JEDEC Draft	2000 hours	1
Thermal Cycle (Sn Whisker)	-55 C to 85 C	JESD22A121.01	1500 cycles	1
Temp & Humidity (Sn Whisker)	60 C / 87% RH	JESD22A121.01	4000 hours	1

Note 1: JESD22-A113D Level 3 or 4 preconditioning is done prior to testing

(W.E. Bernier, “Flip Chip PBGA Assembly – Quality and Reliability Challenges”, presented at IMAPS Upstate NY and Garden State Chapter Fall 2008 Packaging Symposium, Endicott, NY, Oct. 2, 2008)

4.3. C4NP Technology

Controlled Collapse Chip Connection – New Process (C4NP) technology is a novel solder bumping technology developed by IBM [18-23] to address the limitations of existing wafer bumping technologies. Through continuous improvements in processes, materials and defect control, C4NP technology has been successfully implemented in the manufacturing of 300mm Pb-free solder bumped wafers. Both 200 and 150μm-pitch products have been qualified and are in volume production. Extendibility of C4NP to 50 μm-fine-pitch microbump application has been demonstrated with the existing C4NP manufacturing tools. Target applications for microbumps are three-dimensional (3D) chip integration and the conversion of memory wafers from wire bonding (WB) to C4 bumping.

C4NP Wafer Bumping Processes

C4NP process starts with the fabrication of a glass mold, as shown in the SEM image of Figure 13, in which the I/O pads of UBM of an entire wafer is replicated as a mirror image of tiny cavities etched into the glass plate. These cavities are filled with solder as the mold is scanned beneath a fill head, as shown in Figure 14. The fill head contains a reservoir of molten solder and a slot through which the solder is injected into the mold cavities. The cavity depth and diameter determine the volume of each solder bump that will be subsequently transferred to the wafer. The filled mold is inspected automatically and then aligned below a wafer with exposed UBM pads facing the mold. Mold and wafer are heated above the solder melting point in formic acid vapor to activate the UBM pads and solder surface, and then they are brought into contact. The solder forms spherical balls which transfer from the mold to the UBM pads on the wafer, where they wet and solidify. Subsequently, the wafer and mold are separated, and the mold is cleaned for reuse. Fig. 15 describes this process flow.

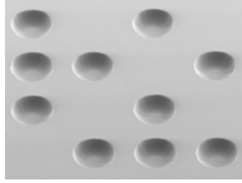


Figure 13. C4NP glass mold with etched cavities [18].

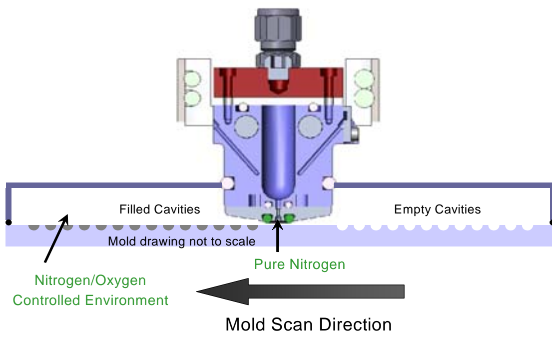


Figure 14. Scan fill head to inject molten solder into cavities of glass mold [18].

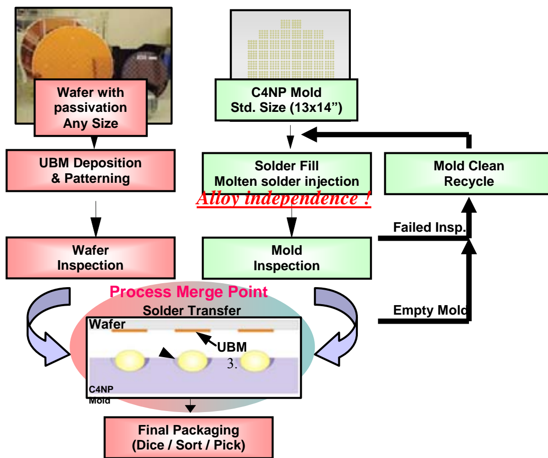


Figure 15. C4NP process flow [18].

Mold Fabrication and Solder Transfer to Wafer

C4NP mold is made of borofloat glass, which has a CTE closely matched to silicon. Photolithographically defined pattern is used to create the cavities by wet etching. The molds are scanned beneath a solder injection head (in Fig. 14) which fills the cavities with molten solder precisely to the top surface of the mold. Therefore, the solder volume transferred to the wafer at contact is a direct function of the glass cavity volume. The processes of the solder fill, auto inspection, solder transfer and cleaning are automated using Mold Fill, Mold Inspection, Solder Transfer and Mold Cleaning tools. The solders chosen for wafer bumping usually do not wet to the glass mold, so upon heating, the solder alloys form spherical balls in the cavities, as described in Figure 16. The reflowed balls protrude above the surface of the mold by 10 – 20 um depending on ball size and cavity. Note from Figure 16 that the balls are not uniformly formed at the center of the mold cavity. The alignment of the mold cavities to the corresponding UBM pads is sufficient to assure that the solder wets to the correct UBM pads.

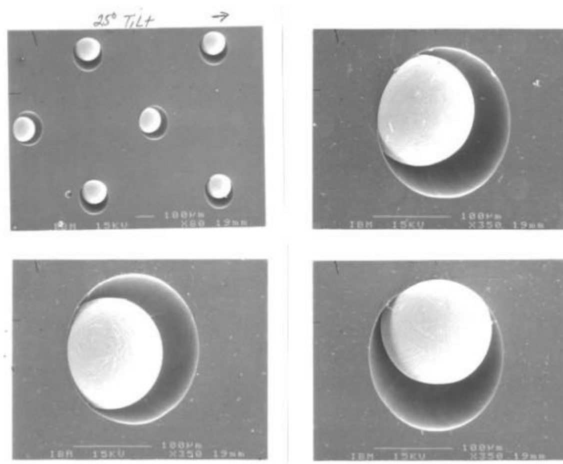


Figure 16. Reflowed solder spheres in glass mold cavities prior to transfer to wafer [22].

The filled molds are aligned with the wafer as shown in Figure 15. After alignment, the mold and wafer are heated and are brought into close proximity/contact, allowing the molten solder balls to wet to the appropriate UBM pads where they preferentially remain when the wafer and mold are separated.

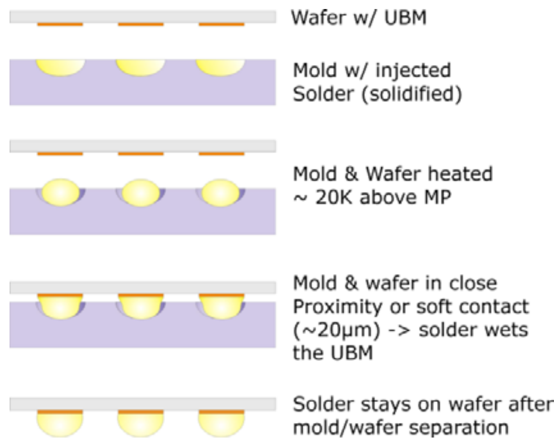


Figure 17. Solder transfer process sequence [20].

For the 200, 150 and down to 50 µm pitch applications [21, 23], as-received glass molds have been successfully used for mold fill and wafer transfer. For further extension to very fine pitch applications, < 50 µm, where solder volume becomes extremely small, to ensure a successful solder transfer, the flatness of the glass surface needs to be improved. And a technique to increase the depth and sidewall angle of mold cavities is essential to maximize the solder stand-off height above the glass surface that would overcome a local non-flatness.

Wafer Bumping Yield Improvements

C4NP bumping yield has improved significantly to meet manufacturing yield requirements. Defect root cause analysis has resulted in process improvements in patterning the UBM pads, as well as in the mold and mold fill areas which contributed to robust yield improvements. Fig. 18 illustrates the significant yield improvement over the years. [20] The yield data is derived from RVSI inspection of the 200 µm pitch product wafers. Yield learning model showed a 15% defect reduction per month since the start of the C4NP program. Initially, the major yield detractor was contamination. With the installation HVM tools with FOUP to FOUP automatic handling and tightened cleanliness control, this type of defects was mostly

eliminated. Also, as the quality of glass mold and mold fill processes improve, a significant reduction in missing C4s, along with improvements in volume uniformity and co-planarity, has contributed to improvements in transfer yield.

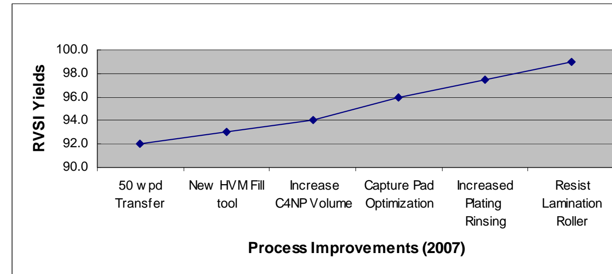


Figure 18. Process improvement, start of manufacturing. (Best Wafers = 100% yield) [20, 21]

All these improvements have resulted in excellent bumping yield for both the 200 and 150 μm pitch applications. Best wafers have consistently achieved 100% yield. The feasibility for 50 μm pitch wafer bumping was successfully demonstrated in the same manufacturing environment using the same set of C4NP tools for mold fill and wafer transfer [23]. The mold inspection tool (MIT) which works well for the 150 to 200 μm pitch was unable to handle the high density bumps (~11,000 bumps per chip at 50 μm pitch) due to lack of pixel density. Using an improved inspection tool developed by RVSI, very high bumping yield was demonstrated. The good results were largely attributed to improvements in the volume uniformity of mold cavities, eliminating contaminations and using pure nitrogen in the fill environment.

Figure 19 compares mold filling under N_2/O_2 ambient (Fig. 19(a)) to that under pure N_2 (Fig.19(b)). More solder bridging defects between adjacent cavities are observed under N_2/O_2 mixture environment, while bridging is mostly eliminated in N_2 ambient. Solder bridging for standard C4s (pitch ≥150μm) does not require special care because the spacing between adjacent cavities is longer. However, bridging is much more sensitive to micro-bumps because of shorter spacing between cavities.

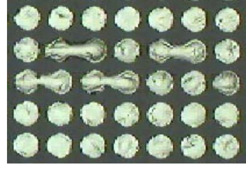


Fig. 19(a) Mold fill in O_2/N_2 mixture gas [21, 23].

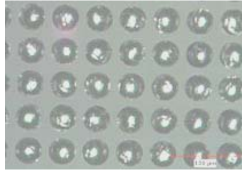


Fig. 19(b) Mold filled in Pure N_2 [21, 23].

With the high-yield molds, micro-bumps were successfully transferred from glass molds to both 200 and 300mm wafers which were patterned with a three-layer UBM, as shown in Figs. 20. With the aid of formic acid vapor flux, excellent wetting was achieved for the SnAg solder micro-bumps. The UBM pads are ~ 28µm in diameter. An additional reflow was performed to reshape the micro-bumps and uniform bump heights were obtained. Excellent height uniformity was achieved for the transferred microbumps (co-planarity < 2 µm). The preliminary results suggest that C4NP technology can be well scaled down to 50 µm to meet ever increasing demand on the I/O density.

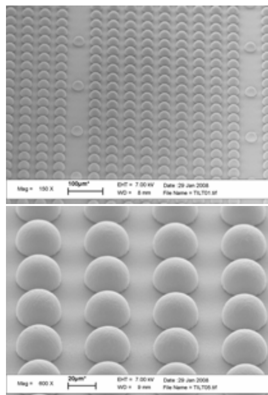


Fig. 20. SEM images of 50 µm microbumps [23].

C4NP Advantages: Alloy Flexibility

For C4NP technology changing solder alloys for wafer bumping is a simple operation. It is accomplished by changing the fill head in the mold fill tool, which is usually done in less than an hour. The process temperatures of the solder reservoir and the mold can be adjusted to accommodate a particular solder alloy. This flexibility allows C4NP to be backward compatible with existing solder alloys and UBM stacks as well as to enable the use of any multi-component new solder alloys and UBM stacks. As discussed later in the section of Pb-free solders, “dopants” can be added to Sn-rich solders to improve EM performance, suppress Kirdendall voiding, reduce copper pad consumption, suppress Sn pest, etc. The ability to maintain alloy flexibility with precisely controlled solder composition and alloy doping is critically important to deliver enhanced performance and reliability. The advantages of having alloy flexibility are described in the other sections.

4.4. Fabrication of Cu Pillar Bumps

Cu pillar bumps have been introduced as an alternative to the conventional collapsible solder bumps for first level flip chip interconnections [15-17, 24]. The structure and production process of a pillar bump are analogous to an electroplated solder bump. The fabrication requires the integration of the photolithography and electroplating processes. A thin metal seed layer is first blanket-sputtered on the passivation surface and pads of the BEOL structure on a silicon wafer. It consists of an adhesion layer, normally Ti or TiW, and a Cu seed layer serving as a conducting layer for plating. A thick photo-resist material is spin-coated over the Cu seed layer, normally with a thickness range of 40 to 100 microns. After exposure and development, the opening cavities with the Cu seed layer at the bottom are electroplated with Cu. A solder cap can be optionally plated on top of the pillar and subsequently reflowed to form a solder bump or cap. Resist stripping is performed in an environmentally friendly solvent system. For the electroplating process, the photo-resist profile, plating durability, and strip ability after plating are important considerations. Cu pillar bumps can be fabricated over a variety of spacing on a Cu-seed layer. Figure 21 is schematic drawings of a conventional solder bump (a), and a copper pillar with solder cap (b) [25]. Figure 22 shows the full array of pillars arrayed at different spacing.

The copper pillar bump is an emerging technology as an option for high performance packaging since it offers fine pitch capabilities and has good electromigration performance. Some concerns of copper pillars on chip include a high risk of chip-to-package interaction (CPI) with ultra low-k dielectrics and a relatively high cost. The significant improvement in EM performance has been demonstrated [26-29]. Figure 23 shows a SEM image of a Cu pillar bump on Intel's Presler processor [30]. The stiff, non-deformable nature of Cu bumps requires a significantly engineered BEOL structure to mitigate the high stress applied to the ultra low-k layer.

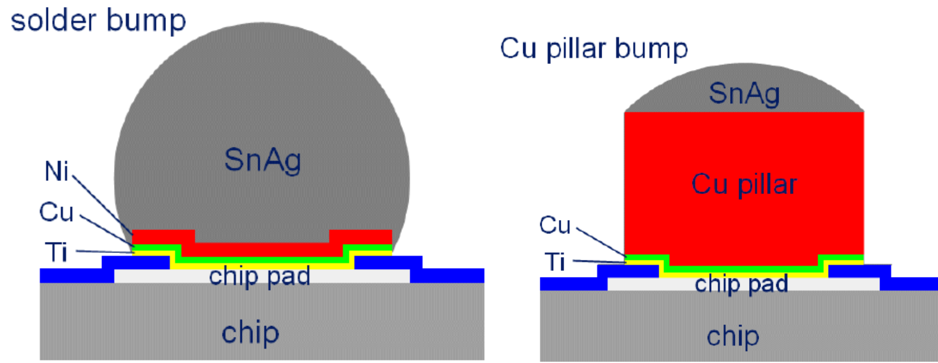
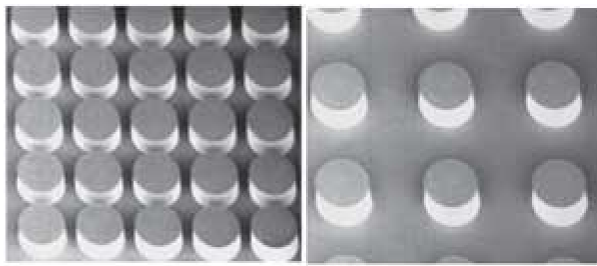


Figure 21. Schematic drawing of a conventional solder bump (a), and a copper pillar with solder cap [25].



(a) *(b)*

Figure 22. Examples of Cu pillars at 50 micron pitch with (a) 12.5 miron spacing and (b) 50 micron spacing [16].

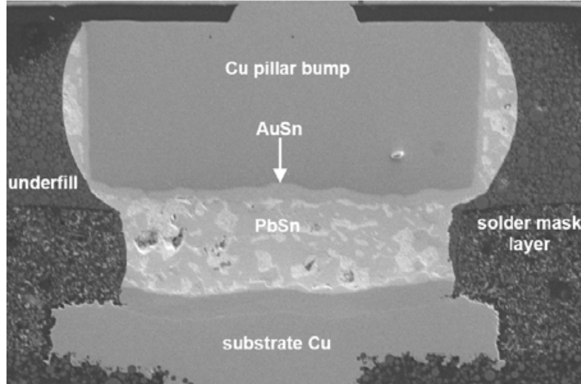


Figure 23. SEM image of a Cu pillar bump on Intel's Presler processor [26]].

4.5. Substrate Bumping Technologies

In the assembly of a chip to an organic laminate substrate, solder interconnects are formed by reflowing both solder bumps on the chip and pre-solder bumps on the substrate. The per-solder bumps on the substrate are needed to compensate the variations in the solder bump height on chip as well as the laminate substrate warpage. This is particularly critical for large chips with fine-pitch bumps. To improve the bump co-planarity on substrate, a coining process is usually applied to form flat tops on the solder bumps on a substrate [31].

There are several solder bump forming methods developed for substrate pre-soldering. The most popular manufacturing technology for forming solder bumps on organic substrates is the solder paste stencil printing method [32-34]. Solder paste, typically consisting of about 50% of flux, is printed onto surface finishing pads on a laminate substrate through a patterned stencil mask. After stencil removal, the substrate is heated to melt the solder paste to form bumps, and then coined to make flat tops. This method is simple and low cost, since it does not require using a photo-lithography process. However, it can not be easily extended to high density interconnects having less than a 150 μm pitch. In the fine-pitch application, the flux tends to bridge after paste screening, which would cause a high defect rate of solder bridging after reflow. In addition, due to the significant volume reduction after reflow, the void population and bump height variation could be significant and, consequently affect die attachment yields negatively. The process steps describing the solder paste stencil printing method is schematically shown in Figure 24 [35]. Stencil paste screening method has the advantage of one step solder bumping of different size solder resist openings on the same substrate by screen-printing different amount of solder paste on the stencil mask openings on the correspondingly mask holes. Due to the large height variation of the paste screened and reflowed bumps on substrate, a coining process is used to guarantee the co-planarity of all the solder bumps for higher assembly yield [31]. A substrate solder bump after the coining process is shown in Figure 25. The process also offers alloy flexibility. Practically any solder alloys can be fabricated into the preformed solder spheres before mixing with the flux to form the paste.

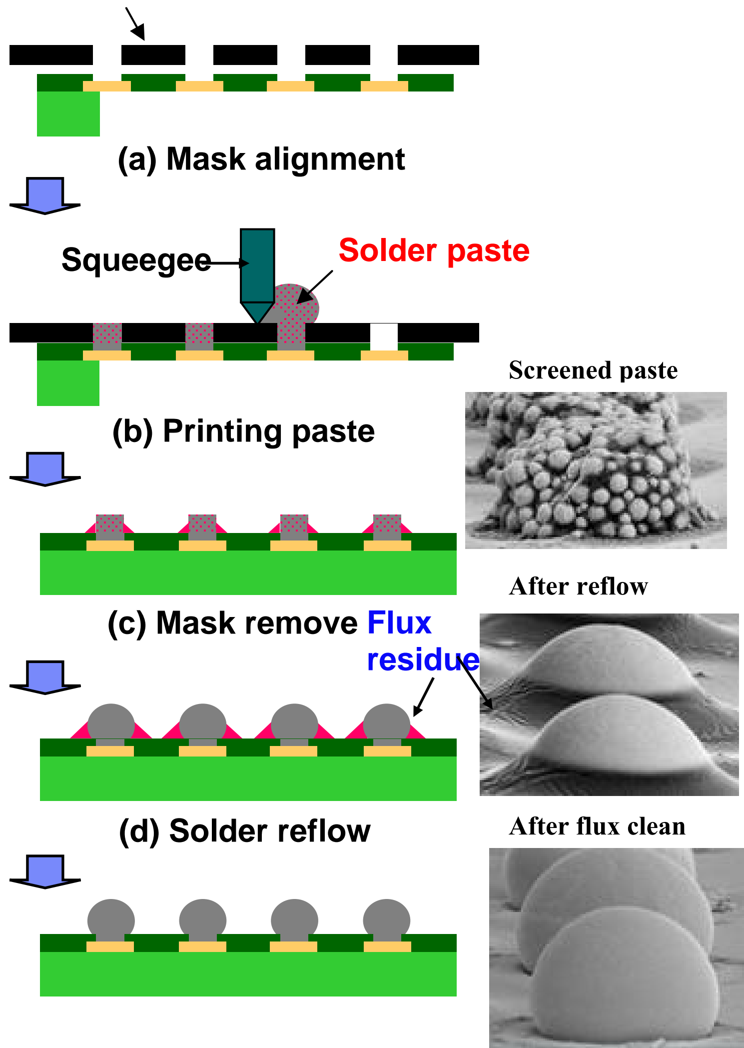


Figure 24. Solder paste stencil printing processes. [35]

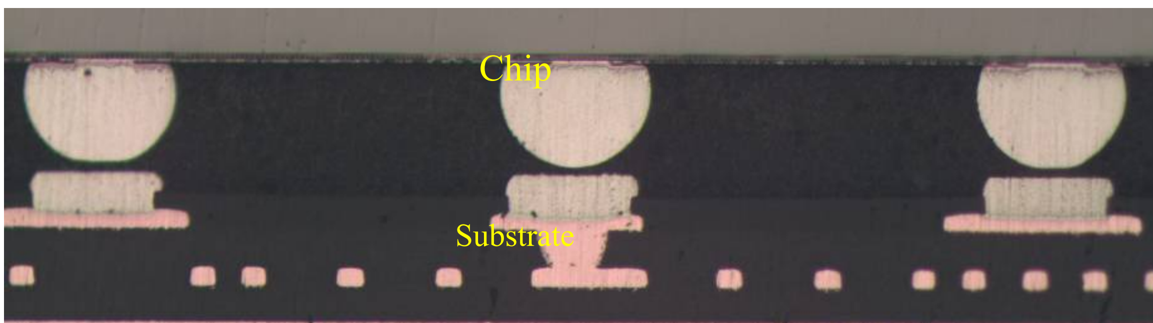


Figure 25. A coining process was used to guarantee the co-planarity of height of all bumps on substrtae within a tight range. [36]

Recently, new solder bumping techniques have been developed to address the ever growing demands for fine pitch and the reduction of solder bump and solder resist opening (SRO) sizes, such as pitches down to 120 microns and SRO sizes of about 60 to 70 microns. One method involves the placement of pre-fabricated micro spheres or micro balls of solder onto substrate pads. Several solder ball placement methods have been developed [36-40]. According to one method, solder balls are sucked into a jig by vacuum suction, and then mounted onto flux-coated pads on substrate. Another micro ball placement method involves the use of a stencil mask [39-40]. In the later method, thick tacky flux is first printed through a stencil mask onto the substrate pads. Solder balls of a uniform size are dispensed onto a second stencil mask with holes aligned with the substrate pads. A squeeze brush is then used to disperse the balls and press them into the mask holes. The balls transfer and stick to the tacky flux which was previously screened on the pads. The stencil mask is removed after ball placement and then heated and melted to form bumps. Figure 26 describes the ball placement method and processes. This method, however, does not have the flexibility of the placement of different size balls on matching pads with different solder resist openings. It generally requires an additional mask process for placement of different size solder spheres or use paste screening method. The micro ball placement method eliminates the volume reduction problem by using preformed solder balls and tacky flux in separate mask processes, as shown in Figure 27. [41].

Micro-ball mounting method can form higher volume solder bumps and could be applied to finer pitch substrates than the stencil printing method. However, the micro-ball mounting processes are more complicated as compared to the stencil printing method. Three masking processes and alignments are needed, respectively, for tacky flux dispensing, micro-ball "brushing" placement on C4 pads, and paste dispensing for the larger capacitor pads [41]. Also, the cost of preformed solder balls significantly increases with size reduction for fine-pitch application. Micro-ball mounting method still has limitation in maximum volume of solder bumps at a given pitch even though it can provide higher solder volume than the stencil printing method. Extendibility to very fine pitch application is difficult because of the fluxing process and handling of very small balls. In addition, the micro-ball mounting method can not handle multiple size pad openings because the same size balls must be used at each mask process. The

co-planarity of solder bump height will degrade if one size solder balls are dispensed on different size pads.

Recently, Intel has integrated Cu pillar bumps on chip UBM using Cu electroplating process in high volume manufacturing and showed reliability benefits on electromigration and thermal conduction [29]. The Cu pillar bumps have flat tops which are different from round tops in the case of solder die bumps. The Cu pillar bumps need round tops of substrate solder bumps to avoid the formation of voids at the Cu/solder interface during flip chip assembly process. The round top solder bumps provide by the micro ball placement method have worse bump co-planarity than the coined flat top solder bumps. Therefore, the round top solder bumps on substrate side need higher volume for flip chip assembly with Cu pillar bumps for high assembly yield.

IBM has recently developed and qualified the C4NP wafer bumping technology for the manufacturing of all Pb-free solder 300 mm wafers at very fine pitch. Feasibility of wafer bumping of 50 μm pitch, on both 200 and 300 mm, has been demonstrated with excellent yield [18, 21]. The new wafer bumping method is extended to substrate bumping, where molten solders are directly injected on substrates pads by using a flexible mask. [41]

The new substrate bumping technique, the Injection Molten Solder (IMS) technology, is shown in Figure 28 using a patterned polyimide decal. First, the holes in the polyimide (PI) mask are aligned to the pads on the substrate. Using an optimized combination of pressure and temperature, molten solder is injected into the aligned holes and fills both the solder resist openings and holes in the mask. In this step, through careful control of the fill environment in low oxygen, neither flux nor formic acid is needed. After the molten solder has wetted and solidified on the pads, the PI mask is separated from the substrate.

The flexible PI mask follows the non-flat surface contour of the laminate substrate by enabling intimate contact between the mask and substrate to prevent solder bridging. The holes in the mask have tapered angle to facilitate mask separation after solder solidification that increases the reusability of the mask.

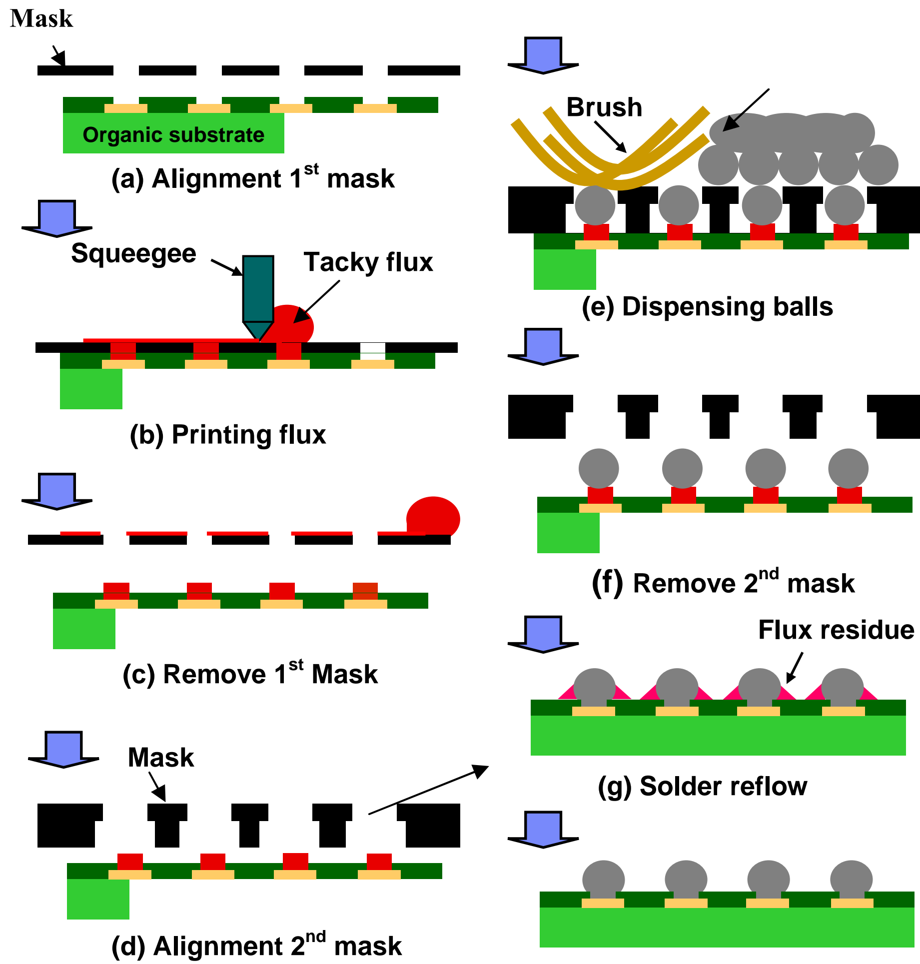


Figure 26. The micro balls placement processes. [35]

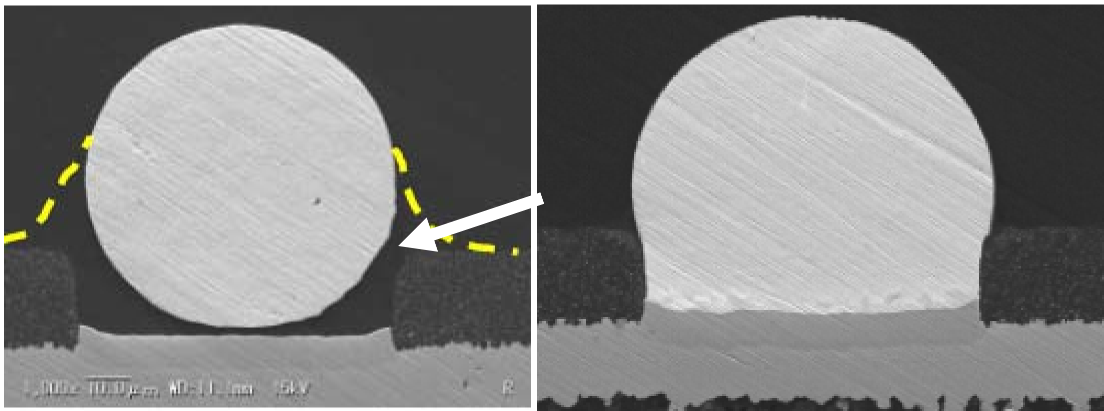


Figure 27. The micro ball placement method; (a) after ball mount, and (b) after reflow.

While the IMS process is very simple and similar to the stencil printing method, the advantage of IMS over the paste process is that it can make higher volume solder bumps for fine-pitch application due to the use of pure molten solder. The solidified solder bumps have column shape and round tops as shown in Figure 29. The shape of the solder bump mimics the hole shape in the flexible mask. Solder volume can be easily changed by the changing of mask thickness or hole size. Any types of solder alloy can be used with no increase in materials cost when applied to very fine pitch applications. Figures 29 and 30 show the side views and cross-sectional images of IMS bumped Cu OSP and ENIG Au finished substrates, respectively. The cross-sectional images show that the IMS bumps have good interfacial microstructures and tight co-planarity on both surface finishes.

Another key advantage of IMS bumping is that IMS makes different solder volumes in a single pass and still maintains good co-planarity when the substrate has different sizes of resist openings, including the large capacitor pads. The technology allows the design flexibility of applying larger volume interconnects for power joints and smaller volume interconnects for signal to meet both performance and reliability requirements. Currently, the method has demonstrated the full area array bumping capability at 80 micron pitch with excellent bum height uniformity. Figure 31 shows a side view of an array of bumps at 100 micron pitch.

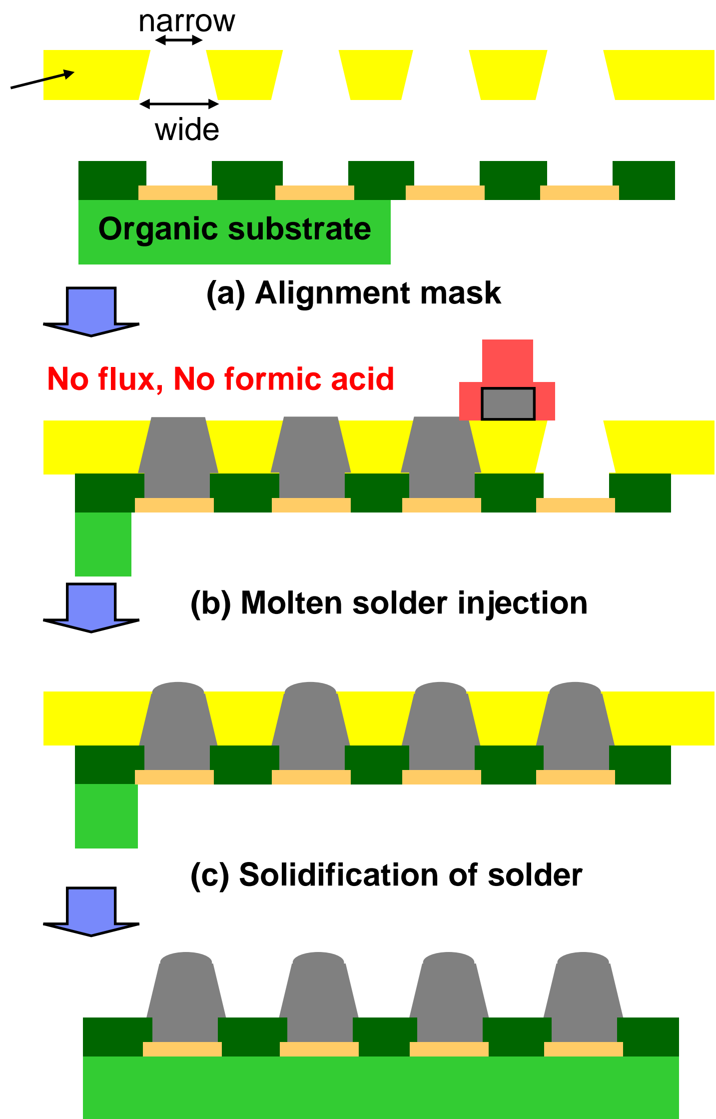


Figure 28. Injection Molded Solder processes [41].

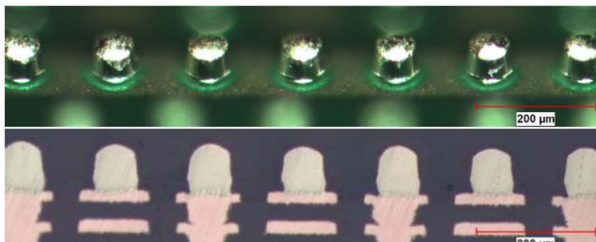


Figure 29. Side and cross-sectional views of IMS bumps on ENIG Ni/Au pads [41].

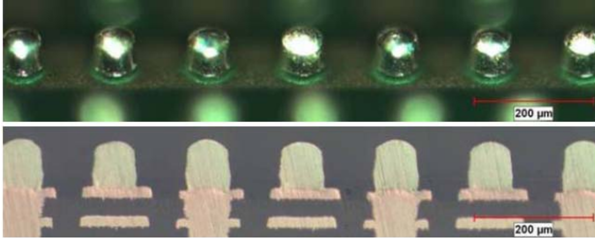


Figure 30. Side and cross-sectional views of IMS bumps on Cu OSP surface finish [41].

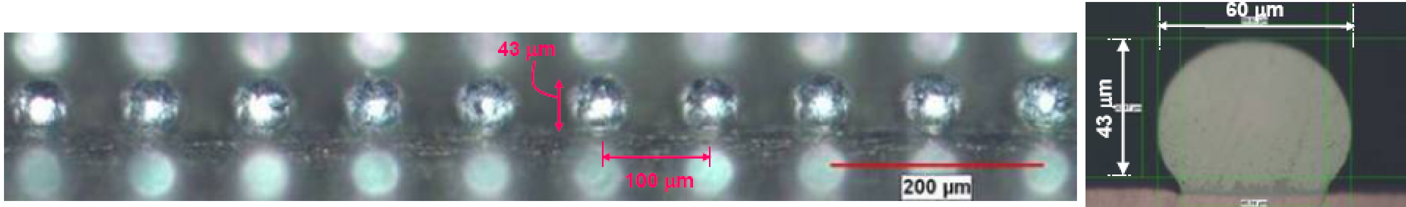


Figure 31. Side view and cross sectional image of IMS bumps on 100 µm pitch substrates [41].

4.6. Pb-free Solders for Flip Chip Applications

Since July, 2006, following the EU's RoHS legislation [42-44], the consumer electronics industry has been offering "green" products by eliminating Pb-containing solders and other toxic materials. This transition has been relatively smooth, because the reliability requirements are less stringent. However, the Pb-free transition for high performance electronic systems (such as servers and telecommunication) is still on-going due to their rigorous reliability requirements. Recognizing this situation, EU has extended the Pb-free exemption date for high performance electronic systems by the end of 2014. The research and development efforts to implement Pb-free flip chip interconnections for high end applications are still very active. A key technical element in implementing Pb-free, flip-chip interconnection is the wafer bumping technology. One new wafer bumping process, C4NP (C4 new process) for Pb-free solders is discussed in this Chapter, while other wafer bumping technologies are covered in Chapter 3.

Pb-free solders in use are listed with their melting point, applications and concerns in Table 2. Two major Pb-containing solders used for flip chip applications, eutectic 63Sn-37Pb and 97Pb-3Sn, are also included in Table I. Pb-free solders used in consumer electronics are mainly applied by paste screen printing, ball mounting or electroplating method, while Pb-free solders for high-end flip chip applications are applied by either electroplating or C4NP technology.

In the early stage of development, many Pb-free solders have been evaluated for flip chip applications [9, 32, 45]. The near-ternary eutectic Sn-Ag-Cu (SAC) solder commonly used in printed circuit board (PCB) assembly, such as BGA or SMT solder joints is not readily accepted for flip-chip applications. This is largely due to several challenging issues, such as difficulty of electroplating a ternary composition, formation of large intermetallic plates of Ag_3Sn in near-ternary SAC, or yielding high modulus or stiff solder joints, and other concerns. To mitigate these concerns, the usage of Sn-Ag or Sn-Cu binary systems with a low Ag or Cu content, was proposed to obtain low modulus or more ductile flip-chip interconnections [46, 47]. However, reducing the alloying content in the binary and ternary Sn-based solders can significantly alter their microstructure, melting point, and consequently their mechanical or other properties.

Table 2. Examples of Some Pb-Free Candidate Solders and Pb-Containing Solders

Composition (wt %)	Melting point (°C)	Applications	Concerns
Sn-3.5Ag	221	SMT, Flip chip	Cu dissolution, Excessive IMCs, Voids
Sn-3.8Ag-0.7Cu	217	SMT, PTH, BGA	Cu dissolution, Excessive IMCs, Voids
Sn-3.5Ag-3Bi	208-215	SMT	Cu dissolution Fillet lift, low mp phase
Sn-0.7Cu	227	PTH, Flip chp	Cu dissolution, Wetting, excessive IMCs
63Sn-37Pb	183	PTH, SMT, BGA Flip chip	Pb toxicity
97Pb-3Sn	317	Flip chip	Pb-toxicity

Properties of Pb-free Solders

Most of Pb-free solders used are Sn-rich solders that typically contain more than 90% Sn. This suggests that the physical, chemical and mechanical properties of Pb-free solders are heavily influenced by the properties of pure Sn, as opposed to eutectic Sn-Pb solder, a mixture of Sn-rich and Pb-rich phases. Pure Sn is polymorphic, capable of existing as three crystal structures (α, β, γ) depending on temperature and pressure [48]. Since the white tin phase (β-Sn), stable at room temperature, has a body-centered tetragonal (BCT) crystal structure in contrast to the face-centered cubic (FCC) structure of Pb, the physical and mechanical properties of white tin are highly anisotropic compared to Pb. The white Sn crystal is optically birefringent, meaning an incident polarized light beam on a β-Sn crystal has a plane of polarization rotated upon reflection. Accordingly, polarized light microscopy is a convenient method to determine the crystal orientation of β-Sn dendrites or grain sizes for Pb-free solders in addition to EBSD (electron backscatter diffraction) technique [49, 50].

The melting point of most Pb-free commercial solders is within the range between 208 to 227ºC, which is about 30ºC higher than the melting point of eutectic Sn-Pb, 183ºC. The higher melting point or reflow temperature has serious implications on the performance of packaging materials and assembly processes, and can affect the integrity and/or reliability of Pb-free microelectronic packages. Another important issue related to the melting points is the difficulty of maintaining solder melting-point hierarchy, which is well established with Pb-containing solders. For example, since the melting point of high Pb flip-chip solder bumps is well separated by more than 100ºC from the melting point of eutectic Sn-Pb used in the next level of assembly, the high Pb, flip-chip solder joints formed at a higher temperature (e.g., 350ºC) do not become molten, during the subsequent eutectic Sn-Pb card assembly reflow operation (e.g., 215ºC). However, the proposed Pb-free solders only allow a maximum possible separation of about 30ºC or less between the melting points of any two solders. Hence, the choice of Pb-free flip chip solder compositions does not allow enough temperature separation for subsequent module or card assembly processes with another Pb-free solder composition.

Owing to the unique crystal structure of β-Sn, body-centered tetragonal (bct) crystal structure (a: 5.83, c: 3.18 Å), the physical, mechanical, thermal and electrical properties of β-Sn are highly anisotropic. Some of selected properties are collected in Table 3. The ratio of

anisotropy (defined as property along c-axis/property along a-axis) is also calculated in Table 3. The coefficient of thermal expansion (CTE) is about two times larger along the c-axis than the a-axis, while the Young's modulus along c-axis is three times larger than along the a-axis. This is a quite unique situation for β-Sn, since the trends of CTE and modulus are usually in an opposite direction for most metals and alloys. The electrical resistivity of β-Sn is significantly different in each direction with the anisotropy ratio of 0.69, i.e., the resistivity is about 70% smaller along the c-axis than the a-axis, consistent with the factor of a shorter lattice spacing along the c-axis.

More dramatic anisotropy is noticed with the atomic transport rates of Ag, Cu, or Ni in β-Sn, as shown in Table 3. The calculated ratios of anisotropy for Ag, Cu, and Ni are about 60, 40 and 30,000, respectively, at 150^oC, indicating enormous disparity in the solute diffusion rates along the c-axis vs. a-axis of β-Sn. The solute diffusion is attributed to the interstitial diffusion of Ag, Cu and Ni atoms, while the self-diffusion of Sn relies on a substitutional diffusion mechanism. The Sn self-diffusion rates are much slower than the solute diffusions, and are much less anisotropic compared to the solute diffusions in Sn.

When a solder joint contains a few grains or one single grain such as in flip chip or BGA joints, the anisotropic properties of β-Sn would seriously impact on the integrity and reliability of Pb-free solder joints. In case of Pb-free, near eutectic SAC solder joints, a clear dependence of the thermomechanical response on Sn grain orientation was reported [59]. BGA solder balls with the c-axis orientation parallel to the substrate were observed to fail before neighboring balls with different orientations. This result was explained based on the disparity of CTE values; a maximal CTE mismatch would occur in shear at the joint interface when the c-axis orientation is parallel to the substrate. In Pb-free, flip-chip solder joints, the effect of Sn grain orientation on electromigration degradation mechanism was reported [60]. Premature electromigration damage was identified when the c-axis orientation is aligned with the electrical current flow direction. This was explained based on the fast solute diffusion along the c-axis of β-Sn.

Table 3. Anisotropic Properties of β-Sn

Properties	a-axis	c-axis	Ratio of anisotropy (c/a-axis)	Reference
Lattice spacing (A)	5.83	3.18	0.54	51
Coefficient of thermal expansion (CTE) (ppm/^{o}C)	15.45	30.50	1.97	52
Young's modulus (GPa)	22.9	68.9	3.01	53
Electrical resistivity (μΩcm) at 300C	14.3	9.9	0.69	54
Self diffusivity of Sn at 150C (cm^2/s)	8.70 x 10^{-13}	4.71 x 10^{-13}	0.54	55
Diffusivity of Ag in Sn at 150C (cm^2/s)	5.60 x 10^{-11}	3.13 x 10^{-9}	56	56
Diffusivity of Cu in Sn at 150C (cm^2/s)	1.99 x 10^{-7}	8.57 x 10^{-6}	43	57
Diffusivity of Ni in Sn at 150C (cm^2/s)	3.85 x 10^{-9}	1.17 x 10^{-4}	30,390	58

Solidification, Microstructure and Undercooling

Formation of solder joints involves with a metallurgical process of melting (reflow) and solidification. The resultant microstructure therefore reveals the unique characteristics of as-cast microstructure. The effects of cooling rates and alloying elements with various Pb-free solders were investigated [50, 61]. One of the distinct properties of Sn-rich solders is a propensity for large amount of undercooling of β-Sn during solidification. The undercooling is defined as the temperature difference between the melting temperature of a solder during heating and the solidification temperature during cooling. The undercooling required for solidification of near-ternary Sn-Ag-Cu solder spheres of a few hundred micrometers in diameter (such as BGA or CSP solder joints) was much larger than high Pb solders or Sn-Pb eutectic solders [61, 62]. This large undercooling is also responsible for the growth of large primary phases such as Ag_3Sn in near-ternary Sn-Ag-Cu solders [62, 63]. It was also reported that the amount of the β-Sn undercooling in Sn-Ag-Cu solders is inversely proportional to sample size, suggesting a larger undercooling in a smaller solder joint (such as flip chip vs. BGA solder joints) [64].

A large undercooling in flip chip solder bumps can have a serious impact on the reliability of solder joints, since random solidification among many solder bumps can cause a situation of some bumps already solidified while others not, which could lead to a stress concentration to some bumps and possibly to early mechanical failures within solder joints.

A systematic investigation was conducted to find critical factors affecting the undercooling of Pb-free, flip-chip solder bumps by DSC (differential scanning calorimetry) and the direct observation of individual solder bumps in a glass mold during melting and solidification [65, 66]. The amount of the undercooling of Sn-rich solders is found to be strongly affected by solder volume, inversely proportional to its volume (or effective diameter of solder balls). It is also found that the solder composition and UBM (under bump metallurgy) significantly affect undercooling, but not so strongly as other factors such as the cooling rate and holding temperature of the mold plate used in C4NP. Sn-0.7Cu C4NP solder bumps in a mold plate were under-cooled by as much as 90°C from its melting point, while a less amount of undercooling (40 to 60°C) was observed on a Si chip with Cu/Ni UBM [65]. The direct observation of individual flip-chip-size solder bumps on a glass mold during their solidification process revealed the random nature of the molten solder nucleation process, and also confirmed the similar amount of the undercooling measured by DSC [66]. It was also found that some

minor alloying elements such as Zn, Co, and Ni are quite effective in reducing the amount of undercooling in Sn-rich solders [66]. Minimizing the amount of the undercooling of Pb-free solder bumps is desirable to provide chip joining integrity as well as solder joint reliability.

4.7. Interfacial Reactions in Pb-free, Flip-Chip Joints

Ball-Limiting Metallurgy (BLM) or Under Bump Metallization (UBM)

In flip chip structures, the chip wiring is terminated by a plurality of metal films that form the ball-limiting metallurgy (BLM), which is also referred as under-bump metallurgy (UBM), as schematically shown in Figure 32. The BLM defines the size of the solder bump after reflow, provides a surface that is wettable by solder and that reacts with the solder to provide good adhesion and acceptable reliability under mechanical, electrical and thermal stress, and is a barrier between the integrated-circuit device and the metals in the interconnection.

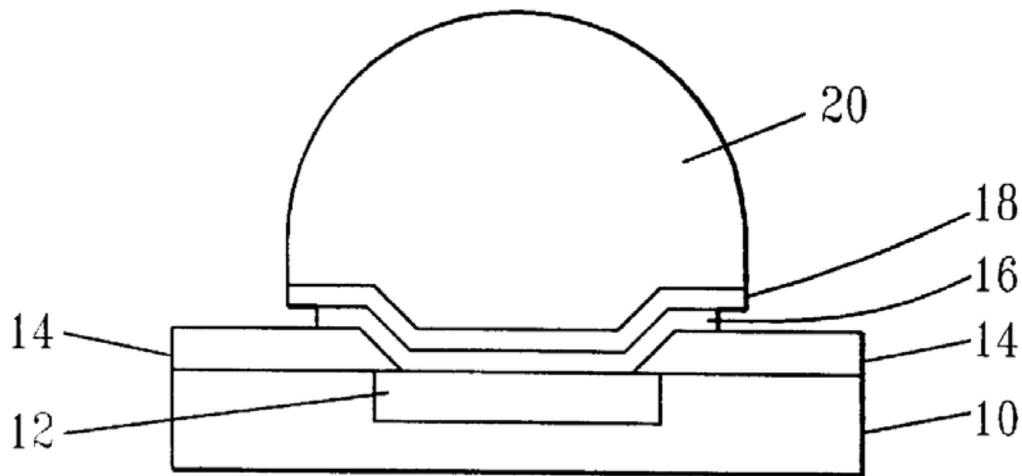


Figure 32. Ball-limiting metallurgy (BLM) or under-bump metallization (UBM) in flip-chip structures [67].

When the chip is attached to a ceramic module, solder with a high Pb content is reflowed at a temperature around 350°C. The Sn content of high Pb solders is typically less than 5% by weight (Table 2). A typical BLM structure is a thin film stack consisting of Cr or TiW (at the chip surface), CrCu, and Cu. The thin film stack of BLM is typically deposited by sputtering on a passivated wafer. The sputtered Cr or TiW layer provides good adhesion of the interconnection structure to the silicon-wafer substrate. The "phased CrCu" is a second adhesion layer consisting of co-sputtered Cr and Cu that is high in Cr at the barrier layer interface and high in Cu at the solderable metal Cu interface. The BLM layer also serves as an electrical connection for the electroplating of solder bumps. After solder bump plating, the BLM is formed by selective electro and chemical etching of the blanket thin film layers. During reflow, the Sn in the solder reacts readily with Cu to form Cu-Sn intermetallics, which provide adhesion between the solder the BLM. For solders with less than about 5% Sn by weight, a thin film of Cu (about 0.5 µm) is a suitable terminal layer for the BLM [67].

When the chip is directly attached to an organic laminate using SnPb eutectic solder, a thin layer of Cu (about 0.5 µm) would be essentially consumed to form Cu-Sn intermetallics, resulting in a loss of mechanical reliability. To control Cu consumption, a thick Cu (a few micron) was proposed as a solder wettable layer of BLM structures for SnPb eutectic [68] as well as Sn-rich solders. But this idea was abandoned after it was found that the thick Cu layer could facilitate the growth of voids during a high temperature aging such as at 150°C.

The proper choice of BLM is a critical element for successful Pb-free, flip chip development. Since most Pb-free solders have the Sn content more than 90% by weight and hence they are required to reflow at a higher temperature (at least 30°C) than eutectic Sn-Pb, the interfacial reactions are very aggressive in terms of UBM consumption and intermetallic formation, particularly with Cu metallization. A thin Ni barrier layer has been commonly used to control the aggressive interfacial reactions [13, 69-70], because Ni has a much less solubility than Cu in the molten Sn at the same reflow temperature. Table 4 compares the solubility of Cu vs. Ni in Sn as a function of temperature [71, 72]. The solubility of Cu in Sn is approximately seven times higher than Ni at a reflow temperature of 260°C, and is about five times higher at the typical aging temperature of 150°C.

Although Ni is an effective reaction barrier over Cu in Sn-rich solders, it is still desirable to control the consumption rate of Ni layer during reflow or high temperature storage or high current electromigration tests. Several other BLM structures are proposed for Pb-free, flip-chip structures [67, 73-75]. Among them, NiFe alloys were found to be an effective, solderable layer for Sn-rich solders [9, 73]. The NiFe was an electroplated thin film; compositions of 90%Ni-10%Fe, 80%Ni-20%Fe, and 50%Ni-50%Fe were investigated. The interfacial reactions of NiFe alloys with Sn-3.5%Ag were investigated to compare with other solderable BLM layers, such as Cu, Ni, and Ni(P) for various reflow times up to 20 min at 250°C. The dissolution of the solderable layers and the growth of intermetallic layers are listed for the case of 50%Ni-50%Fe in Table 5 and 6. The 80%Ni-20%Fe behaved similarly to 50%Ni-50%Fe in terms of the dissolution of the NiFe films and the intermetallic growth. The 90%Ni-10%Fe, on the other hand, reacted about as fast as pure Ni with the molten Sn-3.5%Ag; while a thick Cu layer of 4 μm was nearly consumed after 6 min, and a very thick intermetallic layer was formed. Thus, it was conclude that the composition range of NiFe up to 80% Ni was effective as a barrier layer for the high Sn solders. The electroless Ni(P) layer of 8 μm was compared for its interfacial reaction as shown in Table 4 and 5. In Sn-3.5Ag solder, Ni(P) dissolved more than the 50%Ni-50%Fe or Cu/Ni did, and its intermetallic growth was also more extensive than the NiFe. In a recent study, excellent solderability of electroplated Fe-Ni alloys was also reported with eutectic SnAgCu solder [76].

Substrate Metallization

The choice of substrate metallization either on laminates or ceramic modules is as important as UBM, since a solder joint is formed between two interfaces; UBM and substrate metallization. Most common substrate metallization used are Cu-OSP and electroless Ni(P) with immersion Au (ENIG) on laminates, and Ni(P)/Au on ceramic substrates.

Electroless nickel-phosphorous film, Ni(P) is widely used fro under-bump metallization (UBM) of flip-chip and substrate metallization of ball-grid array packages. This is due to its superior characteristics, such as excellent solderability, corrosion resistance, uniform deposition thickness, and selective deposition process. The microstructure of a Ni(P) film changes significantly with its P content. A Ni(P) layer containing less than 5.5 wt % P is known to be

nanocrystalline, while that of more than 9 wt % P is amorphous. The Ni(P) films with .5.5 – 8.5 wt % P are known to be a mixture of small crystallites and an amorphous phase [77].

When a Ni(P) film reacts with a Sn-Pb eutectic solder, some part of the film underneath the solder crystallizes into Ni3P around the reflow temperature (200-240°C). This low-temperature reaction is called "solder reaction-assisted crystallization" in contrast to the self-recrystallization of Ni(P) at a higher temperature at 300-450°C. The solder reaction-assisted crystallization is accompanied by the formation of the Ni-Sn IMC and Kirkendall voids [78]. These interfacial reactions result in brittle fracture whose paths are often found to be around the -rich layer, causing a reliability issue of Ni(P) metallization. When a Ni(P) film reacts with pure Sn or Sn-rich solders, the extent of interfacial reactions significantly increase, often a severe IMC spalling from Ni(P) is observed [79, 80]. The IMC spalling is found to be strongly influenced by P content, solder volume or deposition method [80]; higher P content and larger solder volume causing more spalling. In addition, higher tendencies of IMC spalling are noted from screen printed solder paste over electrodeposited solder .

To prevent IMC spalling, a thin intermediate layer of Sn or Cu was deposited on top of Ni(P) by electro- or electroless plating. During the reflow reaction of Sn-3.5%Ag solder paste, the intermediate layers effectively suppressed Ni-Sn IMC spalling during the reflow reaction at 250°C, 30 min, while most IMC spalled off the Ni(P) filem in a few minutes in the control samples without an intermediate layer [81]. The Sn layer provided protection of the Ni(P) surface and a good wettable surface during reflow. The thin Cu layer changed the chemical structure of the interfacial IMCs in addition to providing a good wettable surface.

In the study of the interfacial reactions of Pb-free solder joints in plastic ball grid arrays (PBGA), it was found that the choice of substrate metallization can also affect the IMC formation at the UBM interface [13]. By pairing three substrate metallization, Cu/OSP, Ni(P)/Au, and Ni(P)/Pd/Au, five groups of the PBGA laminate modules were produced with surface finishes of Cu-Cu, Cu-Au/Ni(P), Au/Ni(P)-Au/Ni(P), Cu-Au/Pd/Ni(P), and Au/Pd/Ni(P)-Au/Pd/Ni(P). PBGA laminates were assembled using 0.89 mm solder balls of Sn-3.8Ag-0.7Cu, reflowed up to 12 cycles at 260°C. From the systematic analysis of their microstructure, composition and microhardness, it was found that the interfacial reaction of one side is significantly affected by the choice of surface finish at another interface, because the elements from one surface finish dissolve sufficiently into the molten solder and rapidly diffuse to the

other. The microhardness in the BGA solder joints is strongly affected by the choice of surface finish, not much by reflow cycle. The surface finish composed of more Ni layers shows a higher hardness value than without a Ni layer, indicating dissolved Ni solute atoms are much more effective in hardening Sn-rich solder joints than Cu atoms [13]. Considering the big difference in solder volume between a BGA and flip-chip solder joint, the effect of substrate metallization on the interfacial reactions at the UBM side would be even more substantial in the case of flip-chip interconnection.

Table 4. Solubility of Cu vs. Ni in Sn as a function of temperature (all in wt %)

Temperature	Cu solubility	Ni solubility
260°C	1.41	0.216
250°C	1.23	0.198
200°C	0.0035	0.0009
150°C	0.0011	0.0002
50°C	$3.79*10^{-5}$	$3.52*10^{-6}$

Table 5. Solderable Layer Thickness after Simulated Reflows at 250C of Sn-3.5%Ag Solder (all values in μm), [9]

Solderable Layer	0 min	2 min	6 min	20 min
Cu(4 μm)	4.0	1.0-2.3	0.7-1.7	0 -1.7
Cu(2 mm)/Ni(2 μm)	4.0	3.3	3.1	3.1
Cu/50Ni-50Fe(2.7 μm)	6.7	6.1	6.1	6.0
Cu/Ni(P)(8 μm)/Au(50 nm)	8.3	5.8	5.5	4.9

Table 6. Thickness of Intermetallic Layer Formed when Sn-3.5Ag Solder Reacts with Solderable Layer at 250C (all values in μm), [9]

Solderable Layer	2 min	6 min	20 min
Cu(4 μm)	1.7 – 8.3	0.7 - 10.0	1.7 - 13.3
Cu(2 mm)/Ni(2 μm)	1.2 – 4.0	1.8 -4.8	2.0 -6.4
Cu/50Ni-50Fe(2.7 μm)	0.3 – 0.5	0.3 – 0.5	0.3 – 0.6
Cu/Ni(P)(8 μm)/Au(50 nm)	0.7 – 1.7	0.7 – 2.1	0.9 – 2.4

Interfacial Reactions in Pb-free Solder Joints

The interfacial reactions in Sn-rich solder joints are very aggressive compared to those in eutectic SnPb joints, mainly due to the higher Sn content and the higher reflow temperature used in Pb-free soldering [69, 70]. During the reflow, there are two basic reactions occur at the soldering interfaces; dissolution of BLM and substrate metallization into a molten solder, and concomitant intermetallic formation at the interfaces. Both reactions have serious impacts on the integrity of solder joints, and should be controlled for reliable solder joints. The intermetallic phases continue to grow in the solid state during a high temperature aging, often accompanied with interfacial void formation when a disparity of diffusing species across the interface would exist. Numerous studies have been conducted to understand the fundamental characteristics of the interfacial reactions in Pb-free solders (such as intermetallic identification, growth kinetics, etc.), as well as to control the interfacial reactions to improve the reliability of solder joints. A few examples of the intermetallics formed at Cu and Ni metallization are summarized in Table 7 and 8 [82]. With a model joint of Cu(25 μm)/Ni/Sn(40 μm), the interfacial reactions were studied in terms of Ni plating type (electroplated vs electroless), Ni thickness and reflow condition. The IMC phases formed in Cu/Ni/Sn joints are determined by Ni thickness and reflow time due to the involvement of Cu under-layer. Ni_3Sn_4 is detected in all samples for a short reflow time, indicating that . Ni_3Sn_4 is the first-forming IMC phase on Ni layer. For the long reflow time of 10 min, when Ni is less than 1 μm thick, Cu under-layer facilitates to form $(Cu,Ni)_6Sn_5$. The IMC morphology is strongly affected by the type of Ni plating. The angular or faceted Ni_3Sn_4 is observed on electroplated Ni, while needle-like IMC is on electroless Ni(P). The presence of Cu under-layer changes the interfacial microstructure significantly by forming the $(Cu,Ni)_6Sn_5$ phase, which grows faster than the binary Cu_6Sn_5 or Ni_3Sn_4. The effect of Cu over-layer was investigated with the model joint of Cu(25 μm)/Ni/Cu/Sn(40 μm) samples as shown in Table 8. For thin Cu, $(Ni,Cu)_3Sn_4$ forms dominantly, while for thick Cu, $(Cu,Ni)_6Sn_5$ is the major phase. In Table 8, the Cu concentration in Sn-Cu alloys is estimated for each Cu thickness by assuming the entire Cu over-layer to dissolve into 40 mm Sn. This result is quite consistent with the previous work on the effect of Cu concentration on the interfacial reactions between Ni and Sn-Cu solders [83]. The transition of the IMC phases from $(Ni,Cu)_3Sn_4$ type to $(Cu,Ni)_6Sn_5$ occurred around 0.5 wt % Cu.

Recently, many research works have been reported to control their interfacial reactions by adding minor alloying elements to Sn-rich solders, such as Co, Fe, Ge, Ni, Mn, Ti, Zn, rare-earth metals (Ce, La), and others [12, 84-94]. Among them, Zn is found to be the most effective with Cu UBM by providing multiple benefits, such as reducing Cu consumption and IMC formation [12, 91], suppressing void formation during aging [92], reducing the undercooling of Sn-rich solder alloys [90], improving impact strength [93], enhancing electromigration resistance [94], and others. The beneficial effects of Zn addition on the interfacial reactions with Cu metallization was explained by detecting the accumulation of Zn atoms at the interface between Cu and Cu_3Sn IMC layer [12, 92]. This Zn accumulation layer was claimed to be a Cu-Zn solid solution alloy rather than a Cu-Zn IMC layer, based on a chemical etching experiment as well as a thermodynamic calculation of the driving force of Cu_3Sn phase [92]. In addition, a couple of possible mechanisms for suppressing void formation on electroplated Cu during high temperature aging was also proposed, such as reduction of Cu3Sn growth rate or direct diffusion of Zn to the interface to fill up any vacancy sites before they grow into a large size of voids [92].

Since Zn addition has some concerns in soldering such as propensity for oxidation or degradation of wettability, it should be very careful in controlling the amount of Zn addition to Sn-rich solders. It is reported that around 0.4 wt % Zn was effective without degrading other properties. Since the direct addition of Zn into Sn-rich solders is a challenging task in solder manufacturing process, it is recently proposed to use Zn-containing UBM to control the interfacial reactions [95].

In a recent study, the Ni consumption during reflow with Sn-rich solders were evaluated with various Ni-based (electroplated, electroless and sputtered) UBMs [96]. A minor addition of Ni (0.2 wt %) to Sn-rich solders was found to be beneficial in suppressing Ni consumption for pure Sn and Sn-2Ag, but not for Sn-0.7Cu. In fact, the Ni addition has increased the Ni UBM consumption in Sn-0.7Cu. This enhanced Ni consumption in Sn-0.7Cu was attributed to the formation of $(Cu,Ni)_6Sn_5$ intermetallic phase in the solder matrix [96]. A trace amount of Ni and Ge has been added to eutectic Sn-Cu solder to improve fluidity and wettability, to prevent shrinkage cracks (hot tears) or to enhance impact fracture strength [97]. In Table 9, some beneficial effects of other minor alloying additions are also summarized.

Table 7. IMC phases formed in Cu(25 μm)/Ni/Sn(40 μm) samples as a function of Ni thickness and reflow time, [82].

Samples	Reflow Time (min).	
Ni(ED) or Ni(EL)	2	10
0.3	$(Cu,Ni)_6Sn_5$>$(Ni,Cu)_3Sn_4$	$(Cu,Ni)_6Sn_5$ > $(Ni,Cu)_3Sn_4$
0.6	$(Ni,Cu)_3Sn_4$	$(Cu,Ni)_6Sn_5$ > $(Ni,Cu)_3Sn_4$
1	$(Ni,Cu)_3Sn_4$	$(Ni,Cu)_3Sn_4$ > $(Cu,Ni)_6Sn_5$
3	Ni_3Sn_4	$(Ni,Cu)_3Sn_4$
10	Ni_3Sn_4	$(Ni,Cu)_3Sn_4$

Table 8. IMC formed phases in Cu(25 μm)/Ni/Cu/Sn (40 μm) samples as a function of Cu thickness and reflow time on electroplated Ni, [82].

Samples			Reflow Time (min)	
Ni (μm)	Cu (μm)	(wt%)	2	10
1	0.04	0.1	$(Ni,Cu)_3Sn_4$ > $(Cu,Ni)_6Sn_5$	$(Cu,Ni)_6Sn_5$ ~ $(Ni,Cu)_3Sn_4$
	0.3	0.8	$(Cu,Ni)_6Sn_5$	$(Cu,Ni)_6Sn_5$ > $(Ni,Cu)_3Sn_4$
	0.5	1.4	$(Cu,Ni)_6Sn_5$	$(Cu,Ni)_6Sn_5$
3	0.1	0.3	$(Ni,Cu)_3Sn_4$ > $(Cu,Ni)_6Sn_5$	$(Ni,Cu)_3Sn_4$ > $(Cu,Ni)_6Sn$
	0.3	0.8	$(Cu,Ni)_6Sn_5$	$(Ni,Cu)_3Sn_4$ > $(Cu,Ni)_6Sn$
	0.5	1.4	$(Cu,Ni)_6Sn_5$	$(Cu,Ni)_6Sn_5$ > $(Ni,Cu)_3Sn_4$

Table 9. Effects of Minor Alloying Elements on Properties of Sn-rich Solders

Properties	Ag	Cu	Bi	Co	Fe	Ge	In	Mn	Ni	RE	Sb	Ti	Zn
1) Undercooling decrease				X	X			X	X			X	X
2) Microstructre to refine	X	X				X		X		X		X	
3) Shear strength increase	X	X	X						X	X	X		
4) Ductility increase							X			X			
5) Cu dissolution decrease		X	X						X				X
6) Intermetallics control			X								X		X
7) Void formation decrease				X	X								X
8) Impact strength increase									X			X	X
9) Fatigue life increase		X									X		
10) Electromigration improve	X												X
11) Wettability improve						X				X			
Reference	50, 94	50, 91	89	88	88	97	85	87, 98	87, 97	86	99, 100	87, 98	12, 90-94

4.8. Reliability of Flip Chip Interconnect Structure

Thermal Fatigue

Thermal fatigue performance of flip-chip solder joints is a key issue in developing reliable flip-chip packages both on organic and ceramic substrates. Development of flip-chip packages on organic laminates has been only possible by successfully applying underfill encapsulation technology for solder bumps. The underfill encapsulation provides compressive stress to each solder bump as well as reduces the effect of the global thermal expansion mismatch between the silicon chip (2.5 x 10^{-6}/^{o}C) and the organic FR-4 PCB (18.5 x 10^{-6}/^{o}C) by deforming together as a unit to reduce the relative deformation between the chip and the PCB [101]. Without the underfill encapsulation, flip-chip packages on organic substrates would not survive more than a few hundred cycles in a typical thermal fatigue test condition. Flip-chip packages on ceramic substrates would generally not need the underfill encapsulation owing to their small or closely matched thermal expansion mismatch with ceramic substrates. However, as the chip size is continuously increasing for high performance flip-chip interconnection, the underfill encapsulation could be an option to extend the thermal fatigue life or other reliability performance of ceramic flip-chip packages at the expense of reworkability of flip-chip solder joints.

In the early Pb-free, flip-chip development, several research works were reported on the thermal fatigue performance of Pb-free solders compared to Pb-containing flip-chip solder joints [32, 45, 102]. Three Pb-free solders, Sn-0.7Cu, Sn-3.8Ag-0.7Cu and Sn-3.5Ag, formulated as solder paste, were evaluated for flip chip applications [102]. Test dies of 12.6x7.5 mm^2 with TiW-Cu and Ni(P)-Au UBM were directly attached to organic boards with Cu-OSP or Ni(P)-Au pad finish. To accelerate solder bump fatigue, no unerfull encapsulation was used on the assembled parts. The flip-chip packages were then tested in air under 0 to 100°C and -40 to 125°C thermal cycling conditions. Among the solders/UBM evaluated, Sn-0.7Cu bump on both Ni(P) and TiW/Cu UBMs had the longest fatigue life, while Sn-3.5Ag on Ni(P) UBM the shortest life [102]. The Sn-3.8Ag-0.7Cu on TiW/Cu UBM had a better fatigue life than Sn-3.5Ag, worse than Sn-0.7Cu, and a similar life to Sn-37Pb on Ni(P). The better fatigue performance of Sn-0.7Cu joints were explained by the fatigue crack initiation and propagation mechanism through the grain boundaries. The cracks were observed to propagate at the grain

boundaries, significantly removed from the UBM/bump interface near the center of the joint. This solder was claimed to be most compliant in thermal fatigue and to undergo massive deformation before failing by crack propagation [45].

The effect of silver content on thermal fatigue life of Sn-Ag-Cu flip chip interconnects was systematically investigated for flip-chip packages assembled to FR-4 substrate with SAC solder balls of 300 μm in diameter [103]. From the thermal cycling test in air between -45 and 125°C, it was found that solder joints with a high Ag content, 3 and 4 wt %, had a longer fatigue life compared to solder joints with a lower Ag content, 1 and 2 wt %. The better fatigue performance of solder joints with a higher Ag content was attributed to the stable microstructure owing to the dispersion of fine Ag_3Sn intermetallic particles. In the low Ag solder joints, significant microstructure coarsening was observed during the thermal cycling test [103]. In another study, the effect of Ag content on thermal fatigue life of ceramic BGA modules mounted on an organic substrate was evaluated in terms of Ag content, cooling rate and thermal cycling conditions [104]. It was found that the fatigue life was influenced by Ag content as well as thermal cycling test condition. The low-Ag joints (2.1%) had the best thermal fatigue life for the thermal cycling condition of 0 to 100°C with a long cycle time of 120 min, while the high-Ag joints (3.8%) had the best life over other joints for the condition of 0 to 100°C with a short cycle time of 30 min. The slow cooling rate (0.5^{o}C/s) used during assembly was beneficial for the thermal fatigue life of SAC joints regardless of Ag content or thermal cycling conditions in comparison to the fast cooling rate (1.7^{o}C/s). Extensive failure analysis was conducted with thermal-cycled solder joints to propose the failure mechanisms operating during the accelerated thermal cycling (ATC) tests [105].

The fatigue performance of Pb-free flip-chip solder joints would be strongly affected by Sn crystal orientation and its directionality in physical/mechanical properties, since flip-chip solder bumps are expected to be either a single crystal or composed of a few grains, similarly as reported in much larger BGA joints of Pb-free solders [59, 106]. When Sn crystal orientation plays in thermal failure process, the conventional fatigue failure mechanism, largely affected by the DNP-related factors (such as chip size, solder bump height, CTE mismatch or thermal cycling temperature difference, etc), would be more complex to understand. In the conventional thermal cycling test, the solder bumps at the corner of a Si chip with the largest DNP would expect to fail first, but this situation would not be warranted when Sn crystal orientation plays

into the failure process. A similar case has been already reported in the thermal cycling test of Pb-free, BGA solder joints [106], when the c-axis of Sn-crystal is oriented parallel to the substrate direction, a premature fails were observed regardless of the position of solder joints [59].

Drop Impact Reliability

With the recent advent of ubiquitous portable or mobile electronics, drop impact resistance of solder joints has been recognized as a critical reliability issue, especially for chip scale packages (CSP), wafer level packages (WLP), micro-BGA or BGA, where underfill encapsulation is not normally applied [107-110]. For flip-chip-on-board (FCOB) applications, underfill encapsulation is necessary to meet thermal fatigue requirements, and is also beneficial for its drop impact reliablity [109].

The root cause of brittle fracture of solder joints during drop test has been identified as the weak interface between IMC layers and Cu pad [111]. It was reported that upon thermal aging solder joint strength can drastically degrade due to the formation of Kirkendall voids at the interface between IMC and Cu pad in Pb-free solder joints [111, 112]. However, this weak interface is not easily detected by the mechanical testing with a slow strain rate, such as ball shear test, but by drop or impact test of a high strain rate [111, 112]. It is also reported that the formation of interfacial voids is only sporadic with certain electroplated Cu pads, rarely observed in high purity or wrought Cu foils even after extensive thermal aging [92, 113].

In case of Pb-free flip-chip interconnects having thick Cu UBM, similar interfacial voids were observed during a high temperature storage test at 150°C, 1000h, as shown in Figure 33. The concentration of voids between the Cu and Cu_3Sn IMC layer suggests the void formation mechanism being related to the growth of Cu_3Sn layer. This was one of the reasons why the thick Cu UBM structure was not adopted for Pb-free flip-chip applications.

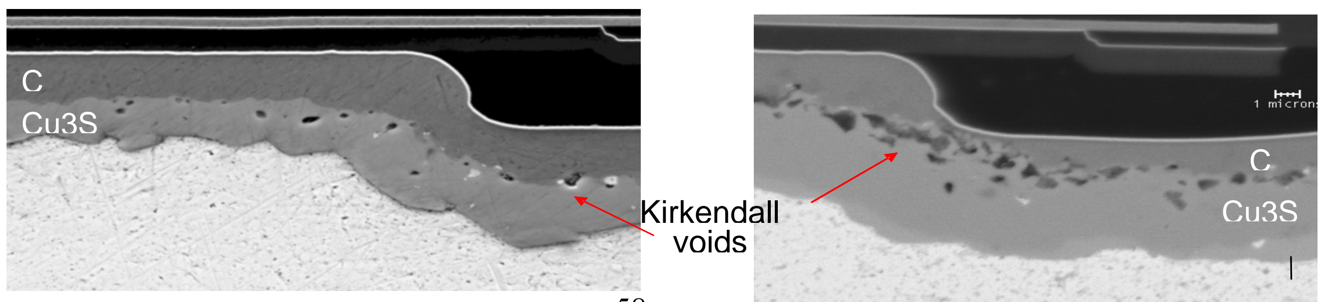
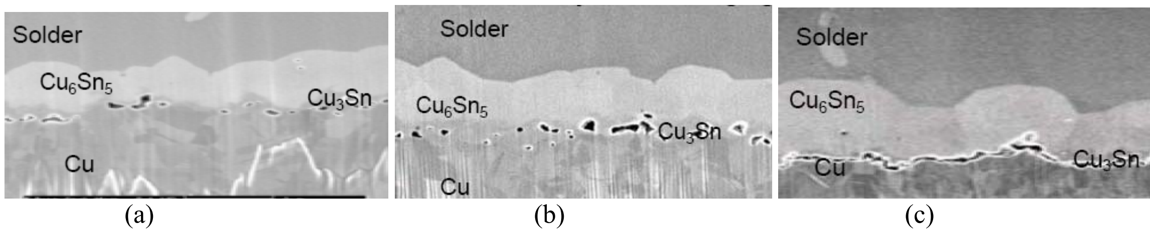


Figure 33; (a) Thick Cu BLM – incoming, (b) Thick Cu BLM- HTS 1000 h

Kirkendall void is a reliability issue when Sn containing solders, both Pb-containing and Pb-free, are joined to thick Cu pad and annealed for a prolonged time. Fig. 34(a) shows a SnAgCu alloy joined to Cu and annealed at 125 ^{o}C for 3, 10 and 40 days, respectively. The voids are formed in the Cu_3Sn intermetallic layer near the interface with Cu. It can form an almost continuous layer after annealing for 40 days and seriously impact the drop reliability of the package assembly, as shown in Figure 35 [111, 114]. The formation of voids is highly variable. Depending on the property of the plated Cu the void density may increase dramatically. The voiding is faster at higher temperatures but even products that do not get very hot in service may still be endangered.

In order to improve the drop reliability of Pb-free solder joints, two approaches have been taken; either reducing Ag or Cu content in Sn-Ag-Cu solders, adopting a low Ag version, such as SAC105 (Sn-1.0%Ag-0.5%Cu) [109, 115, 116] or adding minor alloying elements to control their interfacial reactions and thereby to suppress the interfacial void formation [88, 93, 97, 98, 109, 115]. The additions of Ti, Mn, Ni, or In were reported to improve the impact resistance of Sn-Ag-Cu joints [98, 115], while Ni and Ge were added to Sn-Cu [97], and Zn added to Sn-Ag [56] for the same purpose. One solution to the problem is by doping the solder with a small amount of Zn and the voids are mostly eliminated, as shown in Fig. 36. [12].



(a) (b) (c)

Figure 34. SnAgCu solder joints on Cu and annealed at 125 C for a) 3 days, b) 10 days and 3) 40 days [111].

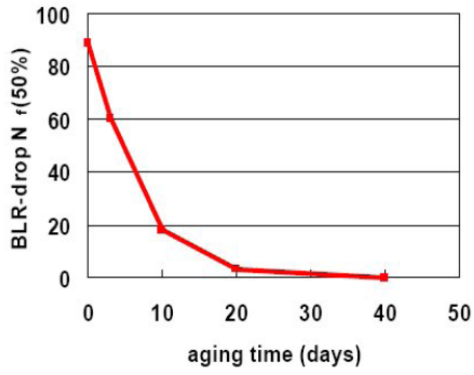


Figure 35. Drastic degradation of the drop reliability of a SAC solder joint after aging at 125 C for up to 40 days [111].

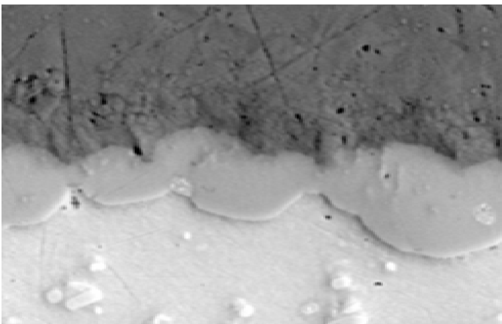


Figure 36. SnAgCu with minor Zn addition joined to Cu and annealed at 150C, 1000 h, showing no void [12].

Chip-Package-Interaction: Interlayer Dielectric Cracking During Module Assembly

Critical reliability challenges were encountered during the qualification of Pb-free solders in microelectronics packages. The challenges are associated with the inability of accommodating the large stress/strain induced during chip joining by high-strength Pb-free solders. This situation often leads to cause either delamination between the BEOL layers or cracking within the low-k layer in the back-end-of-line (BEOL) structure [21, 47, 117]. The first type is commonly referred to as ILD (Interlayer Dielectric) delamination [21, 47] caused primarily by the greater thermo-mechanical stresses imposed on the BEOL structure due to the use of high strength Pb-free solder. The problem is further aggravated by the use of large chips which generate higher stresses due to the global differential thermal expansion mismatch between the chip (CTE~3 ppm) and laminate carrier (CTE~17 ppm). Delamination failure between BEOL layers is shown in Figure 37. The open circuit can be detected by using acoustic scan imaging and is identified as a "white bump", as shown in Fig. 38. To mitigate the problem, a solder with a higher creep rate can be chosen to deform more easily during chip joining, and therefore it reduces the stresses transmitted to the BEOL layers. In addition, improving the adhesion strength between the layers was shown to effectively mitigate the problem. The other type of commonly observed white bump failures involves the coherent cracking within the ultra low dielectric (ULK) layer, as shown in Figure 39 [24]. Corner C4's due to higher DNP (distance from neutral point) stresses are particularly susceptible to cracking. As a consequence of the continued reduction in dielectric constant, typically accompanied with increased porosity, the ILD materials become increasingly fragile. Elastic modules and fracture toughness of the low-k layers decrease rapidly as porosity increases. Cracking in the ILD layers under the flip-chip bump is frequently observed. The move to higher CTE organic laminate (~16 ppm) from the ceramics (3-6 ppm) further aggravates the problem due to increased CTE mismatch and warpage of both the laminate and chip.

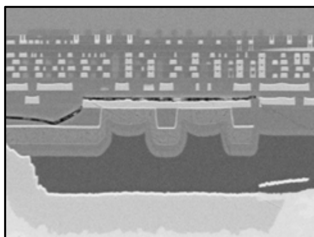


Figure 37. SEM image of interfacial delamination between the Cu pad and the FTEOS layer [21].

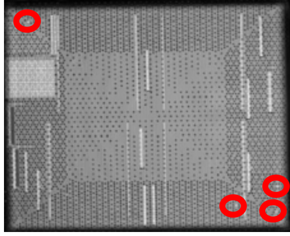


Figure 38. Acoustic scan image showing the "white bumps" [21].

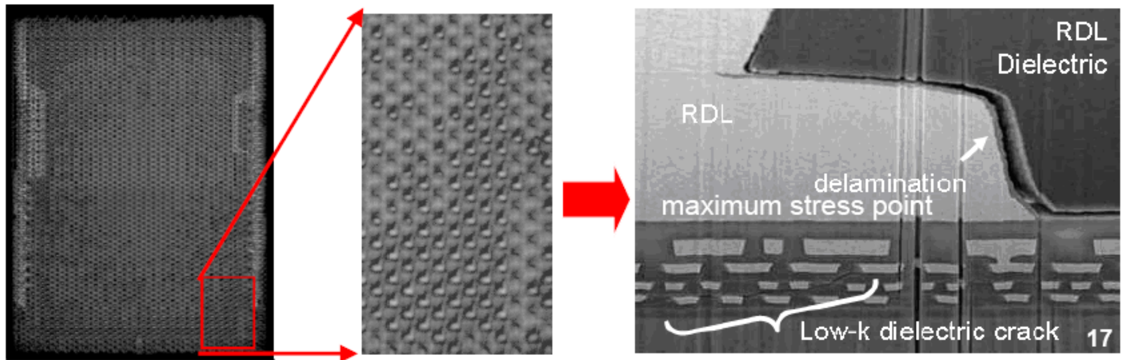


Figure 39. Open failures detected by (a) the acoustic scan image at chip corner, was caused by (b) coherent cracking in the uLK layer [24].

To mitigate the white bump problems the fundamental solutions are to reduce the thermo-mechanical stresses, in particular, the tensile stress transmitted to the ILD layers. Reported stress mitigation methods include optimization of the mechanical properties and microstructure of Pb-free solders [47, 117], temperature profiles during chip joining to the laminate substrate [21, 117], improving the BEOL structure, reducing laminate and chip warpages, and use low CTE laminate material. Stress reduction to the ILD layer can also be achieved by designing a geometrically compliant interconnect which can readily absorb the stresses before transferred to the chip.

Reducing the cooling rate during reflow is shown to reduce the stresses and the incidents of WB. It, however, increases the process time and reduces manufacturing throughput. Solder with a higher creep rate is desired because it deforms more easily and, therefore, reduces the stresses transmitted to the BEOL structure. A faster creep rate often translates into a longer thermo-mechanical fatigue life. Sn0.7Cu bumps creep more easily than Sn3.5Ag bumps and were found to cause less warpage in chip and laminate and, therefore, less stresses to the BEOL layers. To understand the solder stress issues, C4NP bumping technology was used to facilitate quick debug, optimization and, finally, identification of the solder

solution among a comprehensive list of solder candidates. Table 10 correlates the solder compositions with their hardness data, which agree with the laminate warpage data. Low Ag and Cu content solders have lower hardness and more desirable mechanical properties to absorb the stresses before transmitted to the ILD layer to cause cracking. As a result the use of low Ag and Cu was shown to significantly reduce white bumps than the conventional near-eutectic SAC solder alloys. Fig. 40 shows a microhardness indentation on the C4 solder joint.

wt% Sn	wt% Ag	wt% Cu	Hardness, HV Mean (std dev)
97.6	2.2	0.2	**16.0** (0.6)
98.5	1.3	0.2	**14.5** (0.8)
98.5	0.9	0.6	**14.0** (0.0)
98.6	1.2	0.2	**14.0** (0.6)
99.5	0.3	0.2	**12.0** (0.9)
99.3	0	0.7	**11.5** (0.5)

Table 10: Module level solder joint microhardness and indentation measurements.

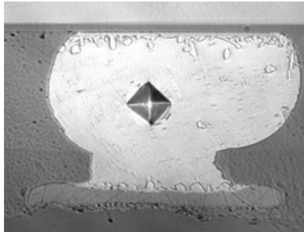


Figure 40. A typical module level micro-hardness indentation measurement on solder joint.

Improving the far-BEOL structure is another effective method to reduce the stresses transmitted to the low dielectric material layer. As shown in Figure 41, several critical elements in Intel's BEOL structures processors have been changed to manage the high stresses of the Cu pillar bumps, including a thick polyimide layer (~ 16 microns) under the Cu pillar bump, small via and a thick M9 Cu pad [24]. The structure optimization is designed to reduce the stresses to the low-k, uLK layer. The cross-sectional view is shown in Figure 41.

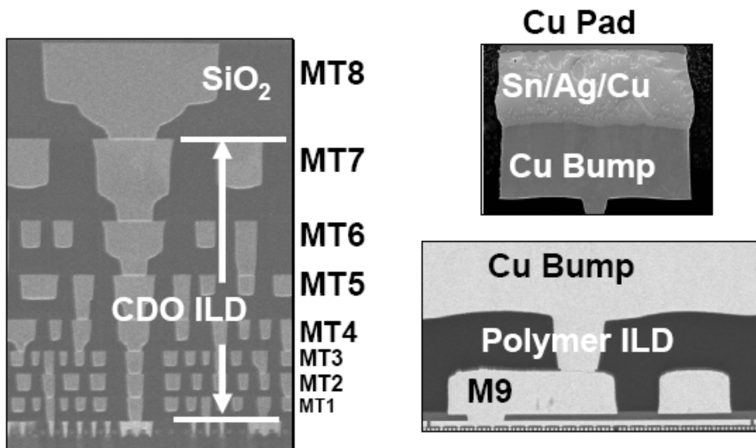


Figure 41. The BEOL of Intel's processor chips have been drastically changed to prevent cracking of the low k materials [24].

With the continued movement to ultra low-k materials in the 32 and 22 nm nodes of BEOL silicon technology which is more porous with low modulus, the chip package interaction (CPI) problem will becomes even more challenging.

To provide a low-stress interconnect for flip-chip BGA package with Pb-free solders, the creep properties of Sn-0.7Cu vs Sn-3.5Ag bumps were measured by nano-indentation technique at various temperatures [47]. It was found that Sn-0.7Cu bumps crept more easily than Sn-3.5Ag bumps, and the difference in the creep rate between them increased at a higher temperature. The different creep rates were explained by the different characteristics of IMC particles formed in each solder system. The chip warpage and the shear stress at the low-k layer were also calculated and measured; finding that Sn-0.7Cu bumps had the smaller chip warpage and shear stress than Sn-3.5Ag bumps. The maximum shear stress with Sn-0.7Cu bumps was about 11% less than the delaminating stress of the low-k layer. In addition, further reduction in the maximum shear stress (36%) was demonstrated by applying post-annealing at 200°C for 10 min with Sn-0.7Cu bumps, but not much with Sn-3.5Ag. This positive result with Sn-0.7Cu bumps was again attributed to the higher creep rate of Sn-0.7Cu compared to Sn-3.5Ag.

As already discussed in the section of Drop Impact Reliability, low-Ag version of Sn-Ag solders were proposed to reduce the propensity for CPI damages [117]. Combining various characterization techniques such as dynamic chip warpage measurement (DCWM), confocal scanning acoustic microscope (CSAM), and EBSD (electron backscatter diffraction), it was able

to demonstrate that solder creep deformation is the limiting process for CPI damages. Lowering the creep resistance (by reducing Ag content) and reducing the strain rate by slow cooling were confirmed to be beneficial in reducing the propensity of CPI dames on actual parts. The reduction in Ag content (from 2% to 0%) in Sn-Ag bumps was very effective to reduce the peak stress by 40%, down to levels comparable to SnPb solders. It was also noted that the significant local variations of CPI damages, without a strong dependence on the distance to the chip center, were explained by the "local" parameters of Sn grain size and orientation by analyzing EBSD data of damaged and undamaged sites [24].

Electromigration Reliability

Electromigration (EM) of metallic atoms in device conductors, such as Al or Cu has been well recognized as critical reliability and design issues in advanced integrated circuits (IC), while electromigration in flip-chip solder joints is not considered as a serious concern simply because of their much larger dimensions and corresponding low current density. However, in the recent years, due to the continuing trend of miniaturization in IC and their interconnects, the electromigration of flip-chip solder joints became an important reliability issue, especially owing to the effects of current crowding or joule heating [118].

In the most recent development of Pb-free flip-chip technology, the electromigration in Sn-rich solder joints has become a critical reliability challenge, largely because of lower melting temperatures of Sn-rich solders in comparison to high Pb solders as well as the remarkable anisotropy in diffusion rates of common solute atoms such as Cu, Ni, or Ag in the Sn matrix as discussed earlier. Since the general subjects of electromigration in flip-chip solder joints are covered in a separate Chapter, only a few selected topics regarding the microstructure effects of Pb-free solders on electromigration are briefly discussed in this section.

Early EM test results obtained from actual flip-chip solder joints are often complicated to compare each other because their solder temperature and current density significantly vary among samples due to current crowding and local joule heating. In order to avoid these complications, a model wire test structure, providing uniform current density and minimal gradients, was adopted to compare pure electromigration effects of solder composition, UBM, and surface finish UBM [60, 119]. From this study,

it was found that Sn-Ag joints have a superior EM performance over Sn-Cu under the same conditions of other variables [119]. In addition, two failure mechanisms are identified [60]; Mode-I, probably dominated by Sn self-diffusion resulting in separation between IMC and solder. Mode-II is responsible for premature fails in EM tests, which is clearly dominated by a fast diffusion process of Ni and/or Cu in Sn, when the c-axis of Sn grain orientation is parallel to the direction of electron flow. EM failure mechanism in Sn-Ag joints with higher Ag content is dominated by Mode-I fail, while more Mode-II was observed in Sn-Cu joints. In the subsequent study, the alloying effects of Ag, Cu and Zn on the EM performance of Sn-rich solders have been systematically investigated using the Cu wire structure [94]. For Sn-Ag joints, the frequency of early EM fails (associated with Mode-II) significantly decreases as Ag content increases, while Mode-II fails are more commonly observed in Sn-Cu joints for all Cu concentrations tested. The EM lifetime of Sn-Cu joints is generally shorter than Sn-Ag or Sn-Ag-Cu joints. The better EM performance of Sn-Ag over Sn-Cu is explained by the stable network of Ag_3Sn particles during EM or high temperature aging experiment [120], and also supported by EBSD work on Sn grain orientations.

The beneficial effect of Zn doping on EM performance is also reported for Sn-Ag joints [94]. It is observed that Zn combines closely with Cu and Ag that stabilizes the IMC network and effectively slows down Cu diffusion. Hence, EM reliability is significantly improved in Zn-doped Sn-Ag joints. The effects of other alloying elements such as Ni, Sb or Bi were also investigated, but finding no appreciable improvement on EM performance.

EM degradation mechanisms in Pb-free solder joint are highly dependent on crystal orientation. Sn, with a compressed body center tetragonal structure, as shown in Figures 42 and 43 [106], has a highly anisotropic electrical, mechanical of diffusion properties. For fast diffusers, such as Ni and Cu in Sn, the difference in diffusivities between c- axis and a- or b-axis can be very large as shown in Figure 44. [55-58].

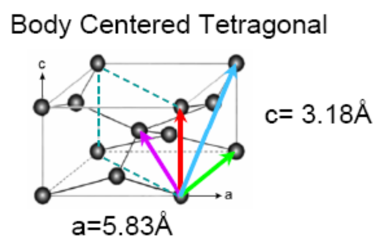


Figure 42. The compressed Sn structure shows c-axis is much shorter than the a- and b-axis [106] .

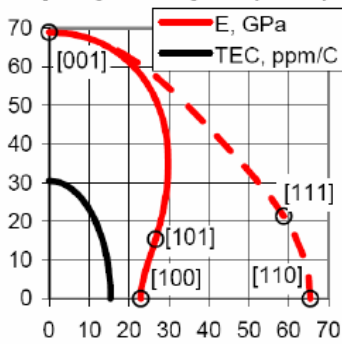


Figure 43. The CTE and modulus of Sn are highly anisotropic [106] .

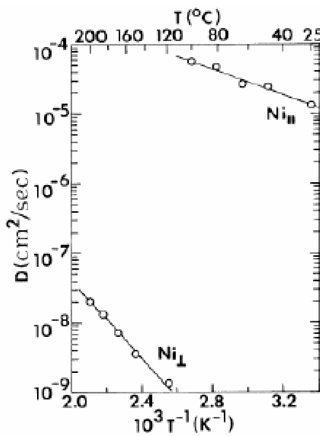


Figure 44. The rate of diffusion of Ni in Sn is much faster along the c-axis [56, 57].

EM degradations were found to depend on grain orientations [60]. As shown in Figure 45, when the c-axis is not closely aligned with the current direction (the right grain), the failure is mostly driven by Sn self-diffusion that causes cavitation at the solder-IMC interface. On the other hand, a much faster EM induced degradation mechanism occurs when the c-axis of the Sn grain is closely aligned with the current direction (on the left grain). With this alignment, the solute atoms such as Cu or Ni from the UBM and interfacial IMC are swept away by the fast interstitial diffusion along the c-axis of the Sn crystal, resulting in rapid consumption of UBM metallurgy and catastrophic failure at an early stage of EM test [60].

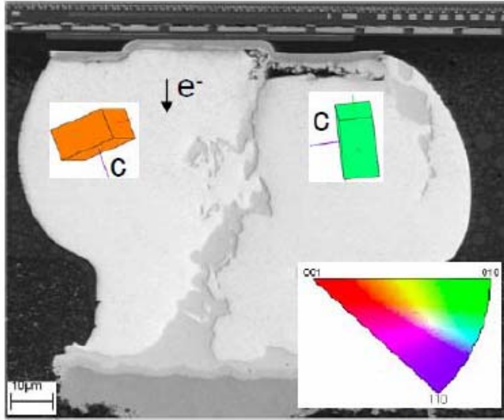


Figure 45. SEM image of a bi-crystal C4 bump with SnCu solder [60].

Statistically, the rapid failure driven by interstitial diffusion of Cu and Ni is more commonly observed in SnCu than in SnAg solder joints, as shown in Figure 46. Kinetic study showed that the activation energy and current density exponent for SnAg solders (Mode-I dominated) are about 0.95 eV and 2, respectively; while those for SnCu solders are about 0.54 eV and 1, respectively [60, 119].

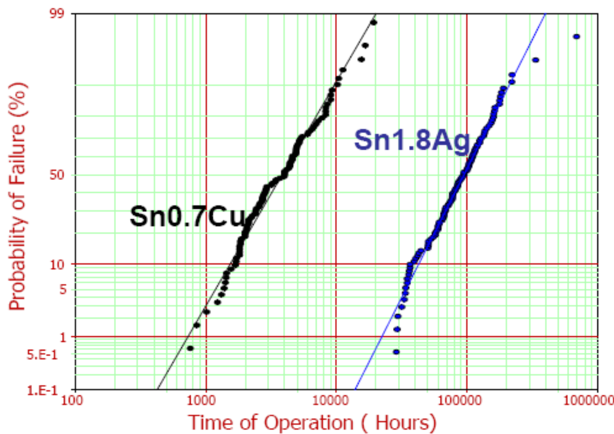


Figure 46. Cumulative failure probability plot comparing SnCu vs. SnAg. Both solders were tested at 90 C at 200 mA [119].

The Blech length effect was observed in SnAg solders, but not in SnCu solders [121, 122]. The saturation in resistance change due to the Blech effect can effectively suppress the diffusion processes and extend the EM lifetime of flip-chip solder joints. The effect of special alloy doping is

important on the EM performance as shown in Fig. 47, for SnAgCu alloy [123]. The increase in resistance is plotted as a function of test time when the solder joints were stressed at $5.2\text{x}10^3$ A/cm^2 and 150 ^{o}C for 1100 hrs. For SAC alloy, shown in Fig. 47(a), some samples showed early failures due to resistance increases that exceeded failure criteria. In comparison, SAC solder doped with minor Zn alloying element significantly enhanced EM performance by eliminating the early failures, as shown in Fig. 47(b). While it is difficult to control the Sn grain orientation, minor alloy doping can influence the Sn microstructure and, thus, the EM performance. For example, Zn reacts strongly with the alloying elements, such as Cu, Ag and Ni, in the Sn-rich solder matrix, as well as at the solder / UBM interfaces. The strong binding of Zn with Cu effectively slows down Cu migration. It is shown that Zn stabilizes both Ag_3Sn and Cu_6Sn_5 IMC networks and suppresses the formation of Cu_3Sn IMC. Although Zn doping does not seem to control the grain orientation in bulk solder, the random grain orientations at the interfaces and strong binding with Cu effectively eliminate the mode–II type early failures and suppress the mode-I type fails. Consequently, the solder EM lifetime with Zn doping is greatly improved [123].

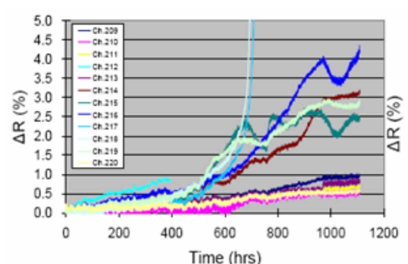


Fig. 47(a) SnAgCu solder joint stressed at $5.2\text{x}10^3$A/cm^2, at 150 ^{o}C for 1100 hrs. Some samples had early failures.

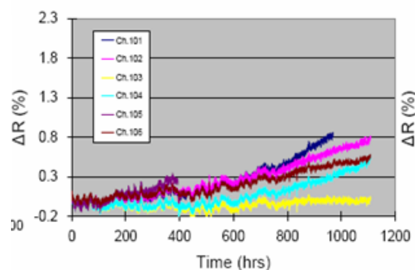


Fig. 47(b). A minor Zn doped SnAgCu solder joint stressed under the same condition. Early failures have been eliminated [123].

In addition to the effects of grain orientation and solder alloying, EM performance can be significantly improved by reducing current crowding [124, 125]. Figure 48(a) is a two-dimensional simulation of current distribution in a solder joint. Figure 48 (b) is a display of current density

distribution in the joint, where the cross section of the joint is plotted on the *x*–*y* plane and the current density is plotted along the *z*-axis. It is the current crowding or the high current density shown at the upper right corner in Fig. 48 (a) and (b) that leads to electromigration damage in the solder joint. Consequently, electromigration damage in a flip-chip solder joint can occur near the cathode contact on the chip side.

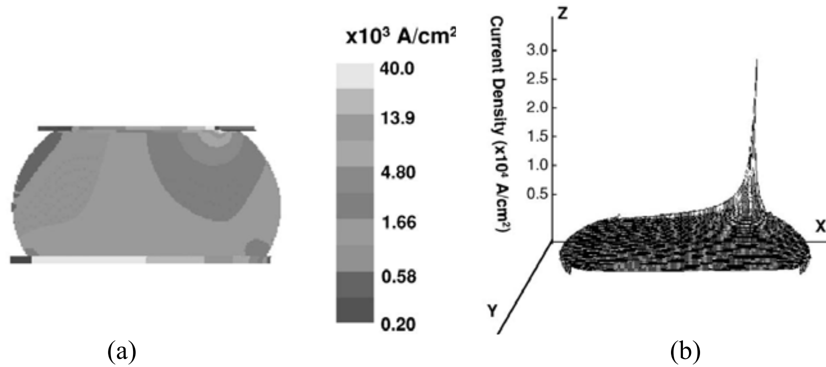


Fig. 48 (a) Two-dimensional simulation of current distribution in a solder joint. (b) Current density distribution in the joint, where the cross section of the joint is plotted on the *x*–*y* plane and the current density is plotted along the *z*-axis [124].

Current distribution in a flip-chip solder joint can be studied using finite element analysis as a function of geometry and resistance of all the conducting elements associated with a solder joint, including the Al or Cu interconnect, the UBM, and the solder bump itself. The factors that affect current distribution the most have been found to be the thickness and resistance of under-bump metallization. If Cu is part of the UBM, the thickness of the Cu can affect current crowding greatly. For a thick Cu UBM of 5 μm, the highest current density due to current crowding will occur within the Cu. Simulation has shown that the maximum current density can be reduced by at least twenty times with a 20 μm Cu UBM as compared to that of a thin UBM. More importantly, the thick Cu will enable a redistribution of current laterally in the entire Cu UBM, so the current density in the solder bump will be much closer to the average value, i.e., only a slight current crowding occurs in the solder near the Cu/solder interface. By using three-dimensional simulation, the current redistribution in the thick Cu and the solder is found to be very uniform. As a consequence, compared with the conventional solder joint with thin UBM, the benefit of thick Cu pillar bump to enhance EM performance has been widely reported. [124, 125]

Figure 49 shows a schematic representation of the EM mechanism in conventional solder vs Cu pillar [126]. The thick pillar, normally more than 40 μm in thickness, significantly improves the current distribution uniformity by eliminating current crowding and hot spot, and, therefore, enhances the EM performance, as indicated in the plot of Figure 50. The enhanced current distribution can be seen in the SEM images of a cross section through PbSn (Figure 51 (a)) and Cu (Figure 51(b)) bumps which have exhibited failure during EM stressing. For the conventional solder bump, the failure occurs in the pad via opening indicating high current crowding in that small region. For the Cu pillar bump, failure occurs away from the via region and shifted to a much greater area at the Cu/solder interface. As reported, despite the significant improvement in EM performance, the extremely stiff structure and, therefore, the high stresses generated by the tall Cu pillar bumps can make the implementation of low-k dielectric materials more challenging. It can often lead to partial or complete die cracking. A special stress mitigation architecture in the silicon back-end structure was necessary, as shown in Figure 41 [27, 42], to accommodate the Cu pillar bump on low-k materials. Controlling the growth of CuSn IMCs and Kirkendall void formation, especially on the side wall of the Cu column, is another reliability issue that need to be resolved.

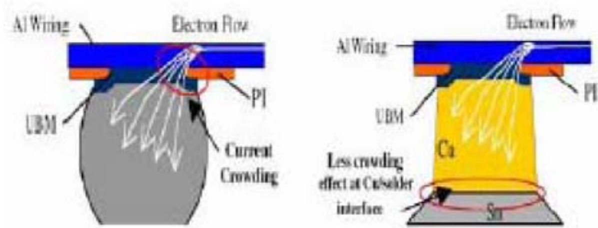


Figure 49. Schematic representation of current spreading mechanism comparing solder bump with cu pillar bump [126].

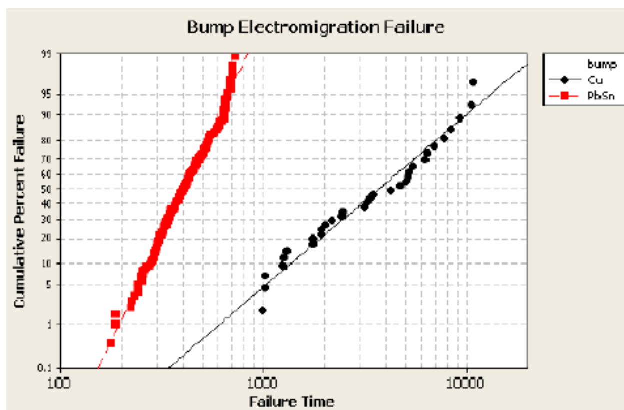


Figure 50. Cumulative failure plot comparing a conventional PbSn bump with a Cu pillar bump [29].

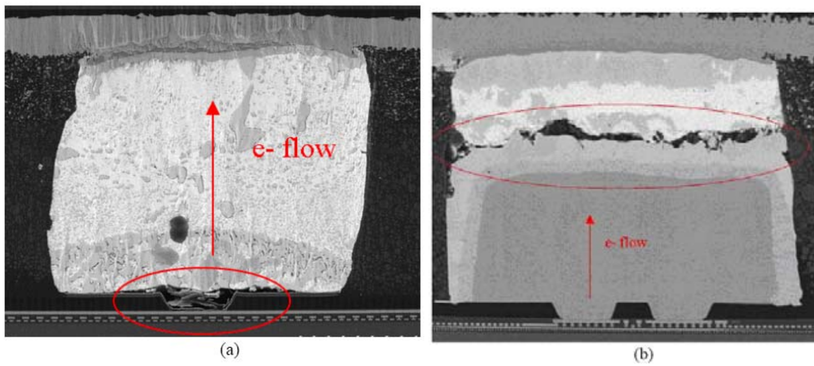


Figure 51. SEM images of a cross section through (a) a conventional PbSn bump and (b) Cu pillar bump [29].

Sn Pest

Sn pest, the allotropic transformation of β-Sn (body centered tetragonal) into α-Sn at temperatures below 13 ^{o}C, is another reliability issue. It has been observed in Pb-free solders at low temperatures, shown in Fig. 52(a) and Fig. 52(b), [127]. The transformation normally takes long time to happen. It is accompanied by an increase in volume by 26% and solder joint could practically disintegrate very rapidly. The presence of residual stress in solder joint accelerates the transformation process. Doping the solder with a small amount of Bi and Sb was reported to suppress Sn pest formation. [62, 128]

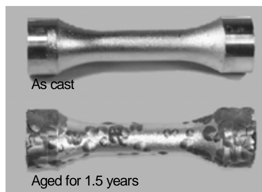


Fig. 52(a). Top view Sn0.5Cu samples aged for 1.5 years at 8 ^{o}C, compared to an as machined sample [127].

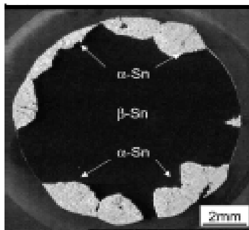


Fig. 52(b) Cross-section view shows Sn pest transformation starts from the surface in the highly stressed grip area [127].

4.9. Future Trends in Flip Chip Technology

As feature size continues to scale down, the number of transistors and interconnects on a chip has increased continuously. As a result, the number of chip to package input/output (I/O) interconnects have also increased significantly in the past decades. On the one hand, flip-chip I/O pitch is being reduced continuously to meet the requirement of I/O counts in high-performance and high-bandwidth applications. On the other hand, chip stacking with fine-pitch wire bond interconnection in low-cost memory and handheld applications are currently being replaced by fine-pitch area interconnection due to the high cost of Au and performance limitation of wire-bond technology in high-frequency regime. Furthermore, fine-pitch interconnection is highly demanded for 3D integration of semiconductor chips. Therefore, manufacturing of fine-pitch flip-chip (50μm pitch or below) interconnects needs to be explored. Integrated circuit (IC) system performance is significantly enhanced by 3D integration of chip and packages because of the benefits of high bandwidth, low latency, low power, and small form factor for a variety of applications. As demand for higher performance and higher bandwidth continue to increase, chip stacking with high-density thru-silicon-vias (TSV) interconnection is being developed and receiving more attention. [129-131]

Conventional Micro-solder Joint

Flip-chip interconnects can be produced by a number of methods. However, not all of the flip-chip bumping technologies are extendable to fine-pitch applications for volume production at low cost. Figure 53 shows SEM images of full area arrays of micro-bumps made of SnAg solder transferred to a 200 mm wafer at 50 μm pitch using C4NP technology. With the full area arrays, each test chip (6.5mm x 5.4mm) contains approximately 11,000 micro-bumps and a wafer contains ~9 million micro-bumps in total. To be able to inspect all the bumps, a high resolution tool is required with large memory for data processing. Figure 54 shows SEM image of a micro-bump in cross section after chip joined to an organic laminate with flux [23].

.

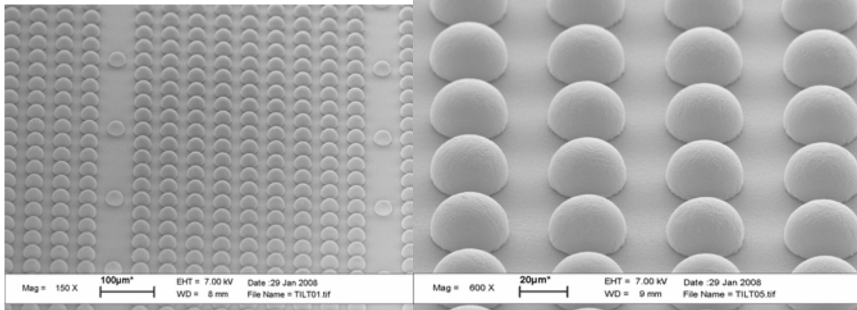


Figure 53 shows a full array of micro-bumps at 50 µm pitch.

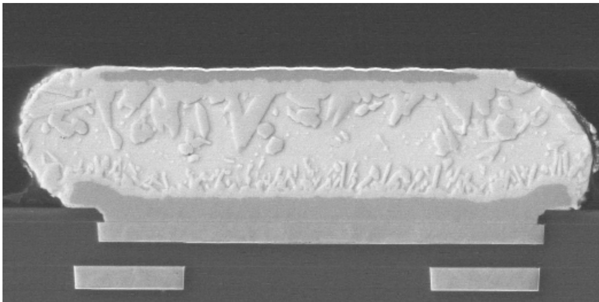


Figure 54 is a SEM image of a cross-sectioned micro-bump at 50 µm pitch with 28 µm diameter UBM pad.

Figure 55 (a) schematically shows stacked chips joined on a substrate with a sequential reflow process. In sequential reflow, the bottom chip is joined first onto the substrate, followed by subsequent chip joining. A sequential process can avoid relative displacement between chips as each subsequent chip is joined into the stack. Figure 55 (b) shows examples of 2-, 3- and 4-layer stacks of thinned TSV chips, utilizing sequential reflow of C4 interconnections. A major drawback of a sequential reflow process is that multiple reflows are necessary to complete the stack assembly. Multiple reflows require more processing time and lead to more dissolution of UBM, especially for the C4s contained in the lowest level of the stack, a concern for high reliability and high-performance applications. An alternative, parallel reflow process has also been demonstrated. A tacky flux is used to hold the stacked chips in place before the reflow process. Up to 4 layers of thinned TSV chips have been successfully formed with a single reflow step. With the self-centering effect of C4 bumps, a small amount of displacement between the chips is well compensated during reflow. To meet the demand for high I/O counts in high-performance and high-bandwidth applications, flip-chip I/O pitch needs to be reduced continuously. According to the International Technology Roadmap for Semiconductors (ITRS), the area-array flip-chip I/O bump (C4) pitch will be less than 70 µm for high-performance applications by 2018. [132]

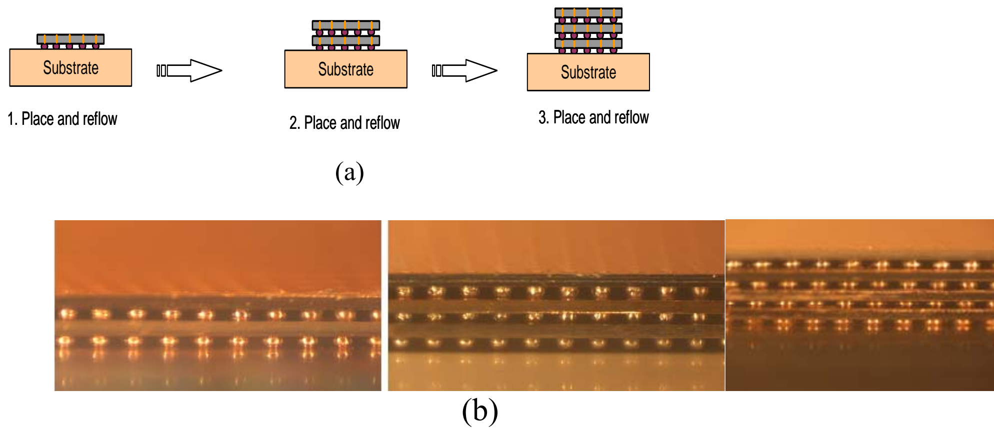


Figure 55 (a). Schematic drawing of a sequential reflow process and 16 (b) photos of 2-, 3- and 4-layer stacks of thinned TSV Chip [132].

To offer high degree of miniaturization, in particular, the 3D packaging technology, the assembly of thin IC's with thickness down to 10-50µm and pitch down to less than 20µm have been realized. The conventional 50-100 µm high solder bumps cannot be applied. Smaller solder volume, typically in the range of a few micrometers, by electroplating or immersion soldering, can be deposited on fine-pitch Cu, Au or Ni UBM pad. Due to the thin solder layer between chip pads the mechanical stability of solder joint is mostly dominated by the intermetallic compounds. These thin interconnects are one of the key element in realizing thin modules and 3D assemblies to meet the requirements of a variety of applications. In one extreme 3D integration may require stacking of multiple dies without the disturbing of the previous bonded dies [129, 131, 132] . This can be achieved by transient liquid phase (TLP) die-to-die or die-to-wafer bonding [133]. The most commonly used eutectic system is Au-Sn, Cu-Sn, Cu-In and Au-In systems. Sn or In can be applied on one or both sides of the bonding pads. When pressure and temperature are applied, the Sn or In will melt at low temperature which react with Cu or Au at their respective eutectic temperatures. As the reaction continues the thin solder joint eventually all converts to intermetallics which melt at much higher temperatures. The TLP bonding process has advantages over the solid-state diffusion bonding of Cu-Cu or Au-Au because of its lower process temperature and less sensitivity to surface topography and roughness. Figure 56 shows cross-section of micro joints at 15 µm pitch with Cu/Sn bump joined to ENIG. Cu-Sn-Cu bonding has becoming more popular with prototyping IC-stacks assembled using this technology [134, 135]. A three die stack using this technology is shown in Figure 57 [134]. Figure 58 shows a 16 Gb memory module made with 8-die stack from Samsung [136].

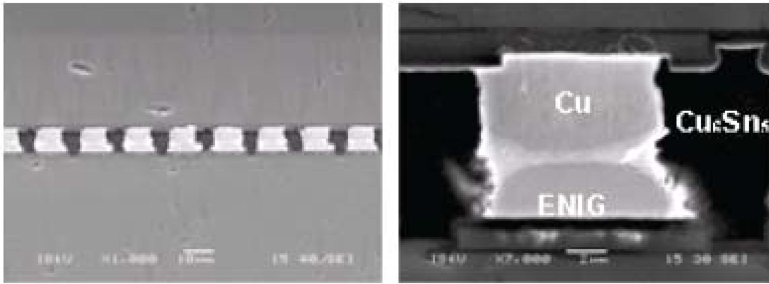


Figure 56 is a cross-section of Cu/Sn micro bump joined to ENIG at 15 μm pitch [133].

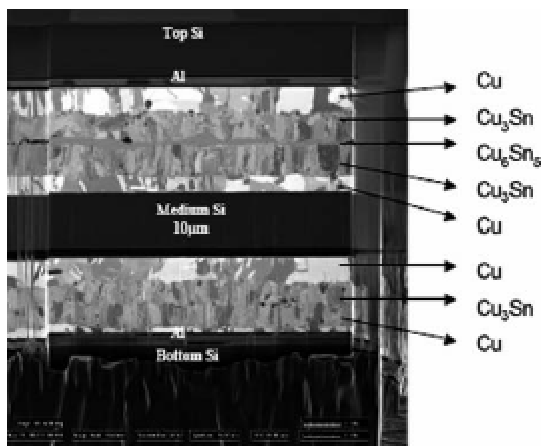


Figure 57. Field Ion Beam cross-section of a 3-die stack using Cu-Sn-cu technology [134].

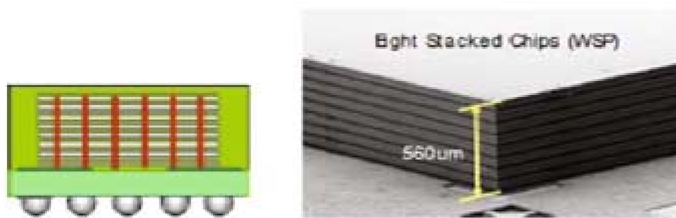
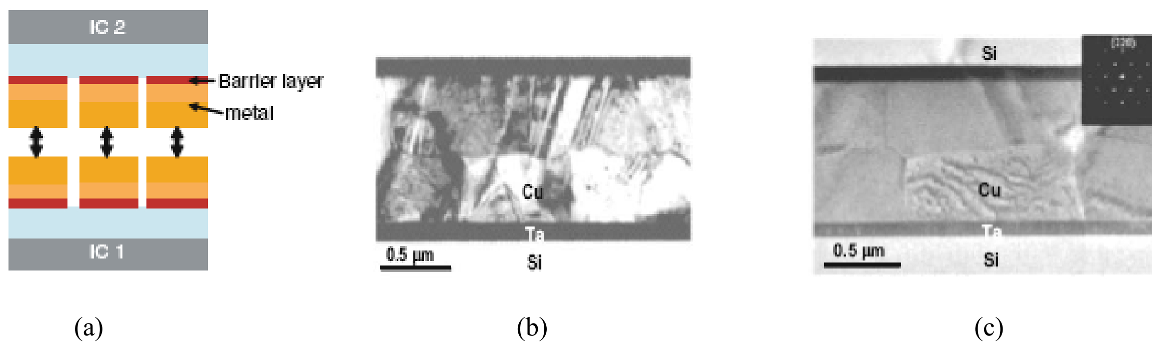


Figure 58. Samsung's 16 Gb memory module made with an 8-die stack using Cu-Sn-Cu technology [136].

Metal-to-Metal Solid-State Diffusion Bonding

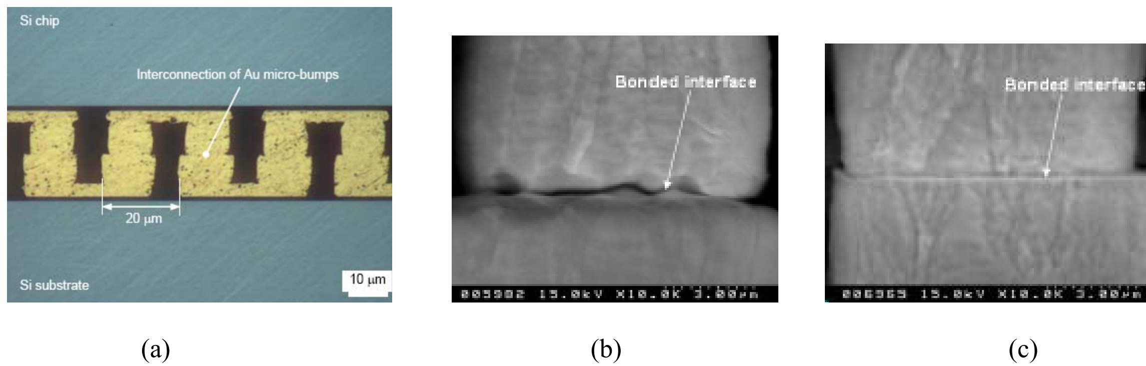
Metal-to-metal solid-state diffusion bonding of Cu to Cu [137-139] and Au to Au [140] has been widely practiced for IC stacking. The advantages are the formation of a non-melting micro joint during any of the sequential stacking processes, good heat transfer, and strong mechanical support. Cu-Cu bonding is achieved by thermo-compression, which requires temperature and force. Surface cleanliness prior to bonding is very critical. The effects of surface oxide, contamination, surface roughness and hardness all play a critical role in achieving successful bonding. An annealing step in N_2 or N_2-H_2 gas is needed to achieve higher bond strength by allowing Cu inter-diffusion and grain growth. Figure 59 shows the cross-section of (a) a schematic drawing and (b) TEM images of Cu-Cu bond after bonding and (c) after annealing (no visible interface)



(a) (b) (c)

Figure 59 shows (a) IC stacking using Cu-Cu bonding, (b) cross-section TEM image of Cu-Cu bond (c) After annealing (no visible interface) [141].

Au-Au can be bonded at lower temperature with surface planarization and plasma cleaning. Figure 60 shows cross-sectional images of Au-Au micro bumps bonded at 20 µm pitch with good shear strength and yield.



(a) (b) (c)

Figure 60 shows cross-sectional images of (a) Au-Au bumps at 20 µm pitch (b) before planarization, and (c) after planarization [140]. .

The main driving force for future flip chip technologies will continue to be dominated by miniaturization, 3D packaging, 3D die-stacking. Flip chip interconnect technology has expanded very rapidly. The conventional solder bumps will continue to dominate and moving toward finer pitch of 50 µm or less. While ultra-fine pitch bonding technologies, namely direct bonding of Cu-Cu and Au-Au, along with thru-Si via (TSV) and indirect bonding through a solder intermediate layer will be pursued at pitch of 20 µm or less to enable 3D packaging and integration. Significant progress has already been made in these areas. Major road blocks still exist. However, global alliance through the joint efforts between the equipment suppliers, device manufacturers, packaging houses, materials suppliers and research institutions are in play to achieve the common goals of small form factor, high performance and low cost.

4.10. Concluding Remark

The recent proliferation of flip-chip interconnects from high-performance microelectronics to low-end consumer electronics is largely owing to the development of several breakthrough technologies, such as high-density interconnect organic laminate (e.g., surface laminar circuitry), underfill encapsulation, direct-chip attachment using low-melt solder, low cost wafer bumping, and others. In this Chapter, the evolution of enabling assembly technologies were discussed with emphasis on their key processes, such as wafer bumping, underfill encapsulation, substrate bumping, copper pillar fabrication, and others..

As the physical feature sizes of the on-chip logic and memory functions are continually shrinking according to the Moore's law, the flip-chip technology has steadily advanced to accommodate the interconnection requirements by decreasing bump size and pitch as well as increasing the number of interconnecting bumps.

Recently, two key technological transitions have imposed significant challenges on the further progress of flip-chip technology. The first transition is coming from the new Pb-free solder technology required by the EU environmental legislations. The second one is associated with the implementation of low-k or ultra-low k dielectric materials in the BEOL structure in the advanced semiconductor devices. The application of Pb-free solders in flip-chip interconnects has raised several critical reliability issues, such as interfacial reactions, electromigration, drop impact resistance or thermal fatigue. In this Chapter, the fundamental issues of Pb-free solders for flip-chip applications were discussed in terms of the microstructure, solidification, physical/mechanical properties and interfacial reactions. Subsequently, an in-depth discussion was presented on several key reliability issues including thermal fatigue, impact drop reliability, electromigration, and others.

The most challenging issue encountered in flip-chip joining is chip-to-package interaction (CPI), leading to interlayer dielectric cracking in the advanced semiconductor devices. This failure mode is becoming more serious when Pb-free solders are implemented together with the ultra-low-k dielectric materials. Various solutions proposed or under development have been discussed in this Chapter.

References

1. L.F. Miller, "Controlled Collapse Reflow Chip Joining," *IBM J. Res. Develop.,* v.13, p.239, 1969.

2. L.S. Goldmann,"Optimizing Cycle Fatigue Life of Controlled Collapse Chip Joints", Proc. of the 19th Electronics Components Conference", P.404-423, 1969.

3. P.A. Totta, " Flip Chip Solder Terninals", Proc. of the 21st Electronics Components Conference", P.89, 1980.

4. P.A. Totta, S. Khadpe, N. Koopman, T. Reiley, and M. Sheaffer,"Chip-to-Package Interactions," Microelectronics Packaging Handbook, Part II, Edition, p. 129-283, Chapman & Hall, 1997.

5. D.-Y. Shih," Effect of Polyimide processing on Multi-chip Glass Ceramic Module Fabrications", IEEE Trans. on CPMT, Part C: Manufacturing, 19, 4, pp. 315, 1996.

6. Y. Tsukada, Y. Mashimoto, and N. Watanuki,' A Novel chip Replacement Method for Encapsulated Flip Chip Bonding", Proc. of the 43rd Electronics Components and Technology Conference", P.199-204, 1993.

7. Y. Tsukada, S. Tsuchida, and Y. Mashimoto,"Surface Laminar Circuit Packaging", Proc. of the 42nd Electronics Components and Technology Conference", P.22-27, 1992.

8. Y. Tsukada, Y. Maeda, and K. Yamanaka,"A Novel Solution for MCM-L Utilizing Surface Laminar circuit on Flip Chip Attach technology,", Proc. of the 2nd International Conference and Exhibition on Multichip Modules," pp.252-259, 1993.

9. S. K. Kang, J.Horkans, P.Andricacos, R.Crruthers, J.Cotte, M.Datta, P.Gruber, J.Harper, K.Kwietniak, C.Sambucetti, L.Shi, G.Brouillette and D.Danovitch, "Pb-Free Solder Alloys for Flip Chip Applications", Proc.49th ECTC, p.283, IEEE, Piscataway, NJ, (1999).

10. A. Rai, Y. Dotta, H. Tsukamoto, T. Fujiwara, H. ishii, T. Nukii, and H. Matsui," COB (Chip on Board) Technology," ISHM Proc. Pp. 474-481, 1990.

11. A. Rai, Y. Dotta, T. Nukii, and T. Ohnishi,"Flip chip COB Technology on PWB," Proc. Of IMC, pp.144-149, 1992.

12. S.K. Kang, D. Leonard, D.Y. Shih, L. Gignac, D.W. Henderson, S. Cho, J. Yu, "Interfacial Reactions of Sn-Ag-Cu Solders Modified by Minor Zn Alloying Addition," *J. Electron. Mater.*, Vol. 35, No. 3, pp. 479-485, (2006).

13. S.K. Kang, W.K. Choi, D.Y. Shih, P. Lauro, D.W. Henderson, T. Gosselin, D.N. Leonard,

"Interfacial Reactions, Microstructure and Mechanical Properties of Pb-Free Solder Joints in PBGA Laminates," *Proc 52nd Electronic Components and Technology Conf*, San Diego, CA, pp. 147-153, (2002).

14. T. Laurila, V. Vuorinen, and J.K. Kivilahti, "Interfacial Reactions Between Lead-free Solders and Common Base Materials", Materials Science and Engineering, 49, pp. 1-60, 2005.

15. T. Wang, F. Tung, L. Foo, and V. Dutta,"Studies on A Novel Flip-Chip Interconnect Structure-Pillar Bump", Proc. 51st *Electronic Components and Technology Conf*, pp. 945, 2001.

16. J. Kloeser,"High-performance flip chip packages with Cu pillar bumping," Global SMT & Packaging, pp.28-31, 2006.

17. D. Mallik, R. Mahajan, and V. Wakharkar,"Flip chip Packaging for Nanoscale Silicon Logic Devices: Challenges and Opportunities", Nanopackaging: nanotechnology and Electronics Packaging, Springer Science, pp.491-516, 2008.

18. P. Gruber et al., "Low Cost Wafer Bumping", *IBM J. Res. & Dev.* Vol. 49 No. 4/5, p.621, 2005.

19. E.. Laine, et al., "C4NP Technology for Lead Free Solder Bumping," *Proc. 57th Electronic Components and Technology Conf*, p. 1320, 2007.

20. E. Perfecto *et al*, "C4NP technology: Manufacturability, yields and reliability", *Proc 58th Electronic Components and Technology Conf*, p. 1642, 2008.

21. D.-Y. Shih, B. Dang, P. Gruber, M. Lu, S. Kang, S. Buchwalter, J. Knickerbocker, E. Perfecto, J. Garant, S. Knickerbocker, K. Semkow, B. Sundlof, J. Busby, R. Weisman,"C4NP for Pb-Free Solder Wafer Bumping and 3D Fine-Pitch Applications", Proc. International Conference on Electronic Packaging Technology, China, 2008.

22. J. Busby et al., "C4NP Lead Free Solder Bumping and 3D Micro Bumping", *ASMC conf.* p.333-339, 2008.

23. B. Dang, D.-Y. shih, S. Buchwalter, C. Tsang, C. Patel, J. Knickerbocker, P. Gruber, S. Knickerbocker, J. Garant, K. Semkow, K. Ruhmer, E. Hughlett, " 50 µm Pitch Pb-free micro-bumps by C4NP Technology", 58th Electronic Component and Technology Conference", pp. 1505-1510, May (2008).

24. R. Kasim, C. Connor, J. Hicks, J. Jopling, and C. Litteken,"Reliability for Manufacturing on 45nm Logic Technology with High-k + Metal Gate Transistors and Pb-free Packaging", International Reliability Physics Symposium, pp.350-354, 2000.

25. B. Ebersberger, and C. Lee,"Cu Pillar Bumps as a Lead-Free Drop-in Replacement for Solder-Bumped, Flip-Chip Interconnects," Proc. 59th *Electronic Components and Technology Conf*,

pp. 59-66, 2008.

26. A. Yeoh, M. Chang, C. Pelto, T. Huang, S. Balakrishnan, and G. Leatherman," Copper Die Bumps (First Level Interconnect) and Low-K Dielectrics in 65nm High Volume Manufacturing, 56th ECTC, pp.1611-1615, 2006.

27. J.W. Nah, J.O. Suh, K.N. Tu, S.W. Yoon, V.S. Rao, V. Kripesh, and F. Hua, "Electromigration in Flip Chip Solder Joints Having a Thick Cu Column Bump and a Shallow Solder Interconnect," J. Appl. Phys., Vol.100, p.123513-1, (2006).

28. L. Xu, J.K. Han, J.J. Liang, K.N. Tu, and Y.S. Lai, "Electromigration Induced Fraction of Compound Formation in SnAgCu Flip-Chip Solder Joints with Copper Column," Appl. Phys. Lett, vol.92, p.262104-1, (2008).

29. Y.S. Lai, Y.T. Chiu, J. Chen, "Electromigration Reliability and Morphologies of Cu Pillar Flip-Chip Solder Joints with Cu Substrate Pad Metallization," J. Elec. Mat's, Vol.37, No.10, p.1624, (2008).

30. A. Longford, and D. James,"Cu Pillar Bumps in Intel Microprocessors", Semicon Europa-Advanced Packaging Conference, Germany, April, 2006.

31. J.-W. Nah, K.W. Paik, T.K. Hwang, and W.H. Kim,"A Study on Coining Processes of Solder Bumps on Organic Substrates", IEEE Trans. On Electronics Pkg. Manuf. v. 26, No.2, PP.166-171, 2003.

32. P. Elenius, J. Leal, J. Ney, D. Stepniak, S. Yeh, "Recent Advances in Flip Chip Wafer Bumping using Solder Paste Technology", Proc. of the 49th ECTC, p.260-265, 1999.

33. L. Li, S. Wiegels, P. Thompson, and R. Lee,"Stencil Printing Process Development for Low Cost Flip Chip Interconnect", Proc. of the 48th ECTC, p.421-426, 1998.

34. J. Kloeser et al.,"Low Cost Bumping by Stencil Printing: Process Qualification for 200 µm Pitch", Proc. Of International Symposium on Microelectronics, pp.288-297, 1998.

35. Photo courtesy of Dr. Jae-Woong Nah.

36. E. Hashino, K. Shimokawa, Y. Yamamoto, and K. Tatsumi," Micro-Ball Wafer Bumping for Flip Chip Interconnection," Proc. of the 51th ECTC, p.421-426, 1998.

37. G. A. Rinne, "Solder Bumping Methods for Flip Chip Packaging", Proc. of 47$_{th}$ Electronic Components & Technology Conference, pp. 240-247, 1997.

38. K. Tatsumi, Y. Yamamoto, K. Iwata, E Hashino, S. Ishikawa, and T. Kohnox,"An Application of Micro-ball Wafer Bumping to Double Ball Bump for Flip Chip Interconnection" Proc. of 55$_{th}$ Electronic Components & Technology Conference, pp. 855-860, 2005.

39. I. Hazeyama,"Micro-Bump Formation Technology for Flip Chip LSIs using Micro-Solder-Ball", NEC res. & Develop. v.44, no.3, pp.219-224, 2003.

40. K. Inoue et al.,"Method of Forming Bumps", US Patent 6,213,386, 2003. (granted to Hitachi)

41. J.-W. Nah, P. A. Gruber, P.A. Lauro, and D.-Y. Shih," Injection Molded Solder – A New Fine Pitch Substrate Bumping Method", Proc. of the 59th Electronic Components & Technology Conference, pp. 61-66, 2009.

42. Directive 2002/95/EC of the European Parliament and of the Council of Jan. 27, 2003, Official J. of the European Union, 13.2.2003, L 37/19-23.

43. Directive 2002/96/EC of the European Parliament and of the Council of Jan. 27, 2003, Official J. of the European Union, 13.2.2003, L 37/24-38.

44. ROHS Expemtions; www.rohs.gov.uk

45. D. R. Frear, J.W. Jang, J.K. Lin, and C. Zhang, "Pb-free Solders for Flip-Chip Interconnects," JOM, pp.28-33, (2001).

46. D. Kim, D. Suh, T. Millard, H. Kim, C. Kumar, M. Zhu, Y. Xu, "Evaluation of High Compliant Low Ag Solder Alloys on OSP as a Drop Solution for the 2nd Level Pb-free Interconnection," *Proc 57th ECTC*, pp. 1614-1619, (2007).

47. M. Uchida, H. Ito, K. Yabui, H. Nishiuchi, T. Togasaki, K. Higuchi, H. Ezawa, "Low-stress Interconnection for Flip Chip BGA Employing Lead-free Solder Bump," *Proc 57th ECTC*, pp. 885-891, (2007).

48. J. D. Barnett, R.B. Bennion, H.T. Hall, Science, Vol.141, No.3585, p.1041, (1963).

49. D.W. Henderson, J.J. Woods, T.A. Gosselin, J. Bartelo, D.E. King, T.M. Korhonen, M.A. Korhonen, L.P. Lehman, E.J. Cotts, S.K. Kang, P.A. Lauro, D.Y. Shih, C. Goldsmith, and K.J. Puttlitz, "The Microstructure of Sn in Near Eutectic Sn-Ag-Cu Alloy Solder Joints and its Role in Thermomechanical Fatigue," J. Mat's Research, Vol.19, No.6, p.1608, (2004).

50. S. K. Seo, S. K. Kang, D-Y Shih, H. Mo Lee, "An Investigation of Microstructure and Microhardness of Sn-Cu and Sn-Ag Solders as a Function of Alloy Composition and Cooling Rate," J. Electronic Materials, Vol.38, No.2, pp.257-265, (2009).

51. M.J. Sullivan, S.J. Kilpatrick, "Handbook of Lead-free Solder Technology for Microelectronic Assemblies," (eds. K.J. Puttlitz, K.A. Stalter), p.920, Marcel Dekker, Inc, NY, (2004).

52. W.P. Mason and H.E. Bommel, *J. Acoust. Soc. Amer.*, 28, 930 (1956).

53. J.L. Everhart, “Properties of Tin and Tin Alloys,” Metals Handbook (T. Lyman, ed), American Society of Metals, Metals Park, p.1142, (1967).

54. J.A. Rayne and B.S. Chandrasekhar, *Phys. Rev.* 120, 1658 (1960).

55. B.F. Dyson, *J. Appl. Phys.* 37, 2375 (1966).

56. B.F. Dyson, T.R. Anthony, and D. Turnbull, *J. Appl. Phys.* 37, 3408 (1967).

57. D.C. Yeh and H.B. Huntington, *Phy. Rev. Lett.* 53(15), 1469 (1984).

58. F.H. Huang and H.B. Huntington, *Phys. Rev. B* 9(4), 1479 (1974).

59. T.R. Bieler, H. Jiang, L.P. Lehman, T. Kirkpatrick, E.J. Cotts, “Influence of Sn Grain Size and rientation on the Thermomechanical Response and Reliability of Pb-free Solder Joints,” 46th ECTC Proc., p.1462, [2006].

60. M. Lu, D.-Y. Shih, P. Lauro, C. Goldsmith, and D.W. Henderson, *Appl. Phys. Lett.* 92, 211909 (2008).

61. S.K. Kang, P. Lauro, D.Y. Shih, D.W. Henderson, K.J. Puttlitz, “The Microstructure, Solidification, Mechanical Properties, and Thermal Fatigue Behavior of Lead(Pb)-free Solders and Solder Joints Used in Microelectronic Applications”, IBM Journal of Res.&Dev, Vol. 49, No. 4/5, pp.606-620, July/Sept, (2005).

62. S.K. Kang, W.K. Choi, D.Y. Shih, D.W. Henderson, T. Gosselin, A. Sarkhel, C. Goldsmith, and K. Puttlitz, “Formation of Ag_3Sn Plates in Sn-Ag-Cu Alloys and Optimization of Their Alloy Composition”, Proc. 53rd ECTC, (New Orleans, LA), May 2003, p.64-70.

63. S.K. Kang, W.K. Choi, D.Y. Shih, D.W. Henderson, T. Gosselin, A. Sarkhel, C. Goldsmith, K.J. Puttlitz, “Study of Ag_3Sn Plate Formation in the Solidification of Near Ternary Eutectic Sn-Ag-Cu Alloys”, JOM, Vol.55, No.6, June, 2003, pp.61-65.

64. R. Kinyanjui, L.P. Lehman, L. Zavalij, and E. Cotts, “Effect of sample size on the solidification of temperature and microstructure of SnAgCu near eutectic alloys”, J. Mater. Res., Vol.20, No. 11, Nov.2006, pp.2914-2918.

65. S. K. Kang, M.G. Cho, P. Lauro, D-Y Shih, “Study of the Undercooling of Pb-free, Flip-chip Solder Bumps and In-situ Observation of Solidification Process”, J. Mater. Res., Vol.22, No.3, p.557, Mar. (2007).

66. S. K. Kang, M.G. Cho, P. Lauro, D-Y Shih, “Critical Factors Affecting the Undercooling of Pb-free, Flip-chip Solder Bumps and In-situ Observation of Solidification Process,” Proc. 2007 ECTC, p.1597, Reno, NV, May (2007).

67. P.C. Andricacos, M. Datta, W.J. Horkans, S.K. Kang, K.T. Kwietniak, "Barrier Layers for Electroplated SnPb Eutectic Solder Joints," US Patent No.5,937,320, Aug.10, (1999).

68. S.Y. Jang, J. Wolf, O. Ehrmann, H. Gloor, T. Schreiber, H. Reichl, K.W. Park,"CrCu Based UBM Study with Electroplated Pb/63Sn Solder Bumps-Interfacial Reaction and Bump Shear Strenght," IEEE Trans. CPT, Volo.26, No.1, p.245, (2001).

69. S.K. Kang, R.S. Rai, S. Purushothaman, "Interfacial Reactions During Soldering with Lead-Tin Eutectic and Pb-Free, Tin-Rich Solders," *J. Electron. Mater.*, Vol. 25, No.7 p.1113-1120, (1996).

70. S.K. Kang, D.Y. Shih, K. Fogel, P. Lauro, M.J. Yim, G. Advocate, M. Griffin, C. Goldsmith, D.W. Henderson, T. Gosselin, D. King, J. Konrad, A. Sarkhel, K.J. Puttlitz, "Interfacial Reaction Studies on Lead (Pb)-Free Solder Alloys," *IEEE Trans. Electron. Packag. Manuf.*, Vol. 25, No.3, p.155, (2002).

71. K.-W. Moon, W.J. Boettinger, U.R. Kattner, F.S. Biancaniello, C.A. Handwerker, "Experimental and Thermodynamic Assessment of Sn-Ag-Cu Solder Alloys", *J. Electron. Mater.*, Vol. 29, No. 10, pp. 1122-1136, (2000).

72. G. Ghosh, "Thermodynamic Modeling of the Nickel-Lead-Tin System," *Metall. Mater. Trans. A*, 30A, pp. 1481-1494, (1999).

73. P.C. Andricacos, M. Datta, W.J. Horkans, S.K. Kang, K.T. Kwietniak, G.S. Mathad, S. Purushothaman, L. Shi, H-M Tong, "Flip-Chip Interconnections Using Lead-free Solders," US Patent No.6,224,690 B1, May 1, (2001).

74. Y-T Cheng, S.R. Chiras, D.W. Henderson, S.K. Kang, S.J. Kilpatrick, H.A. Nye, C.J. Sambucetti, D-Y Shih, "Ball Limiting Metallurgy, Interconnection Structure Including the same, and Method of Forming an Interconnection Structure," US Patent No.7,273,803, Sep.25, (2007).

75. K.E. Fogel, B. Ghosal, S.K. Kang, S. Kilpatrick, P.A. Lauro, H.A. Nye, D-Y Shih, D.S. Zupanski-Nielsen, "Interconnections for Flip-Chip using Lead-free Solders and Having Reaction Barrier Layers," US Patent No.7,410,833 B2, Aug.12, (2008).

76. J. Guo, L. Zhang, A. Xian, J.K. Shang, "Solderability of Electrodeposited Fe-Ni Alloys with Eutectic SnAgCu Solders," J. Mater. Sci. Tech., Vol.23, No.6, p.811, (2007).

77. G. Dietz, H.D. Schneider, J. Phys; Condens. Matter, Vol.2, p.2169, (1990).

78. J.W. Jang, P.G. Kim, K.N. Tu, D.R. Frear, P. Thompson, J. Appl. Phys. Vol.85, p.8456, (1999).

79. Y. C. Sohn, Jin Yu, S. K. Kang, W. K. Choi, D. Y. Shih, "Study of the Reaction Mechanism Between Electroless Ni-P and Sn and its Effect on the Crystallization of Ni-P," J. Mat's Res, Vol.18, No.1, pp.4-7, January, (2003).

80. Y.C. Sohn, Jin Yu, S.K. Kang, D.Y. Shih, and T.Y. Lee, "Spalling of Intermetallic Compounds During the Reaction Between Lead-free Solders and Electroless Ni-P Metallization," J. Materials Research, Vol.19, No.8, pp.2428-36, (2004).

81. Y.C. Sohn, J. Yu, S.K. Kang, D.Y. Shih, T.Y. Lee, "Effect of Intermetallics Spalling on the Mechanical Behavior of Electroless Ni(P)/Pb-free Solder Interconnection," Proc. 55th ECTC, pp.83-88, (2005).

82. W.K. Choi, S.K. Kang, Y.C. Sohn, D.Y. Shih, "Study of IMC Morphologies and Phase Characteristics Affected by the Reactions of Ni and Cu Metallurgies with Pb-Free Solder Joints," *Proc. 53rd Elec. Comp. & Tech Conf*, New Orleans, LA, CA, pp.1190-96, (2003).

83. W.T. Chen, C.E. Ho, C.R. Kao, "Effects of Cu Concentration on the Interfacial Reactions between Ni and Sn-Cu Solders," J. Mater. Res, Vol.17, No.2, p.263, (2002).

84. J.Y. Tsai, C.R. Kao, "The Effect of Ni on the Interfacial Reaction between Sn-Ag Solder and Cu Metallization," *Proc 4th International Symposium on Electronic Materials and Packaging*, Kaohsiung, Taiwan, Dec. 2002, p. 271, (2002).

85. W.K. Choi, J.H. Kim, S.W. Jeong, H.M. Lee, "Interfacial Microstructure and Joint Strength of Sn-3.5Ag-X (X=Cu, In, Ni) Solder Joint," *J. Mater. Res.*, Vol. 17, No. 1, p.43, (2002).

86. D.Q. Yu, J. Zhao, L. Wang, "Improvement on the Microstructure Stability, Mechanical and Wetting Properties of Sn-Ag-Cu Lead-free Solder with the Addition of Rare Earth Elements," *J. Alloys and Comp.*, Vol. 376, No. 1/2, pp. 170-175, (2004).

87. K.S. Kim, S.H. Huh, K. Suganuma, "Effects of Fourth Alloying Additive on Microstructure and Tensile Properties of Sn-Ag-Cu and Joints with Cu," *Microelectron. Reliab.*, Vol. 43 pp. 259-267 (2003).

88. I.E. Anderson, J.L. Harringa, "Suppression of Void Coalescence in Thermal Aging of Tin-Silver-Copper-X Solder Joints," *J. Electron. Mater.*, Vol. 35, No. 1, pp. 94-106, (2006).

89. M.J. Rizvi, Y.C. Chan, C. Bailey, H. Lu, M.N. Islam, "Effects of Adding 1 wt% Bi into the Sn-2.8Ag-0.5Cu Solder Alloy on the Intermetallic Formation with Cu Substrate during Soldering and Isothermal Aging," *J. Alloys and Comp.*, Vol. 407, pp. 208-214, (2006).

90. S.K. Kang, D.Y. Shih, D. Leonard, D.W. Henderson, T. Gosselin, S.I. Cho, J. Yu, W.K. Choi, "Controlling Ag_3Sn Plate Formation in Near-Ternary-Eutectic Sn-Ag-Cu Solder by Minor Zn Alloying," *J. the Minerals, Metals and Materials (JOM),* Vol. 56, p.34, (2004).

91. I. de Sousa, D.W. Henderson, L. Patry, S.K. Kang, D.Y. Shih, "The Influence of Low Level Doping on the Thermal Evolution of SAC Alloy Solder Joints with Cu Pad Structures," *Proc 56th Electronic Components and Technology Conf*, San Diego, CA, p.1454, (2006).

92. M.G. Cho, S.K. Kang, D.-Y. Shih, H.M. Lee, “Effects of Minor Addition of Zn on Interfacial Reactions of Sn-Ag-Cu and Sn-Cu Solders with Various Cu Substrates during Thermal Aging,” *J. Electron. Mater.*, Vol. 36, No. 11, pp. 1501-1509, (2007).

93. Y.K. Jee, J. Yu, Y.H. Ko, “Effects of Zn Addition on the Drop Reliability of Sn-3.5Ag-xZn/Ni(P) Solder Joints,” *J. Mater. Res.*, Vol. 22, No. 10, pp. 2776-2784, (2007).

94. M. Lu, P. Lauro, D.Y Shih, S.K. Kang, S.H. Chae, and S.K. Seo, “The effects of Cu, Ag Compositions and Zn doping on the Electromigration Performance of Pb-free Solders,” Proc. 2009 ECTC, San Diego, May 26-29, p.922, (2009).

95. M.G. Cho, S. Seo, H.M. Lee; “Wettability and Interfacial Reactions of Sn-based Pb-free Solders with Cu-xZn Alloy Under Bump Metallurgies,” J. Alloys Compd, v.474, p.510, (2009).

96. S. K. Kang, M.G. Cho, D-Y Shih, S.K. Seo, H.M. Lee, “Controlling the Interfacial Reactions in Pb-free Interconnections by Adding Minor Alloying Elements to Sn-rich Solders,” Proc. 58th ECTC, p.478, (2008).

97. T. Sawamura, H. Komiya, T. Inazawa, F. Nakagawa, “Pb-free Soldering Alloy,” US Patent No.6,692,691B2, Feb. 17, (2004).

98. W. Liu, P. Bachorik, N.C. Lee, “The Superior Drop Test Performance of SAC-Ti Solders and its Mechanism,” Proc. 58th ECTC, p.452, (2008).

99. G.Y. Li, B.L. Chen, J.N. Tey, “Reaction of Sn-3.5Ag-0.7Cu-xSb Solder with Cu Metallization during Reflow Soldering,” IEEE Trans. Elec. Pack. Manuf. Vol.27, No.1, p.1521, (2004).

100. H.T Lee, H.S. Lin, C.S. Lee, P.W. Chen, “Reliability of Sn-Ag-Sb lead-free solder joints,” Mat’s Sci. & Eng. A, 407, p.36-44, (2005).

101. J.H. Lau, “*Low Cost Flip Chip Technologies*,” McGraw-Hill, New York, p. 183, (2000).

102. C. Zhang, J.K. Lin, Li Li, “Thermal Fatigue Properties of Pb-free Solders on Cu and NiP Under Bump Metallurgies,” Proc. 51st ECTC, p.463, (2001).

103. S. Terashima, Y. Kariya, T. Hosoi, M. Tanaka, “Effect of Silver Content on Thermal Fatigue Life of Sn-xAg-0.5Cu Flip-Chip Interconnects,” J. Elec. Mat’s, vol.32, no.12, p.1527, (2003).

104. S.K. Kang, P. Lauro, D-Y Shih, D.W. Henderson, J. Bartelo, T. Gosselin, S.R. Cain, C. Goldsmith, K. Puttlitz, T.K. Hwang, W.K. Choi, “The Microstructure, Thermal Fatigue, and Failure Analysis of Near-Ternary Eutectic Sn-Ag-Cu Solder Joints,” Materials Transactions (The Japan Inst of Metals), Vol.45, No.3 pp.695-702, (2004).

105. S.K. Kang, P. Lauro, D-Y Shih, D.W. Henderson, T. Gosselin, J. Bartelo, S.R. Cain, C. Goldsmith, K. Puttlitz, T.K. Hwang, “Evaluation of Thermal Fatigue Life and and Failure

Mechanism of Sn-Ag-Cu Solder Joints with Reduced Ag Contents," Proc. 54th ECTC, p.661, (2004).

106. B. Arfaei, Y. Xing, J. Woods, N. Wolcott, P. Tumne, P. Borgesen, E. Cotts, "The Effect of Sn Grain Number and Orientation on the Shear Fatigue Life of SnAgCu Solder Joints," Proc. 58th ECTC, p.459, (2008).

107. H. Quinones, A. Babiarz, "Flip Chip, CSP, and WLP Technologies: A Reliability Perspective," IMAPS Nordic, p.xxx, September, (2001).

108. S.Y. Jang, S.M. Hong, M.Y. Park, D.O. Kwok, J.W. Jeong, S.H. Roh, Y.J. Moon, "FCOB Reliability Study for Mobile Applications," Proc. 2004 ECTC, p.xxx, (2004).

109. A. Syed, T.S. Kim, S.W. Cha, J. Scanlon, C.G. Ryu, "Effect of Pb-free Alloy Composition on Drop/Impact Reliability of 0.4, 0.5, 0.8mm Pitch Chip Scale Packages with NiAu Pad Finish," Proc. 2007 ECTC, p.951, (2007).

110. A. Farris, J. Pan, A. Liddicoat, B.J. Toleno, D. Maslyk, D. Shanggun, J. Bath, D. Willie, D.A. Geiger, "Drop Test Reliability of Lead-free Chip Scale Packages," Proc. 2008 ECTC, p.1173, (2008).

111. T.C. Chiu, K. Zeng, R. Stierman, D. Edwards, K. Ano, "Effect of Thermal Aging on Board Level Drop Reliability for Pb-free BGA Packages," Proc. 2004 ECTC, p.1256, (2005).

112. M. Date, T. Shoji, M. Fujiyoshi, K. Sato, K.N. Tu, "Impact Reliability of Solder Joints" Proc. 2004 ECTC, p.668, (2004).

113. P.Borgesen, L. Yin, R. Kondos, D.W. Henderson, G. Servis, J. Therriault, J. Wang, K. Srihari, "Sporadic Degradation in Board Level Drop Reliability – Those Aren't All Kirkendall Voids!", Proc. 2007 ECTC, p.136, (2007).

114. Z. Mei, M. Ahmad, M. Hu, and G. Ramakrishna, "Kirkendall Voids at Cu/Solder Interface and Their Effects on Solder Joint Reliability," Proc. of 55th Electronic Component and Technology Conference, pp. 1256-1262, 2005.

115. M. Amagai, Y. Toyoda, T. Ohnishi, S. Akita, "High Drop Test Reliability: Lead-free Solders," Proc. 2004 ECTC, p.1304, (2004).

116. H. Kim, M. Zhang, C.M. Kumar, D. Suh, P. Liu, D. Kim, M. Xie, Z. Wang, "Improved Drop Reliability Performance with Lead Free Solders of Low Ag Content and Their Failure Modes," Proc. 2007 ECTC, p.962, (2007).

117. J. Sylvestre, and A. Blander, V. Oberson, E. Perfecto, and K. Srivastava," The Impact of Process Parameters on the Fracture of Device Structures", *Proc. of the 58th Electronic Components and Technology Conf*, pp.82-88, 2008.

118. K. Zeng, K.N. Tu," Six cases of reliability study of Pb-free solder joints in electronic packaging technology," Mat's Sci. & Eng, R, v.38, pp.55-105, (2002).

119. M. Lu, D-Y Shih, r. Polastre, C. Goldsmith, D.W. Henderson, H. Zhang, M.G. Cho, "Comparison of Electromigration Performance for Pb-free Solders and Surface Finishes with Ni UBM," Proc. 58th ECTC, p.360, (2008).

120. S-K Seo, S. K. Kang, D-Y Shih, and H.M. Lee, "The Evolution of Microstructure Microhardness of Sn-Ag and Sn-Cu Solders during High Temperature Aging", *Microelectronics Reliability*, Vol.49, p.288, (2009).

121. I. A. Blech, J. Appl. Phys. **47**, 1203, 1976.

122. M. Lu, D.-Y. Shih, P. Lauro, and C. Goldsmith," Blech effect in Pb-free flip-chip solder joint", J. Appl. Phycs. Lett. **94**, 011912, 2009.

123. M Lu, D.-Y. Shih, S. K. Kang, C. Goldsmith, and P. Flaitz," Effect of Zn doping on SnAg solder microstructure and electromigration stability", J. Appl. Phys. **106**, 053509, 2009.

124. K.N. Tu,"Electromigration in Flip chip Solder Joint", Chap. 9, in Solder Joint Technology, pp. 245-287, Springer, 2007.

125. C. Chen, and S.W. Liang,"Electromigration issues in lead-free solder joints", in Lead-Free Electronic Solders, pp.259-268, Springer, 2007.

126. S. Lee, X. Guo, and C.K. Ong,"Electromigration Effect on Cu-pillar (Sn) Bumps", Electronics Packaging Technology Conf. pp.135-139, 2005.

127. Y. Kariya et al., "Tin pest in lead-free solders", *Soldering & Surface Mount Technol.* P.39, 2000.

128. D.W. Henderson, T.A. Gosselin, C.C. Goldsmith, K.J. Puttlitz, S.K. Kang, D.Y. Shih, W.K. Choi, "Lead-free Tin-Silver-Copper Alloy Solder Composition," US Patent No.6805974, issued October, 19, 2004.

129. J. U. Knickerbocker, P. S. Andry, B. Dang, R. R. Horton, M. J. Interrante, C. S. Patel, R. J. Polastre, K. Sakuma, R. Sirdeshmukh, E. J. Sprogis, S. M. Sri-Jayantha, A. M. Stephens, A. W. Topol, C. K. Tsang, B. C. Webb, and S. L. Wright, "Three-dimensional silicon integration," IBM J. Res. & Dev., vol. 52, no. 6, pp. 553-569, 2008.

130. J. D. Meindl, J. A. Davis, P. Zarkesh-Ha, C. S. Patel, K. P. Martin, and P. A. Kohl, "Interconnect opportunities for gigascale integration," IBM J. Res. & Dev., vol. 46, pp. 245-263, 2002.

131. B. Dang, S. L. Wright, P. S. Andry, E. J. Sprogis, C. K. Tsang, M. J. Interrante, B. C. Webb, R. J. Polastre, R. R. Horton, C. S. Patel, A. Sharma, J. Zheng, K. Sakuma, J. U. Knickerbocker, "3D chip stacking with C4 technology," IBM J. Res. & Dev., vol. 52, no. 6, pp. 599-609, 2008.

132. B. Dang, S. Wright, P. Andry, E. Sprogis, S. Ketkar, C. Tsang, R. Polastre, J. Knickerbocker," 3D Chip Stack with Integrated Decoupling Capacitors" 59th Electronic Component and Technology Conference, pp. 1-5, May (2009)

133. A. Yu, J. Lau, S. Ho, A. Kumar, W. Hnin, D. Yu, M. Jong, V. Kripesh, D. Pinjala, D. Kwong, " Study of 15 µm Pitch Solder Microbumps for 3D IC Integration", 59th Electronic Component and Technology Conference, pp. 6-10, May (2009).

134, A. Krupp et al., "3D Integration with ICV-Solid Technology," Conference on 3D Architecture for Semiconductor and Packaging, Tempe, AZ, June, (2005).

135. P. Ramm, "Vertical Integration technologies," Workshop on 3D Integration of Semiconductor Devices, San Diego, October, (2004).

136. K. Lee, " The Next Generation Package Technology for Higher Performance and Smaller Systems" Conference on 3D Architecture for Semiconductor and Packaging, Burlingame, CA, Oct. (2006).

137. L. Schaper, 53rd Electronic Component and Technology Conference, pp.631-633, May (2003).

138. L. Schaper et al., Trans. IEEE Adv. Packaging, V. 28, No. 3, pp.356-366, Aug. (2005)

139. P. Ramm, "Vertical Integration technologies", Workshop on 3D Integration of Semiconductor Devices, San Diego, October, (2004).

140. Y. Wang, T. Suga, "20-µm Pitch Au Micro-bump Interconnection at Room Temperature in Ambient Air," 58th Electronic Component and Technology Conference, pp. 944-949, May (2008).

141. R. Chanchani," 3D Integration Technology- An Overview", Materials for Advanced Packaging, Springer Science, (Ed, by D. Lu and C.P. Wong (2009).