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Graphene Field-Effect Transistors with Self-Aligned Gates

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We present a new device fabrication process that produces graphene-based field-effect transistors with self-aligned gates. This process utilizes the inherent nucleation inhibition of atomic-layer-deposited films with the graphene surface to achieve electrical isolation of the gate electrode from the source/drain electrodes while maintaining electrical access to the graphene channel. Self-alignment produces access lengths of 15 - 20 nm, which allows for improved device stability, performance, and a minimal normalized contact resistance of 540 Ω μm.

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Due to its unique electronic properties, graphene is a material of intense investigation for both scientific and technological applications.[1] Specifically, the high mobility of charge carriers in graphene combined with the ability to modulate the carrier concentration by an external electric field has made graphene-based field-effect transistors (FETs) promising candidates for future high frequency applications.[2] Recently, graphene FETs have been demonstrated to operate at cut-off frequencies (f_T) as high as 100 GHz.[3,4] Additional increases in f_T will be achieved through further improvement of both the constituent device materials and the device design. One of the critical factors limiting the ultimate performance of graphene FETs is the parasitic series resistance between the source/drain contacts and the gated graphene channel. While these access regions serve to reduce the parasitic capacitance between the gate and the source/drain electrodes, their resistance results in a lower current that hinders the device performance. It is therefore desirable to minimize the access resistance (R_A) as much as possible. This is especially crucial in the downscaling of graphene devices because R_A can become comparable to the gated channel resistance (R_G) and adversely affect the device behavior. In conventional silicon-based FETs, the access resistance is reduced by doping these ungated regions through ion implantation.[5] The two-dimensional structure of graphene negates the use of this technique, which would inevitably damage the fragile carbon lattice.[6] Alternative methods of reducing R_A are therefore needed.

Previous attempts to minimize R_A employed a dual-gate configuration that modulates R_A via electrostatic doping.[7] While this led to a twofold reduction of the total parasitic series resistance (R_S), it uses global bottom-gating of the substrate, and can therefore only be implemented with transferred or mechanically exfoliated graphene.

Furthermore, the ability to modulate R_A implies undesirable variability in the device characteristics, and this configuration may be impractical for high-frequency applications due to the additional capacitance contributed by the bottom-gate. Here, we employ self-aligned gating to minimize R_A in which the source/drain and gate electrode edges are automatically positioned so that no overlap or significant gap exists between them. Since it does not require dual-gating, this approach is universally applicable to all sources of planar graphene, including epitaxial. As compared to more conventional device configurations, we find that self-alignment results in a significant improvement in device performance.

Graphene FETs are fabricated from mechanically exfoliated flakes of graphene.[8] These flakes are deposited on 300 nm-thick SiO_2 films that were thermally grown on heavily p-doped Si substrates. A schematic of the device fabrication procedure is shown in Figure 1. The graphene is first coated with a 25 nm-thick gate dielectric. For reasons of both simplicity and chemical compatibility, Al_2O_3 is chosen to be the gate dielectric material for these experiments, and a combination of Al evaporation and Al_2O_3 atomic layer deposition (ALD) are used as the deposition techniques.[9] Top-gate electrode stacks of 0.5 nm Ti/20 nm Pd/40 nm Au are then patterned onto the oxide surface. These electrodes serve as masks for subsequent etching of the Al_2O_3, which is done in a 1:3 solution of H_3PO_4:H_2O at 300 K ($\backsim$ 0.4 nm/min). Once the oxide is completely etched away from the unprotected areas, the devices are rinsed with copious amounts of water and isopropanol, and then undergo a 425 K anneal in forming gas for 5 min to further clean the exposed graphene surfaces (Fig. 1a). This is followed by a second ALD step of 10 nm Al_2O_3 deposition that electrically isolates the gate electrode from the self-aligned

source/drain electrodes. This is the most innovative step of the fabrication process because it exploits the inherent chemical inertness of the graphene surface to ALD precursors.[10,11] While the 10 nm-thick oxide conformally coats the gate electrode and the sidewalls of the gate dielectric, oxide nucleation on the exposed graphene surface is sporadic, presumably due only to the random presence of structural defects and residual contaminants on the surface (Fig. 1b). The large portion of the graphene surface that is left uncoated allows for direct electrical contact with the source/drain electrodes, which are deposited by electron-beam evaporation. With a total thickness that is approximately half that of the gate dielectric to avoid leakage currents (0.5 nm Ti/4 nm Pd/5 nm Au), these electrodes are aligned by the edges of the gate, and therefore minimize the length of the access regions (Fig. 1c). Device fabrication is completed with the deposition of thicker source/drain metal pads (0.5 nm Ti/20 nm Pd/40 nm Au) and etching of the exposed graphene with O_2 plasma to define the channel dimensions (Fig. 1d). This process differs from what has previously been done in carbon nanotube devices, where lift-off techniques were used to achieve self-alignment.[12] The difference is principally due to the poor adhesion of the dielectric to the graphene surface, which does not allow for satisfactory lift-off behavior. This problem is not encountered in single nanotube devices because good adhesion is made with the supporting substrate.

An SEM image of a completed device is shown in Figure 1e. Here, the isolation layer of Al_2O_3 has been removed in order to evaluate the length of the access region (L_A), which is found to be L_A = 15 - 20 nm. Also, the random, non-continuous nucleation of the Al_2O_3 isolation layer on the graphene surface can be seen under the self-aligned source/drain electrodes. It is clear from this that continuous pathways of exposed,

electrically contacted graphene are accessible up to the edge of the gate. For reference, the critical resistive components and lengths of these graphene FETs are shown in Figure 1f. Unless otherwise indicated, all measurements presented herein are made in vacuum (5×10^{-6} Torr) at 300 K with a drain bias of $V_D = 100$ mV.

Transfer characteristics of a graphene FET with a self-aligned gate are shown in Figure 2a. Using the Si substrate as a global bottom-gate allows for dual gating of the device and subsequent determination of the top-gate dielectric capacitance. The Dirac voltage (V_{Dirac}), defined as the top-gate voltage (V_{TG}) at the point of minimum conductance, is linearly dependent on the bottom-gate voltage (V_{BG}) (Fig. 2a inset). The slope that is extrapolated from this linear shift gives the ratio of the top-gate and bottom-gate capacitances (C_{TG}/C_{BG}). With the capacitance of 300 nm SiO_2 known to be $C_{BG} = 11.6$ nF/cm^2 and the slope determined to be 32, the top-gate dielectric capacitance is found to be $C_{TG} = 370$ nF/cm^2, in agreement with previous studies that utilize this gate dielectric.[7,13] The most striking feature of the transfer curves is that the drain current at V_{Dirac} is constant, independent of V_{BG}. This is a direct result of the self-alignment, and is in contrast to what is observed in devices that have appreciable access lengths.[9] Further illustration of this can be seen in Figure 2b, where the normalized resistance (R/R_{min}) at V_{Dirac} of four graphene FETs with gate lengths of $L_G = 1$ μm are compared. Two of the devices are self-aligned and $L_A = 1$ μm for the other two. It can clearly be seen that the change in R/R_{min} for the $L_A = 1$ μm devices is dramatic (as much as 180%), while the change in R/R_{min} for the self-aligned devices is minimal (less than 8%). Eliminating the contribution of R_A through self-alignment greatly increases the consistency of the device performance.

The properties of two graphene FETs, one self-aligned and the other with L_A = 1 μm, with identical channel widths and channel lengths (W = 1.9 μm, L_G = 1 μm) that were fabricated on the same graphene flake are shown in Figure 3. The transfer characteristics and corresponding transconductances of these devices show the benefits of self-alignment in this one-to-one comparison. The self-aligned device exhibits an I_{ON}/I_{OFF} ratio of 3 and a maximum transconductance (g_m) of 56 μS, while I_{ON}/I_{OFF} = 1.7 and g_m = 11 μS for the non-aligned device (Fig. 3a). These transconductances translate into device mobilities, $\mu_{DEV} = g_m L/V_D W C_{TG}$, of 270 cm^2/Vs for the non-aligned device and 1360 cm^2/Vs for the self-aligned device. The improvement afforded by self-alignment is also seen by comparing the output characteristics of the devices, where the maximum drive current increases from 0.73 mA for the non-aligned device to 2.35 mA for the self-aligned device (Fig. 3b). It should be mentioned that the maximum gate leakage of the self-aligned device measured during these output sweeps did not exceed 300 fA, signifying good electrical isolation between the gate and source/drain electrodes.

A deeper understanding of the devices presented in Figure 3 can be achieved by fitting their resistance profiles (R_T) to the expression,

$$R_T = R_S + \frac{L_G}{We\mu_{FE}\sqrt{n_o^2 + n^2}} \quad (1)$$

where e is the electron charge, n is the field-modulated carrier concentration, n_o is the residual carrier concentration, and μ_{FE} is the intrinsic field-effect mobility of the gated graphene channel (Fig. 3c).[9] Also, R_S consists of contributions from both the access regions and contact regions, $R_S = 2R_A + 2R_C$ (Fig. 1f). Fitting the experimental

resistances to this expression allows for extrapolation of μ_{FE} and R_S. Due to contact-induced conduction asymmetry,[14] R_T is fitted separately for electron ($V_{TG} - V_{Dirac} > 0$) and hole ($V_{TG} - V_{Dirac} < 0$) transport. While the extrapolated values of μ_{FE} for both devices are in reasonable agreement, 3,000 ± 500 cm^2/Vs for holes and 2,500 ± 500 cm^2/Vs for electrons, the corresponding values of R_S greatly differ, 2.48 kΩ for the non-aligned device and 0.57 kΩ for the self-aligned device. Since the devices are identical with the exception of the access regions, the difference between these values gives the resistance of the access region in the non-aligned device, $2R_A$ = 1.91 kΩ. This agrees well with the experimentally measured resistance difference between the two devices of 2.1 ± 0.23 kΩ, validating the extrapolated values (Fig. 3c). It is clear from these results that the improvement achieved through self-alignment is due to a significant reduction of the parasitic access resistance. Furthermore, since L_A is small in the self-aligned device, the series resistance of this device can be assumed to be dominated by the contacts, $R_S = 2R_C$ = 0.57 kΩ. This gives a normalized contact resistance of R_CW = 540 Ω μm, which is slightly less than the previously reported minimum graphene contact resistance of 800 ± 200 Ω μm.[15]

In summary, a process for fabricating graphene FETs with self-aligned gates has been established. The inherent inertness of the graphene surface to ALD precursors is exploited in order to isolate the source/drain electrodes from the gate electrode while still allowing for electrical contact to the graphene channel. This process greatly reduces the access length to below 20 nm, increasing the overall stability of the device characteristics, and reducing the total parasitic series resistance to the contact-dominated

limit of 540 Ω μm. It is hoped that this process will be utilized to further improve the performance of high-frequency graphene FETs.

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[1] A.H. Castro Neto, F. Guinea, N.M.R. Peres, K.S. Novoselov, and A.K. Geim, Rev. Mod. Phys. **81**, 109 (2009).

[2] K.I. Bolotin, K.J. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Hone, P. Kim, and H.L. Stormer, Solid State Commun. **146**, 351 (2008).

[3] Y.-M. Lin, K.A. Jenkins, A. Valdes-Garcia, J.P. Small, D.B. Farmer, and Ph. Avouris, Nano Lett. **9**, 422 (2008).

[4] Y.-M. Lin, C. Dimitrakopoulos, K.A. Jenkins, D.B. Farmer, H.-Y. Chiu, A. Grill, and Ph. Avouris, Science **327**, 662 (2010).

[5] R.B. Fair, Proc. IEEE **86**, 111 (1998).

[6] F. Giannazzo, S. Sonde, V. Raineri, and E. Rimini, Appl. Phys. Lett. **95**, 263109 (2009).

[7] Y.-M. Lin, H.-Y. Chiu, K.A. Jenkins, D.B. Farmer, Ph. Avouris, A. Valdes-Garcia, IEEE Electron Device Lett. **31**, 68 (2010).

[8] K.S. Novoselov, A.K. Geim, S.V. Morozov, D. Jiang, Y. Zhang, S.V. Dubonos, I.V. Grigorieva, and A.A. Firsov, Science **306**, 666 (2004).

[9] S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc, and S.K. Banerjee, Appl. Phys. Lett. **94**, 062107 (2009).

[10] Y. Xuan, Y.Q. Wu, T. Shen, M. Qi, M.A. Capano, J.A. Cooper, and P.D. Ye, Appl. Phys. Lett. **92**, 013101 (2008).

[11] X. Wang, S.M. Tabakman, and H. Dai, J. Am. Chem. Soc. **130**, 8152 (2008).

[12] A. Javey, J. Guo, D.B. Farmer, Q. Wang, E. Yenilmez, R.G. Gordon, M. Lundstrom, and H. Dai, Nano Lett. **4**, 1319 (2004).

[13] For the sake of accuracy, C_{TG}/C_{BG} is independently determined for every device measured.

[14] B. Huard, N. Stander, J.A. Sulpizio, and D. Goldhaber-Gordon, Phys. Rev. B **78**, 121402(R) (2008).

[15] S. Russo, M.F. Craciun, M. Yamamoto, A.F. Morpurgo, and S. Tarucha, Physica E **42**, 677 (2010).

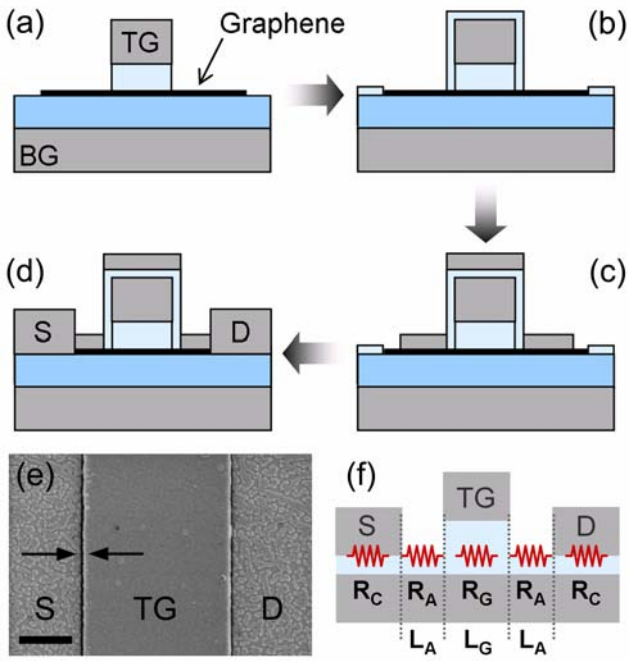

Figure 1. (Color Online) a) After etching the exposed Al_2O_3, b) an additional layer of Al_2O_3 is deposited to isolate the gate electrode. While nucleation of this layer is continuous on the gate dielectric and gate electrode, it is not on the graphene surface. c) The source/drain electrodes are then deposited, which are aligned with the contours of the isolated gate electrode edges. d) Thicker source/drain pads are deposited for probing. e) The top-view SEM of a self-aligned device reveals that the separation of the source/drain and gate electrodes is 15 - 20 nm (arrows). The non-continuous isolation oxide layer can also be seen on the source/drain regions (400 nm scale bar). f) Diagram of a graphene FET showing the critical lengths and resistances of the device.

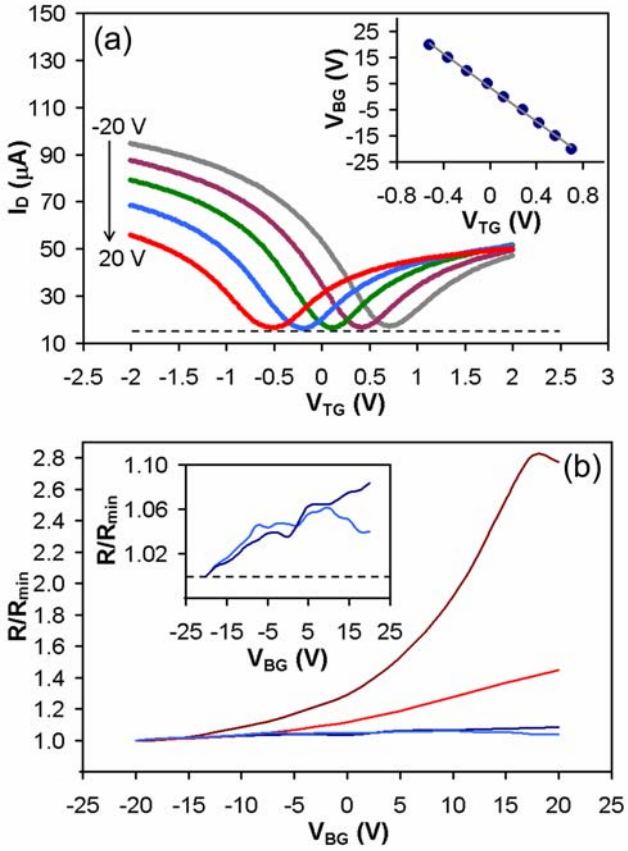

Figure 2. (Color Online) a) Transfer characteristics of a self-aligned device. The bottom-gate is swept between -20 V and 20 V in 10 V steps. The minimum value of I_D does not substantially change within this sweep range, as denoted by the dashed line. The Dirac voltage varies linearly with the top and bottom-gate voltages (inset). b) The resistance at the Dirac voltage normalized by its minimum value shows that the self-aligned devices (blue) are insensitive to electrostatic doping from the bottom gate, while non-aligned devices exhibit appreciable sensitivity (red). An adjusted scale shows the minor resistance changes of the two self-aligned devices (inset).

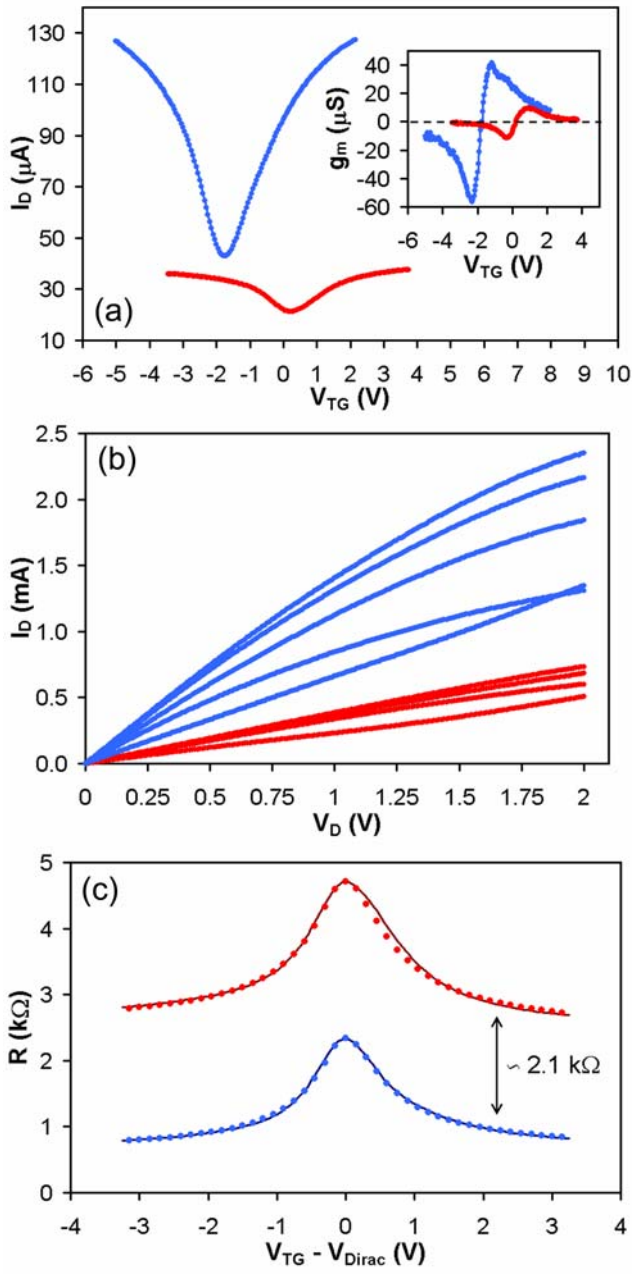

Figure 3. (Color Online) Comparison of a self-aligned device (blue) to a device in which L_A = 1 μm (red). a) Transfer characteristics reveal a dramatic improvement in I_{ON}/I_{OFF} and transconductance (inset) when self-alignment is employed. b) The output characteristics of the self-aligned device are also superior. Here, V_{TG} is swept from -4 V

to 4 V in 2 V steps. c) The measured resistance profiles (solid lines) show a 2.1 kΩ reduction of the parasitic resistance in the self-aligned device. The values of the parasitic resistances are found by fitting these profiles to Equation 1 (circles).