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Co-Integration of III-V with Si for Scaled CMOS

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Relentless scaling of CMOS transistors has continued despite formidable challenges in lithography and processing. However, scaling to sub-20-nm dimensions presents unique challenges that threaten to end Moore's scaling within the next decade (Table 1). The increase in the drive current in scaled devices for faster switching speeds at lower supply voltages has largely occurred at the expense of an exponentially growing leakage current, thus leading to a large standby power dissipation. This strategy has worked well until recently because our computation needs have been dominated primarily by high performance end products (mainframes, desktops, PCs). However, with the recent shift of paradigm in user choice towards low form-factor hand-held gadgets, performance requirements for computing have shifted towards low-power consumption (Figure 1). Current exploration of high carrier mobility channels is being fueled by ever reducing low-power requirements at high performance for future products.

While changing the device architecture (e.g. FinFET, Trigate, Nanowire) can improve the electrostatics of a transistor, fundamental improvement in device performance arises from the carrier mobility. Novel techniques including strain engineering have been applied to enhance electron and hole mobilities in Si, but such improvement is near saturatation. Further carrier mobility enhancement has to be achieved intrinsically by high mobility channel materials. Obvious choice of materials thus includes III-Vs for electrons and Ge containing Si for holes.

In this talk we will discuss options for 14 nm and beyond CMOS scaling. The current CMOS roadmap is on track to use Si for both 14 and 11 nm technology nodes. Further scaling to 8 nm node and beyond may require both Si and III-V channel materials. There are multiple III-V device options that are being pursued (Figure 2) How soon the inclusion of III-Vs occurs in future CMOS will depend on the pace of progress over next 3-5 years in addressing the following fundamental challenges: (1) surface passivation; (2) overcoming lower density of states limitations; (3) scaling with an acceptable I_{ON}/I_{OFF} ratio; (4) developing an appropriate HKMG stack; (4) developing III-V p-channel alternatives; and (5) development high quality selective III-V n-regions on a Si substrate. Furthermore, maturity of III-V tooling infrastructure supporting this technology will be pivotal in deciding whether III-V based CMOS technology is ready for prime time.

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Table 1.

Element	Scaling	Implication
Litho Shrink	0.7X Linear, historical **0.8X, Future**	30% Lower power **20%**
Device FPG	~30-35% faster, historical **~20%, Future**	~30% Frequency and/or Lower Power **Less F or P**

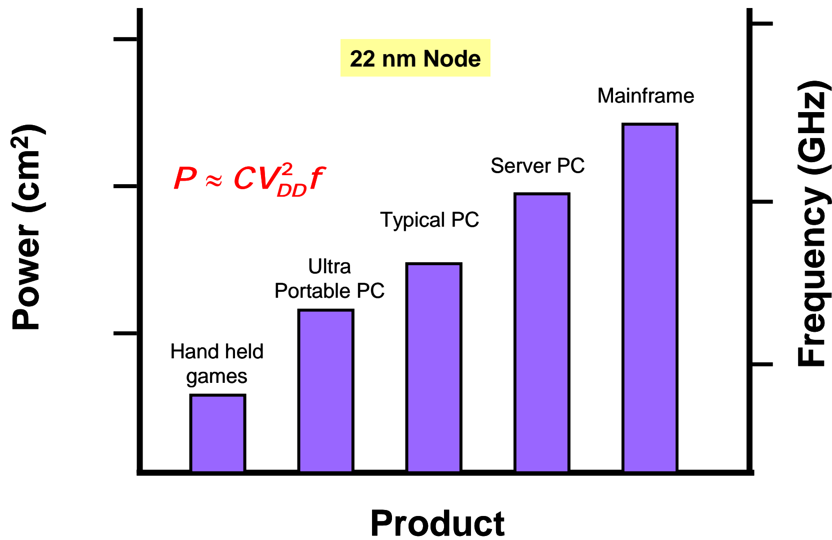

Figure 1: Power-performance for various products

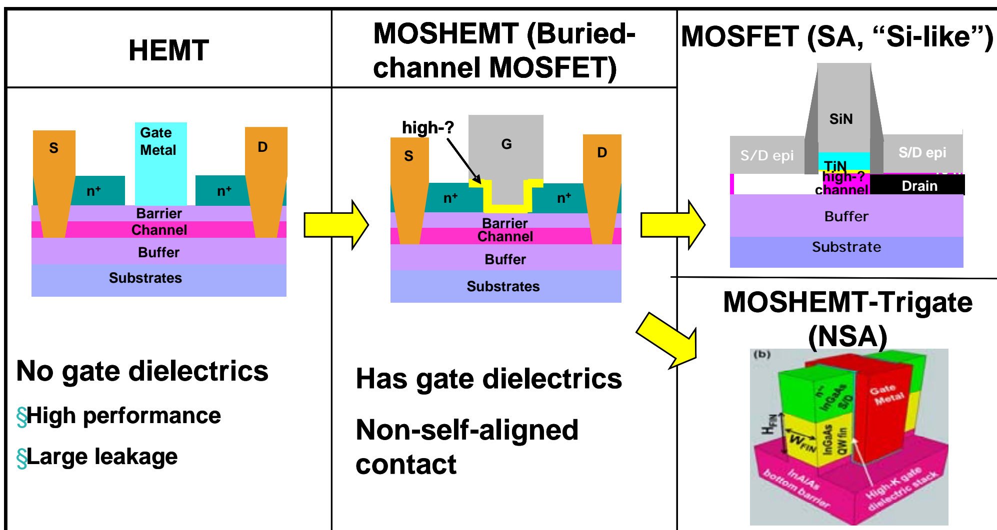

Figure 2: Various III-V device options for scaled CMOS