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Sequential Lateral Solidification of Silicon Thin Films on Low-k Dielectrics for Low Temperature Integration

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We present the excimer laser crystallization of amorphous silicon on a low dielectric constant (low-k) insulator for VLSI monolithic 3D integration and demonstrate that low dielectric constant materials are suitable substrates for 3D integration through laser crystallization of silicon thin films. We crystallized 100 nm amorphous silicon on top of SiO_2 and SiCOH (low-k) dielectrics, at different material thicknesses (1 μm, 0.75 μm and 0.5 μm). The amorphous silicon crystallization on low-k material requires 35% less laser energy than on an SiO_2 dielectric. This difference is related to the the thermal conductivity of the two materials, in agreement with one dimensional simulations of the crystallization process. We analyzed the morphology of the material through defect-enhanced microscopy, Raman, and X-ray diffraction analysis. SEM micrographs show that polycrystalline silicon is characterized by micron-long grains with an average width of 543 nm for the SiO_2 sample and 570 nm for the low-k samples. Comparison of the Raman spectra does not show any major difference in film quality for the two different dielectrics, and polycrystalline silicon peaks are closely placed around 517 cm^{-1}. From X-ray diffraction analysis, the material crystallized on SiO_2 shows a preferential (1,1,1) crystal orientation. In the SiCOH case the (1,1,1) peak strength decreases dramatically and samples do not show preferential crystal orientation. A 1D finite element method simulation of the crystallization process on a back end of line structure, shows that interconnect lines experience a maximum temperature lower than 70°C also for the 0.5 μm dielectric, which is a favorable condition for monolithic 3D integration.

Excimer laser crystallization (ELC) is an important technique which achieves large grains polycrystalline thin film starting from an amorphous layer. One of the main advantage of the ELC process is the ability to fabricate polycrystalline silicon (polysilicon) material on top of temperature sensitive substrate, which allows integration of high performance thin film transistors (TFTs) without compromising the substrate integrity. Low temperature polysilicon TFTs have found particular application in the display industry[1–5], and are now attracting increasing attention in the Very Large Scale Integration (VLSI) area as path to achieving monolithic 3D integration.[6–8] One limitation to Back End Of Line (BEOL) 3D integration is the thermal budget of the metal interconnect. Cu interconnect lines are embedded in a stack of inter-level dielectric (IDL), which are fabricated in the BEOL process. The IDL is generally a low-k material because it reduces the parasitic capacitance between lines, which affects the operation frequency of the system. Integration in the BEOL process has a stringent thermal budget requirement, which limits the substrate temperature below 400°C to avoid structural damage of the metal lines and drift of the device parameters. While other techniques to deposit polysilicon layers exist, such as solid phase crystallization and metal induced crystallization, they require applying the same high temperatures to the whole wafer stack, which is impractical for monolithic 3D integration. ELC of amorphous silicon (a-Si) is an efficient way to achieve good quality polysilicon which, using a combination of high energy short time laser pulses, meets the Cu interconnect thermal budget requirements.

During the integration process, depending on the condition of the excimer laser (i.e. laser fluence, laser pulse width and number of shots), material crystallization can occur in a number of regimes, such as partial-melting, near-complete-melting (where super lateral growth occurs[9]), and complete-melting conditions. Each of these regimes leads to different material structure and grain sizes.[4,10] Our set of experiments uses an advanced ELC technique in which super lateral growth is achieved by controlling the physical dimensions of the molten area by proper optics in the beam path in a technique known as line-scan Sequential Lateral Solidification (SLS).[11–13] The excimer laser used is a Lambda-Physics operating at 308 nm (XeCl) with an effective pulse width of approximately 30 ns pulse duration and a repetition rate of 30 Hz. The laser beam is shaped into a line with a 3.4 μm by 5 cm area. Figure 1 represents the Line-Scan SLS process. During the first shot the irradiated area is completely melted and, upon cooling, grains nucleate from the liquid/solid interface from opposite fronts meeting in the middle of the line, creating a polycrystalline structure. Before the second shot the sample is translated by less than half beam-width and is irradiated once again. During the cooling process the grains seed again from the liquid/solid interface, where this time, they template from the structure formed during the previous shot.

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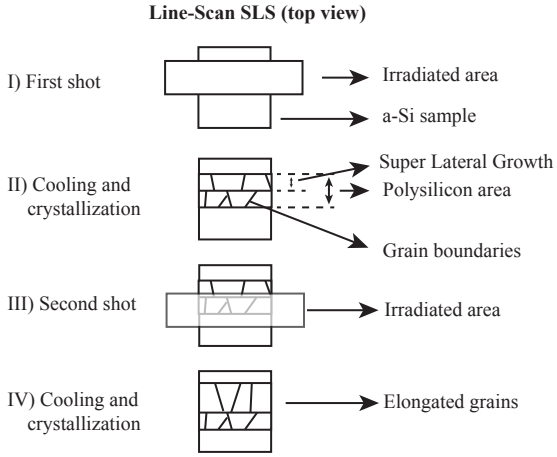

FIG. 1. Line-scan SLS process. I) Laser melts irradiated area; II) Grains nucleate from liquid/solid interface and meet in the middle of the melted area; III) Sample is translated by less than half beam width and irradiated again; IV) Grains nucleate templating from previous structure.

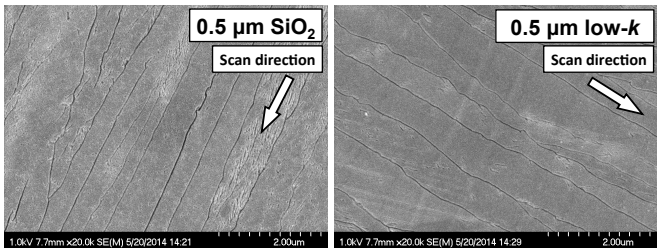

FIG. 2. SEM images of two Secco etched samples crystallized with Line-Scan SLS. The ELC material has very long grain along the laser scan direction, with an average width of 543 nm for the SiO_2 sample and 570 nm for the low-k.

Careful control of the wafer movement and laser repetition rate allows achieving relatively large and arbitrarily long grain polycrystalline structure.

Our starting substrates are six different silicon wafers; on three of them SiO_2 dielectric are deposited at different thicknesses (1 μm, 0.75 μm and 0.5 μm), and the other three have a low-k dielectric of the same three thicknesses. The low-k dielectric material has a dielectric constant (k) of 3.0 and is deposited by plasma enhanced chemical vapor deposition in a 200 mm chamber. The material is an organosilicate glass with a network structure of Si-O bonds and pendant Si-CH_3 groups, also referred to as a SiCOH dielectric. A 100 nm a-Si layer is then evaporated on top of the six wafers through Physical Vapor Deposition (PVD) sputtering technique. To drive out any trapped gas, all of the wafers are annealed at 350°C for 30 minutes, which is a temperature compatible with BEOL integration. All of the wafers undergo crystallization in an ambient environment at room temperature using the same laser setup. The only parameter adjusted between crystallization runs is the average laser fluence which is optimized for each dielectric. The laser intensity is directly measured, after successful crystallization, through an energy monitor that replaces the sample. Each measurement is the average intensity of 40 laser pulses. An average taken over 10 different measurements yields the estimated laser fluence, which is 974 mJ/cm^2 in the case of SiO_2 dielectric and 630 mJ/cm^2 for the SiCOH dielectric, a 35% reduction. The laser fluence does not need to be changed for crystallization on different thicknesses of the same dielectric.

TABLE I. Material parameters of the SiCOH and SiO_2 based dielectric.

Parameters	**SiCOH**	**SiO_2**
Dielectric constant [ ]	3.0	3.9
Thermal conductivity [W m^{-1} K^{-1}]	0.4	1.4
Density [g cm^{-3}]	1.4	2.2
Heat capacity [J K^{-1} g^{-1}]	0.636	0.730

Figure 2 shows two SEM pictures of the ELC material both with a SiO_2 and low-k dielectric for the thinnest layer. Secco etch is used to remove the grain defect providing contrast for the SEM picture. The crystallized material shows very long grains with grain boundaries parallel to the laser scan direction and an average width of 543 nm for the SiO_2 sample and 570 nm for the low-k sample.

Figure 3 shows the Finite Element Method (FEM) simulation (using COMSOL Multiphysics) of the 1D temperature evolution for different dielectric thicknesses during sample irradiation. The simulation starts with a laser pulse irradiating the sample at t = 100 ns, and further details are based on the approach by Förster and Vogt.[14] Table I lists the physical parameters of the dielectrics used in the simulation. While the density, thermal conductivity, and dielectric constant of the SiCOH correspond to measured values[15,16], the heat capacity is calculated starting from the SiO_2 sample using the ratio between the material density of the low-k and the SiO_2 as a scaling factor. In the SiO_2 case, the standard properties in the COMSOL Multiphysics library are used and listed in Table I for comparison. The inset in Figure 3 shows the material stack used in the simulation, which matches the substrate structure. The energy of the laser used in the FEM simulation is constant for all dielectric materials and thicknesses to highlight the influence of the dielectric on the maximum temperature reached by the a-Si thin film. The heat profiles for different thickness of the same dielectric show little difference in the maximum temperature reached, while the thickness has a great effect on the cooling rate of the a-Si layer, as shown in Figure 3. The density of the material impacts the maximum temperature reached during the process. This is consistent with our experimental observation that the lower thermal conductivity of the SiCOH allows achieving the a-Si melting temperature ($\sim$ 1167°C) at a lower laser fluence.

Figure 4 reports the Raman peak area ratio of the dif-

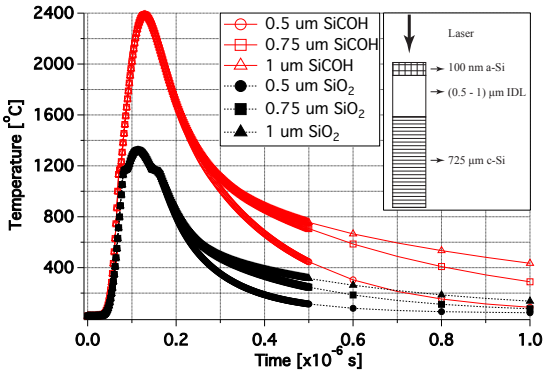

FIG. 3. 1D FEM simulation of the temperature evolution of the a-Si layer during the crystallization process on SiCOH and SiO_2 dielectrics at different thicknesses. The inset shows the simulation of the 2D version of the structure.

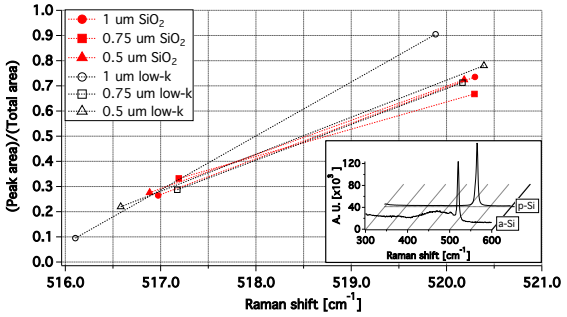

FIG. 4. Peak area intensity ratio of the Raman spectra for the different dielectric and relative thicknesses. The inset shows the comparison between the Raman spectra of the 0.5 μm low-k dielectric sample before and after crystallization.

ferent samples after crystallization, and the inset shows the Raman spectra of the 0.5 μm low-k sample before and after crystallization. The Raman spectrum of a-Si shows a broad peak around 480 cm^{-1}, which is characteristic of the material phase, and a second peak centered at 520 cm^{-1}, expected of crystalline silicon[17,18], which is attributed to the substrate. The Raman spectra of all of the crystallized samples have a single peak which is the convolution of the substrate contribution and the laser crystallized polycrystalline material contribution (peak around 517 cm^{-1})[19]. The analysis of both the Raman shift and Raman peak area ratio shows a consistent material in all the samples.

Figure 5 shows XRD spectra which reveal the crystallographic orientation of the grains from both SiO_2 and low-k samples. Due to the anisotropy of the grain the XRD spectra are collected with the X-ray beam impinging on the sample both on a parallel and perpendicular direction to the grain length, to check for possible preferential crystallization directions. The inset shows the diffraction scan from the as-deposited sample before ELC which has no obvious diffraction peaks consistent with the amorphous nature of the film. In contrast, XRD

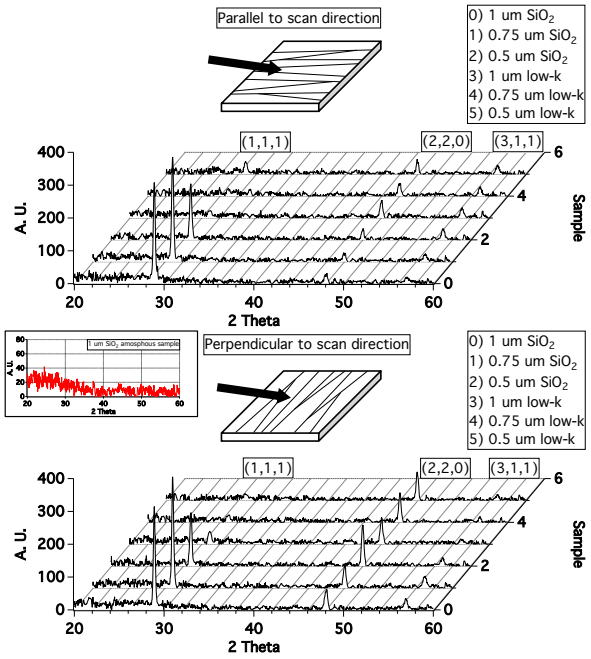

FIG. 5. XRD spectra of the different samples taken both parallel and perpendicular to the grain growth direction. The inset shows the XRD of an amorphous sample for comparison.

spectra from the ELC samples with SiO_2 dielectric show three main peaks corresponding to the (1,1,1), (2,2,0) and (3,1,1) crystal orientations. However, integrated intensity of the (1,1,1) peak is 9.83× (3.64× for perpendicular scan) and 18.60× (7.13× for perpendicular scan) higher compared with that of (2,2,0) and (3,1,1) peaks indicating preferred (1,1,1) texture normal to the sample surface. This observation is consistent with the results from previous studies.[3,10] Although 0.5 μm thick SiO_2 sample exhibits slightly weaker (1,1,1) peak, no significant changes in the crystallinity of the grains is observed for different dielectric thickness. In case of the ELC samples with low-k dielectric, the intensity of the (1,1,1) peak is greatly reduced indicating that there is no (1,1,1) preferential orientation in the surface normal direction. We note however that in-plane preferential orientation might exit for these grains and are not investigated in this studies.

Figure 6 reports the FEM simulation on a structure which closely represents a typical BEOL wafer to study the impact of the ELC process on the buried Cu interconnect. The simulated structure is composed of 100 nm a-Si on top of a SiO_2 dielectric at different thicknesses. Underneath the dielectric layer 20 nm of SiN is present on top of 200 nm of Cu line on 725 μm of Si substrate. The thermal simulation shows that while the a-Si layer rapidly reaches its melting temperature, the Cu line does not reach a temperature above 70 °C, even for the 0.5 μm thick dielectric, which is a favorable condition for monolithic 3D integration on a BEOL structure.

In this work, we demonstrate the excimer laser crys-

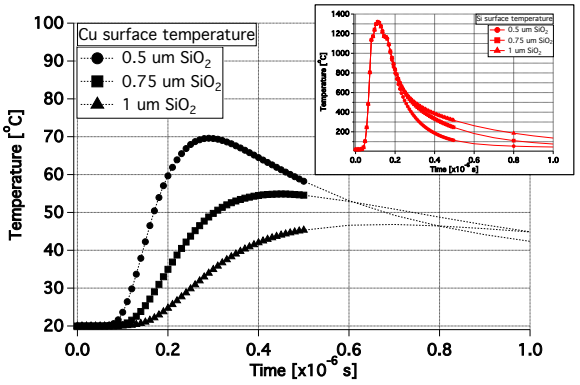

FIG. 6. 1D FEM simulation of the temperature evolution during ELC on the BEOL Cu surface structure in the case of SiO_2 dielectric. The inset shows the temperature reached by the a-Si layer which match the one in Figure 3.

tallization of amorphous silicon on low-k dielectrics for monolithic 3D integration on the BEOL of processed silicon wafers. The crystallization on low-k dielectrics requires about 35% less energy than required for otherwise equivalent SiO_2 dielectrics, because of the difference in thermal conductivity between the two materials. The long grains characteristic of the process reach a width of 500 nm. Raman analysis of the crystallized wafers does not show any major difference in the quality of the polysilicon. The XRD spectra show a preferential (1,1,1) orientation for the silicon on top of SiO_2 dielectrics independent of the scan direction, while it does not show a preferential direction for the polysilicon on low-k materials. We further performed 1D FEM simulation of a typical BEOL structure showing that the temperature reached by the Cu lines during the ELC process is lower than 70°C, which is compatible with BEOL integration. We conclude that low-k materials are preferred over SiO_2 interlevel dielectrics for BEOL 3D integration of active silicon devices, and that the low thermal conductivity of low-k materials yields superior processing characteristics and protection of underlying metal interconnects.

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