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Local Measurements of Flow Boiling Heat Transfer on Hot Spots in 3D Compatible Radial Microchannels

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LOCAL MEASUREMENTS OF FLOW BOILING HEAT TRANSFER ON HOT SPOTS IN 3D COMPATIBLE RADIAL MICROCHANNELS

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ABSTRACT

Hot spots and temperature non-uniformities are critical thermal characteristics of current high power electronics and future three dimensional (3D) integrated circuits (ICs). Experimental investigation to understand flow boiling heat transfer on hot spots is required for any two-phase cooling configuration targeting these applications. This work investigates hot spot cooling utilizing novel radial micro-channels with embedded pin arrays representing through-silicon-via (TSV) interconnects. Inlet orifices were designed to distribute flow in radial channels in a manner that supplies appropriate amounts of coolant to high-power-density cores. Specially designed test vehicles and systems were used to produce non-uniform heat flux profiles with nominally 20 W/cm^2 background heating, 200 W/cm^2 core heating and up to 21 W/mm^2 hot spot (0.2 mm x 0.2 mm) heating to mimic a stackable eight core processor die (20 mm x 20 mm) with two hot spots on each core. The temperatures associated with flow boiling heat transfer at the hot spots were locally measured by resistance temperature detectors (RTDs) integrated between the heat source and sink. At nominal pressure and flow conditions, use of R1234ze in these devices resulted in a maximum hot spot temperature (T_{hs}) of under 63 °C and average T_{hs} of 57 °C at a hot spot power density of 21 W/mm^2. A semi-empirical model was used to calculate the equivalent heat transfer rate around the hot spots which can provide a baseline for future studies on local thermal management of hot spots.

INTRODUCTION

Continuously scaling down the CMOS feature size and increasing the clock frequency of semiconductor devices requires high performance cooling to handle resulting thermal issues, which accelerate device failure, increase power leakage and reduce system efficiency. Furthermore, the spatially non-uniform heating conditions have to be considered for practical implementation of cooling technologies targeting ICs. A traditional approach to mitigate localized high heat flux is the use of thermal spreaders in the packaging of current 2D circuitry. However, it may not be applicable in future 3D ICs since the space between each stacked layer is limited. Use of solid state thermoelectric coolers (TEC) [1, 2] is another approach to locally reduce local temperature rise, but requires fitting such devices into 3D stacks and increases the total heat which needs to be rejected.

Development of a new generation of 3D processor chips [3] indicates the need for between-chip cooling, with single phase coolant flowing between the chips presented as one approach. Using two phase cooling rather than single phase cooling allows the use of the latent heat of vaporization to require much lower coolant mass flow rates.[4] Previous studies [5-7] show that, unlike single phase cooling, heat transfer coefficients (HTC) increase with increasing local heat flux and vapor quality until eventual dry-out at a critical heat flux (CHF) condition.[8] An additional advantage of two phase cooling particular to local hot spots is that the hot spot may have only a weak influence on the global evaporation process. A numerical method developed by R. Revelin et al [9] shows that the hot spot heat flux could exceed global CHFs by 10 times or more, depending on conditions.

A limited number of experimental studies have investigated non-uniform flow boiling heat transfer in parallel microchannel heat sinks. Y. Madhour et al measured HTC as high as 270,000 W/m^2·K for two-phase flow boiling of R134a inside a copper microchannel heat sink [7]. S. N. Ritchey et al found HTC and wall temperatures under non-uniform heating significantly deviate from a uniformly heated case [10]. None of these studies address hot spots in a radial flow boiling configuration. In this study, flow boiling of R1234ze in radial microchannels under non-uniform heating is experimentally investigated utilizing a thermal test vehicle (TTV) which mimics the geometries and power maps of a typical processor. This TTV has radial microchannels with embedded pin arrays which represent TSVs. This work focuses on local measurements of flow boiling heat transfer around hot spots (200 µm x 200 µm) at very high local heat fluxes. No additional local thermal management approaches (e.g. enhanced structures, impingent jets) were used to concentrate cooling effects on hot spots. Since the silicon layer spreads heat between the hot spots and microchannel walls, a semi-empirical model was used to calculate the equivalent HTC on walls which can provide a baseline for future study of the local thermal management concentrating on hot spots.

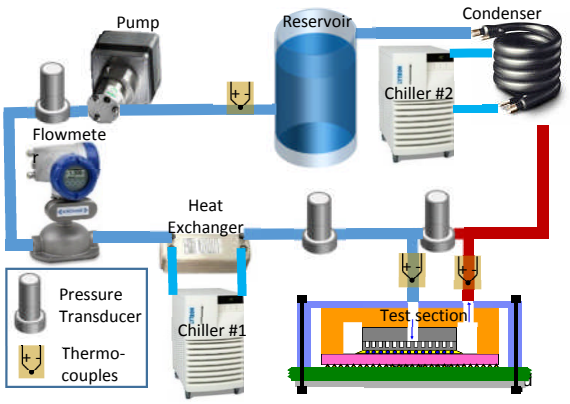

Figure 1. The system diagram of the test setup. Blue and red wires represent flow tubing.

EXPERIMENTAL SETUP

An experimental setup was built to measure local temperature at hot spots in radial microchannels with pin arrays. A schematic of this setup is shown in Fig. 1. This setup is a closed loop flow system, which is comprised of a thermal test vehicle (TTV), a reservoir, a condenser, a magnet driven gear pump (Fluid-o-Tech™ FG200), a pre-heater and a Coriolis mass flowmeter with an accuracy of 0.035% full scale (KROHNE™ OPTIMASS 3000). The temperatures of the condenser and the pre-heater are controlled by two Lytron™ recirculating chillers. Mass flow rate is actively controlled by a PID (proportional-integral-derivative) algorithm. Pressures and temperatures in the loop are monitored by three Omega™ pressure transducers with an accuracy of 0.1% full scale and eight K-type thermocouples (TC). All data is collected by an Agilent™ 34980A DAQ system.

The thermal test vehicle sits on a test board, which provides all electrical and signal connections. To measure the fluid inlet and outlet temperatures, two K-type TCs are attached onto the inlet and outlet tubing, very close to the test vehicle. These tubing mounted TC's show a temperature difference of 0.3°C relative to immersed TC's.

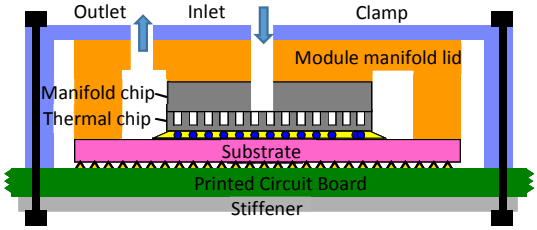

Figure 2. A schematic map of thermal test vehicle clamped onto a printed circuit board (PCB).

THERMAL TEST VEHICLE

The TTV is composed of four different parts: a copper manifold lid, a silicon manifold chip, a silicon thermal chip and a ceramic substrate. As shown in Fig, 2, the module manifold lid, the manifold chip and the thermal chip are bonded by reflow soldering. The thermal chip has a heater array on the back side to simulate a non-uniform thermal profile. Embedded in the heater array are RTDs to measure local temperatures. The front side incorporates radial microchannels with an embedded pin array representing TSVs. A manifold die provides the top surface of the refrigerant channels. Refrigerant is fed into a center hole in the manifold die and exits at the perimeter of the chip pair. This chip pair was mounted onto the ceramic substrate using C4 solder balls. The mounted chip pair was then underfilled using an electrically-insulating adhesive (the yellow area in Fig. 2) to protect the solder balls. The ceramic substrate was clamped into a LGA (land grid array) socket on the PCB (printed circuit board), to make electrical signal and power connections to the external testing apparatus. The TTV cooling structures formed embedded channels which are compatible with 3D chip stacks. In a stack each thermal die above the first would include the central hole, with a single manifold die capping the stack. However, only a one layer thermal chip is demonstrated in the current vehicle as an early stage of study on flow cooling in 3D ICs.

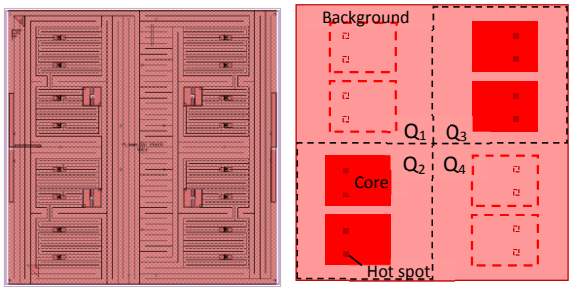

Figure 3. The design of heaters (left) and thermal map (right) on the silicon thermal chip. 4 out of 8 cores and 8 out of 16 hot spots are powered at high heat flux.

THERMAL CHIP

The thermal chip was designed to mimic an eight core processor under a non-uniform thermal profile. The die size is 20.25 mm x 20.25 mm. As shown in Fig. 3, a set of metal thin-film heaters is deposited on the backside of the silicon thermal chip. It has a background heater (area: 246 mm^2), eight core heaters (single core area: 16.5 mm^2) and 16 hot spot heaters (single hot spot area: 0.04 mm^2). They are divided into four symmetric quadrants. Core heaters representing processor cores were originally designed as symmetric features, however only four out of the eight cores on diagonal quadrants Q_2 and Q_3 were powered at the high heat flux of 200 W/cm^2 in this study (red area in Fig. 3). Similarly, eight of the 16 hot spot heaters (those on the corresponding quadrants) were powered up to 20 W/mm^2 (small dark red areas in Fig. 3). The rest of the area was powered

as background heating (pink area in Fig. 3) at the relatively low heat flux of 20 W/cm^2.

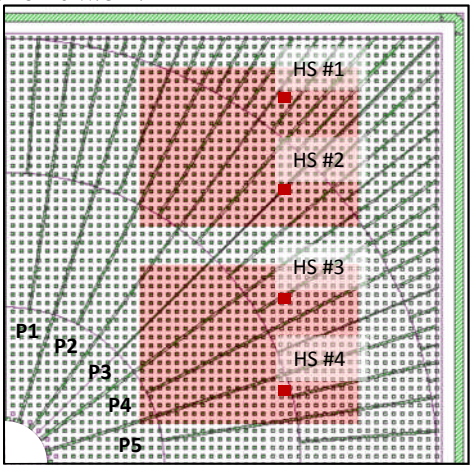

Figure 4. A quadrant (Q3) of a radial microchannel with embedded pin arrays. The core areas and hot spots are overlapped under the microchannels. Five partitions are labeled as P1 to P5. Four hot spot positions are labeled as HS #1 to HS #4.

The radial microchannel is symmetrically designed and fabricated by a DRIE (deep reactive ion etch) process. The height of the pins and the walls in the radial microchannels is 120 µm. The orifice width for flow entering between guiding walls varies from only 80 µm to wide open at 264 µm. The pin diameter is 80 µm and the longitudinal and transverse pitches are both 200 µm.

As shown in Fig. 4, the whole quadrant is evenly divided into five partitions (P1 to P5) starting at the central feed in the lower left corner and each partition bifurcates downstream stepwise, three times. Since the thermal profile is non-uniform, the fluid distribution is passively controlled by the inlet orifice on each partition. The orifices have different widths to distribute the refrigerate flow based on local heat transfer requirements, with the middle orifice being the largest. The inlet orifice is narrowed for other two partitions since less total heat is to be applied in those partitions.

Generally, there are two major advantages for these expanding microchannels. First, this structure passively suppresses reverse flow and stabilizes two-phase flow. Second, the expanding cross-section reduces the vapor flow velocity, mitigating undesirable liquid entrainment which may induce an early dry-out condition in the downstream channel.

DATA ACQUISITION & REDUCTION

Agilent™ N5767A power supplies controlled the electrical current for the background and core heaters with 0.1% accuracy. Background and core heat fluxes were kept at 20 W/cm^2 and 200 W/cm^2, respectively. A HP™ 6624A four channel power supply powered the hot spot heaters on each quadrant. Voltage taps were used in order to accurately monitor voltage on every heater. Local RTD temperatures were measured as a function of hot spot heat flux ranging from 200 to 2100 W/cm^2 (2 - 21 W/mm^2). All data are acquired by an Agilent™ 34980A at a frequency of 1.2 Hz. For every measurement, 100 steady-state samples were taken in about two minutes and the results averaged.

In this study, two cases tested with total mass flow rates at 10 kg/hr and 15 kg/hr. However, due to the asymmetric thermal profile, the flow rate for individual quadrants cannot be directly estimated using the mean value. An alternative approach used experimental pressure drops for symmetric conditions. The pressure drop Δp_c for 200 W/cm^2 symmetric core heating is 130.3 kPa and the pressure drop Δp_b for 20 W/cm^2 symmetric background heating is 100.7 kPa. Based on the Darcy-Weisbach equation, a mass flow rate ratio between $Q_{1,4}$ and $Q_{2,3}$ could be derived as:

$$\frac{\dot{m}_{1,4}}{\dot{m}_{2,3}} \propto \sqrt{\frac{\Delta p_b}{\Delta p_c}} \quad (1)$$

According to the above equation, there is less than 7% variation between asymmetric quadrants. It suggests that an asymmetric thermal profile would not significantly unbalance the flow distribution. For total flow rates of 10 kg/hr and 15 kg/hr, the mass flow rates for tested high power quadrants $Q_{2,3}$ could be estimated as 2.3 kg/hr and 3.5 kg/hr, respectively. It should be noted that there could be partial local solder blockage in the untested quadrants $Q_{1,4}$ due to defects from fabrication processes in the early stage of this study. However, flow distribution is mainly determined by inlet orifices and partial blockage inside radial channels would not likely result in a significant change.

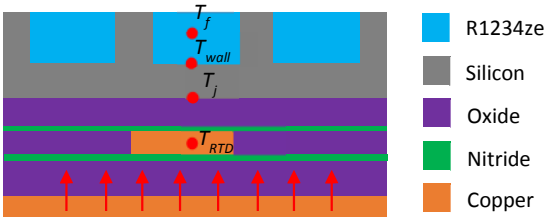

Figure 5. Microstructures between heater and channel.

In this study, the RTD temperature data T_{RTD} do not represent the actual junction temperatures, T_j, on actual processors since there is an insulating layer of 466 nm thick oxide and another 51 nm thick nitride layer, which do not exist in a real-world processor. This additional thermal resistance could be substantial at very high heat flux conditions. Therefore, it is subtracted from the experimental RTD results to understand the actual thermal resistance between the equivalent T_j and the fluid temperature T_f of refrigerant R1234ze during flow boiling. Using a 1D heat transfer model, the equivalent T_j is derived as,

$$T_j = T_{RTD} - q\left(\frac{t_n}{k_n} + \frac{t_o}{k_o}\right) \quad (2)$$

In this equation, k_n and k_o are the thermal conductivities of silicon nitride and oxide thin-films [11] and t_n and t_o are the corresponding thicknesses, respectively. The local heat flux on hot spots is q.

Local T_f is calculated based on the existing relationship between saturated temperature and pressure for R1234ze. The local pressure in radial microchannels is derived by assuming a linear relationship between pressure drop and the change of vapor quality. A semi-empirical equation for local pressure, p, can be derived as,

$$p = p_o + (\Delta p - \Delta p_{orifice})\left(1 - \frac{\chi}{\chi_o}\right) \quad (3)$$

p_o is the outlet pressure, Δp is the total pressure drop, $\Delta p_{orifice}$ is pressure drop across inlet orifices and pre-calibrated in adiabatic tests. χ is local vapor quality and χ_o is vapor quality at the outlet. The vapor quality could be derived by the conservation of energy.

Therefore, the thermal resistance of the radial microchannel around hot spots is calculated as,

$$R = \frac{T_j - T_f}{q} \quad (4)$$

And the overall heat transfer coefficient of this radial microchannel, h, is $1/R$.

RESULTS AND DISCUSSIONS

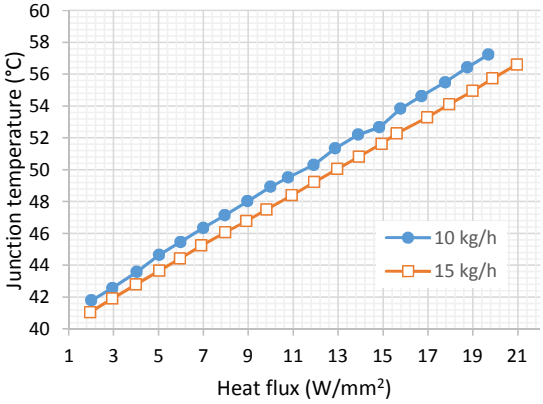

Figure 6. Equivalent average junction temperature as a function of hot spot heat flux.

As shown in Fig. 6, average T_j is plotted as a function of hot spot heat flux at two different flow rates, 10 kg/hr and 15 kg/hr. It shows that junction temperature increases linearly with increasing hot spot heat flux. Moreover, Figure 6 shows that the higher flow rate likely enhanced local convective heat transfer and reduce average hot spot temperatures. Average T_j are lower for flow rate of 15 kg/hr than flow rate of 10 kg/hr.

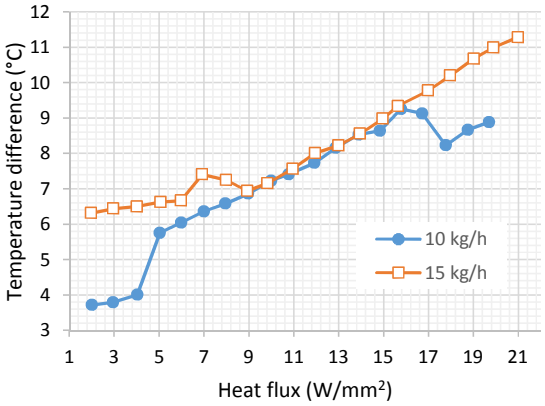

Figure 7. Maximum-to-minimum temperature difference among eight hot spots as a function of hot spot heat flux.

Temperature non-uniformity is also characterized in this study. The maximum-to-minimum temperature difference among the eight hot spots is plotted in Fig. 7, which shows up to 9.3 °C and 11.3 °C differences for 10 kg/hr and 15 kg/hr, respectively. The temperature difference likely results from the flow distribution and non-uniform heat flux design of the TTV as shown in Fig. 4. Generally, an upward trend of non-uniformity is noticeable in this data set with increasing heat flux.

It should be noted that the total heat associated with the hot spots is relatively negligible compared to the total heat input to the "cores" and "background". Variation of hot spot heat flux should not influence overall vapor quality and flow patterns inside radial microchannels. The overall flow condition is passively controlled by inlet orifices. Under moderate hot spot heat flux, the convective heat transfer and nucleate boiling are effective in cooling hot spots and suppressing temperature rise on all partitions. However, at very high hot spot heat flux, the local heat transfer shall highly depend on liquid supply in each partition. The highest hot spot temperature is usually found on HS#4 (Fig. 4), which is in partition P5 with the narrowest orifice compared to the middle partitions (P2 to P4) with wide open orifices.

Moreover, increasing total liquid flow would not mitigate this non-uniformity. At the flow rate of 15 kg/hr, the temperature difference is generally increased compared to 10 kg/hr. In the case of 15 kg/hr, most of the liquid flows into the three middle partitions, which lowers average temperature. However, it increases the difference between flow rates of middle partition (P2 - P4) and P1. As a result, the higher flow rate even exacerbates non-uniformity as shown in Fig. 7.

The hot spot thermal resistance of this radial microchannel is plotted as a function of hot spot heat flux (Fig. 8). It indicates the thermal resistance gradually decreases with hot spot heat flux. It could be explained by the fact that silicon has good thermal conductivity. At the beginning, hot spots experience the same heat flux as the surrounding core heating. Thus, there is no substantial temperature gradient. With increasing hot spot heat

flux, the temperature gradient becomes significant and the silicon substrate and pins likely work as a thermal spreader around the hot spots, which reduces the effective heat flux on the wall surfaces (Fig. 5). The overall thermal resistance between hot spots and refrigerant is then reduced by this thermal spreading effect.

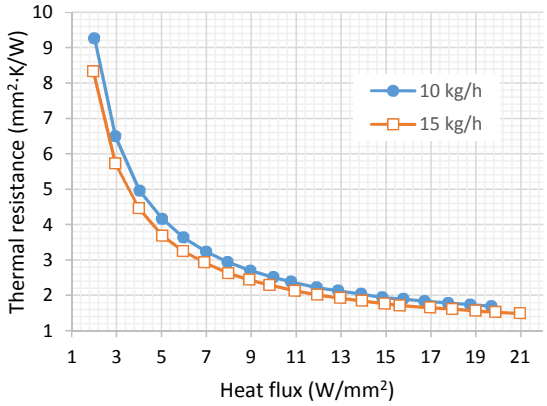

Figure 8. Thermal resistance of the radial microchannel as a function of hot spot heat flux.

The overall local heat transfer coefficients between hot spots and refrigerant are shown in Fig. 9. This results shows the ability of this type of pin-finned radial microchannels to manage hot spots. This set of data could be a baseline for local thermal managements on hot spots. As shown in Fig. 9, increasing the flow rate by 50% only leads to a small heat transfer enhancement of about 8%. More significant heat transfer increases could be achieved by concentrating cooling effects. For example, integration of nanoporous structures [12, 13] may further cool down hot spots by enhanced nucleate boiling and thin-film evaporation.

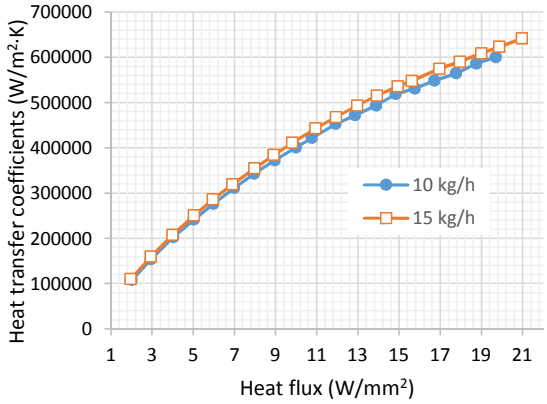

Figure 9. Overall heat transfer coefficients as functions of hot spot heat fluxes.

CONCLUSION

This study experimentally investigated flow boiling heat transfer on hot spots and tested its non-uniformity in a radial microchannel with pin arrays under non-uniform heating. Core and background heating were kept constant but hot spot heat flux was varied. Two different flow rates were tested and showed similar trends in this study.

In this study, we demonstrated that embedded radial microchannels could manage a heat flux of 21 W/mm^2 with a hot spot temperature below 63 °C for 200 µm x 200 µm hot spots at different locations on a thermal die. Up to 11.3 °C temperature difference was observed among these hot spots at the highest heat flux condition. The temperature difference increases with hot spot heat flux due to an unbalanced liquid supply. To mitigate this non-uniformity, we could redesign the inlet orifice to balance the flow distribution in each partition of the radial microchannels at the target flow rate.

The local thermal resistance is gradually reduced with locally increasing hot spot heat flux, likely as a result of thermal spreading. At the highest heat flux condition, overall local heat transfer coefficient including this spreading is as high as 636,000 W/m^2·K.

This study shows that it is not effective to simply increase the flow rate for suppressing non-uniformity. Local thermal management is necessary to concentrate cooling effects and achieve more effective heat transfer and better temperature uniformity on hot spots. Experimental data in this study could be a baseline for future thermal managements on hot spots.

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