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The First Thin-Film Electronic Package

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Abstract

The magnetic thin-film head, announced by IBM in 1979, marked the transformation of electrochemical technology from a shop art to a precision manufacturing process with far wider applications than the thin film head. An important application of electroplating was in the fabrication of the multichip module that provided the packaging for chips in advanced computers. These modules included copper strip lines for data transmission between chips. To minimize pulse distortion, these lines had to have precisely controlled propagation characteristics, and plating through a lithographic mask was the most effective way to insure the tight control on the geometry of the lines necessary to meet this requirement. This paper highlights the evolution of packaging for computers and tells how the scientists and engineers from the IBM T.J. Watson Research Center who had created the thin film head, worked with the development and manufacturing groups at IBM's East Fishkill plant to bring electrochemistry into the manufacture of advanced packaging modules.

Introduction

As late as the end of the 1970's, electroplating was regarded as a mystical shop art that had no place in microelectronic fabrication. In 1979 IBM introduced the magnetic thin film head that was made possible by a newly invented process based on electroplating – an achievement that brought a quantum leap to data storage technology and cast electroplating in a new light. The story of how the thin film head went from a laboratory concept to a manufactured product illustrates many of the principles that govern the path from invention to product and has been described by the authors in a forthcoming publication (1). Today, electroplating is used in producing the metal structures in MEMS devices and in a host of other applications ranging in scale from the patterning of 10

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nanometer and smaller copper BEOL wiring on silicon chips to the deposition of materials for synthesis into photovoltaic layers on 60 cm by 120 cm solar panels. Figure 1 is a graphic representation of the many offshoots that stemmed from the thin-film head and from the science that supported its creation.

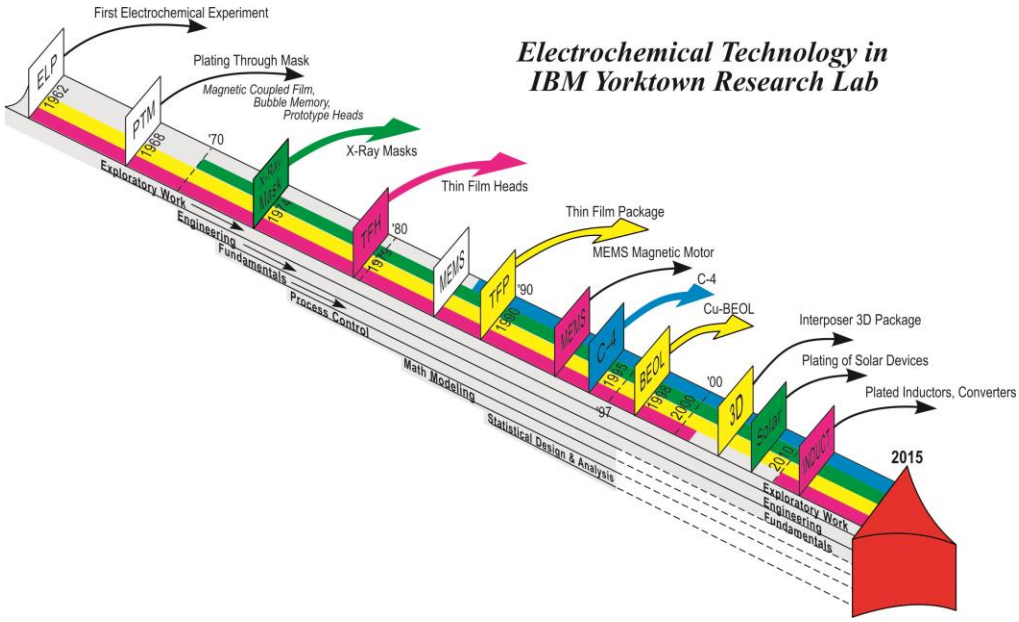

Figure 1. This time-line shows the increasing use of electrochemical technology in precision micro-electronic manufacturing at IBM. The flags on the top surface with broad arrows indicate products that have gone into production using electrochemical technology. Other flags represent exploratory devices made as the thin film head was being invented (left end of the time-line) and recent development work on new applications (right end). The bars on the underside of the arrow show the parallel science and engineering programs that supported the manufacturing lines and continue to advance the technology.

An important application of electroplating technology is in the fabrication of the multichip module. In advanced computers, these modules are multilayer ceramic structures that, among other functions, provide the power connections to the circuit chips and copper strip lines for data transmission between chips. In the first electroplated package, the strip lines consisted of copper conductors with a rectangular cross-section that might be 6 μm high and 10 to 20 μm wide embedded in a polyimide dielectric between two ground planes. To minimize pules distortion, the strip lines must have precisely controlled propagation characteristics. Plating through a lithographic mask proved to be the most effective way of achieving the tight control on the geometry of the lines necessary to meet this requirement.

This paper describes the path of electrochemistry into the manufacturing process for the thin film package. The first section gives a brief overview of computer packaging to put the thin film package in proper context in the evolution of packaging technology.

The specific references in that section and the volume, *Principles of Electronic Packaging* edited by Seraphim *et al* (2), will provide the reader with more extensive details on the evolution of packaging technology. The section that follows describes the fabrication process using electroplating technology that was accepted as the most effective way to manufacture the thin film package. The paper concludes with remarks on the importance of close interactions among the research, development and manufacturing groups in putting electroplating technology on the production line.

A Brief Overview of Packaging

The term "Packaging" as it is used today in reference to computers deals with how all the components necessary to create a functional computer are put together. Thus, packaging encompasses the connections that bring power to the chips, the connections among the active and passive elements on the chip, and the high speed transmission lines for signals between the chips. Packaging also provides physical mounting and protection of the components, thermal management (cooling) for these components, and fan-out from the dense terminals on the chip to the more widely spaced pin connections on the ceramic modules and circuit boards that link the chips to each other and to the outside world.

The underlying approach to manufacturing electronic equipment had remained unchanged from the invention of the vacuum tube in the early part of the twentieth century through the 1950s. Vacuum tubes were the active elements for electronic circuits. The tubes were manually wired up with the individual, passive components to produce the combination of functional circuits required by the product. The home radios that found their way into family living rooms in the 1930s, the radar units that played a key role in the outcome of World War II in the 1940s, and the advanced electronic computers of the 1950s that could perform calculations in microseconds all used vacuum tubes and all were produced by similar, manual fabrication processes. The invention of the transistor in 1947, along with the introduction of circuit boards, brought some changes in

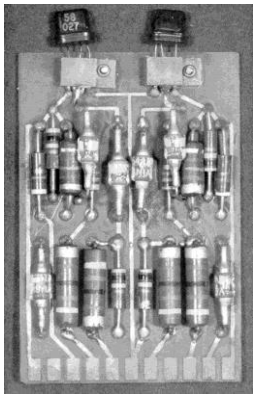

Figure 2. Mounting discrete components on a printed circuit board allowed for some automation and for a reduction in the amount of hand wiring in the manufacture of electronic systems.

the approach to fabrication, particularly in computers. With computers like the ENIAC containing over 17,000 tubes, each tube a rather large component with a heated cathode, the prospect of replacing the tubes with transistors was very attractive, and engineers in the 1950s spent much of their time developing transistor circuits for computers. One such circuit is shown in Figure 2. The components were mounted on a metallized circuit board where the metallization has been photo-lithographically patterned to make the required

interconnections among the components. The circuit was designed to use the two transistors that were plugged in at the upper edge of the circuit board as the active elements. Although the circuit was built with discrete components, the use of the circuit board did allow for some automation and for a reduction in the amount of hand wiring

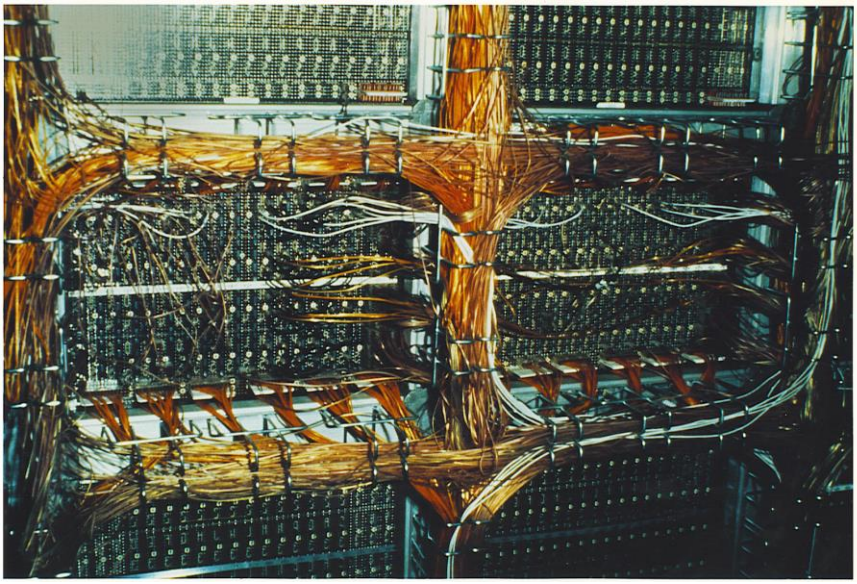

Figure 3. The circuit boards of Figure 2 were plugged into larger boards with extensive hand wiring behind the boards to provide interconnections. Advances in packaging moved these connections to the back-end-of-the-line (BEOL) wiring on the chip or into the multi-layer ceramic module on which the chips were mounted.

needed to build the individual circuits. Since a computer required many such circuits to do its job, arrays of boards such as those in Figure 2 were plugged into larger boards that, in combination with extensive hand-wiring behind the boards, made the necessary interconnections. (Figure 3.) However, it was obvious that this production process was not the way to build computers as the number of transistors necessary to meet higher and higher performance demands increased.

Electronics engineers had many proposals to achieve at least some semblance of mass production without labor intensive manual operations. One approach to this objective, SLT (Solid Logic Technology), was introduced by IBM in 1964 in its System/ 360 series of machines and is illustrated in Figure 4. SLT was a hybrid approach in which specially designed circuit chips were fabricated on one-half inch square ceramic chips (3). (Right side of Figure 4.) Wiring was done with patterned metallization, the resistors were produced by silk screening a resistive material and precisely trimming it to the proper value, and transistors and diodes were added as discrete elements using flip-chip technology. The chips were encapsulated in a metal cover and mounted on printed circuit boards that were in turn mounted on the back panel of the computer. SLT was a major advance in computer packaging and in the manufacture of computers. However, neither SLT nor any of the other hybrid packaging schemes that other manufacturers were pursuing, could keep up with the ever increasing need for more transistor circuits in the computer.

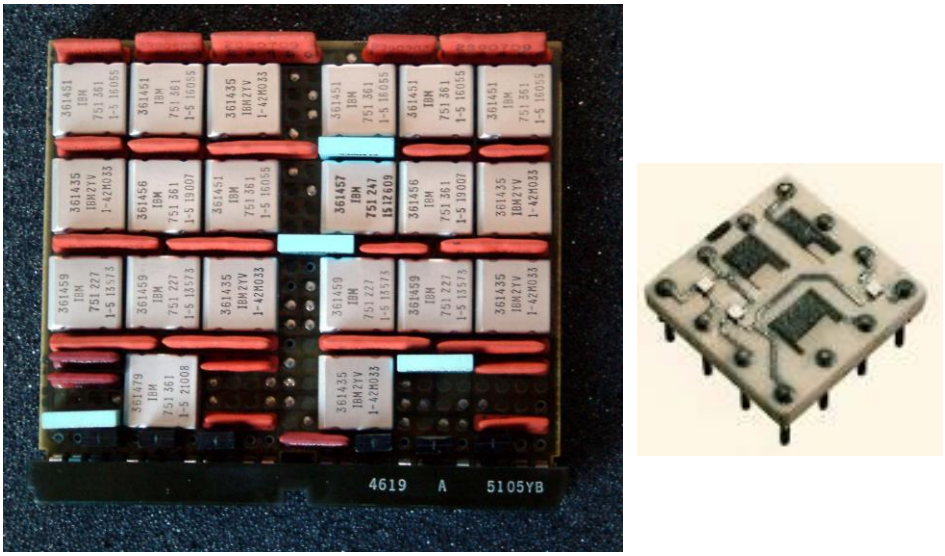

Figure 4. Circuit board with an array of SLT (Solid Logic Technology) chips. IBM's SLT chip was a hybrid approach in which resistors and wiring were formed on ½ inch square ceramic chips shown at right. Discrete transistors and diodes were attached, the units w encapsulated with a metal cap, and the completed SLT chips were mounted on the circuit boards.

In 1959 Jack Kilby at Texas Instrument and Robert Noyce at Fairchild Semiconductor independently filed their respective patents for an integrated circuit (4,5). These patents described circuits in which the active and passive components were both formed on the surface of a suitably doped silicon wafer and were interconnected by

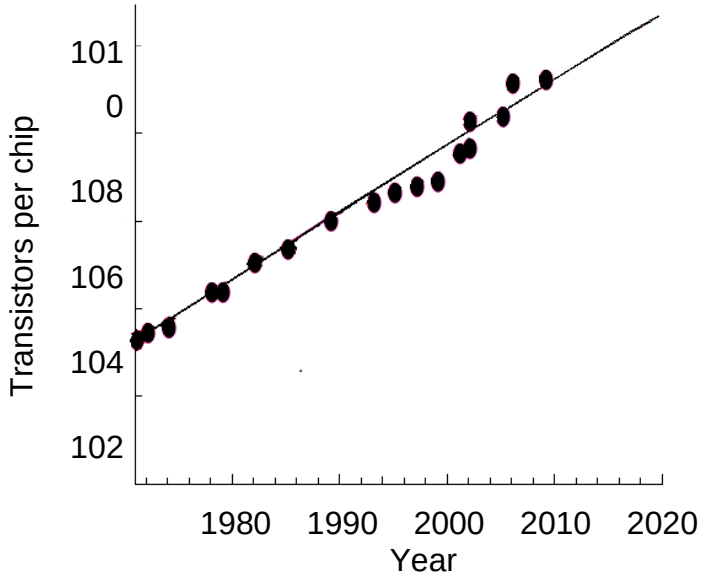

Figure 5. The number of transistors that can be fabricated on a chip has doubled roughly every two years.

patterned metallization to perform the required functions. The integrated circuit made it possible not only to efficiently mass produce electronic components that were already wired together as functional circuits; it enabled much smaller components that could be packed more closely than was possible with SLT and other hybrid approaches – an important consideration when the speed of computers was increasing to the point where the time for a signal to travel within the computer was becoming a limiting factor in performance. A major part of semiconductor activity in the next decade was aimed at extending the integrated circuit from a functional circuit with a few transistors into a technology that could mass produce arrays of interconnected circuits on a single wafer. The success of this activity can be seen in Figure 5. Many readers will recognize this plot as a representation of Moore's Law, named for Gordon Moore, who was among the first to recognize that the number of transistors on a chip approximately doubled every two years. By 1970, chips with 2000 transistors per chip were in production; by 1990 this number reached a million transistors per chip; today, a chip contains about a billion transistors. As the degree of integration progressed, the technology took on names like LSI (Large Scale Integration) and VLSI (Very Large Scale Integration). LSI and its successors, by whatever other names, remains the basic technology for the mass production of circuit chips.

The advances that increased the number of circuits on a chip drove the development of new packaging structures to make full use of the performance capabilities these chips offered. By the late 1970s chips were mounted on 2" x 2" square ceramic chip

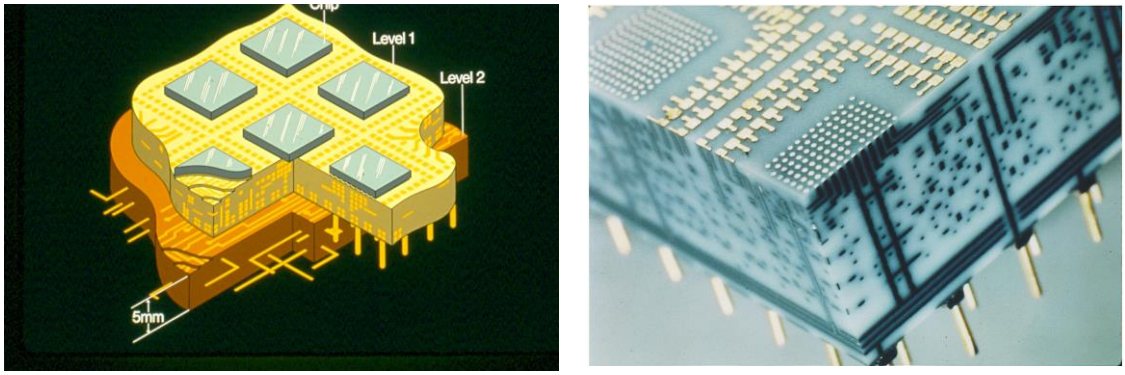

Figure 6. *(Left)* Artist's rendering showing chips mounted on a Multi-Chip Module (MCM) from the late 1970s.

(Right) Photo of an MCM after firing. Square arrays of pads for C-4 attachment of the chips, and rows of pads for probe testing or engineering changes are visible on the top surface. Pins brazed to pads on the bottom surface plug the MCM into the printed circuit board.

carriers, also called Multi-Chip Modules (abbreviated as MCMs) in groups of nine per module using C-4 solder connections as shown in Figure 6 (6,7). Each MCM was made by stacking 49 layers of alumina, some of which were screened with molybdenum paste to form wiring patterns. Holes punched in the alumina and filled with Mo paste interconnected the conductor layers and, when fired, formed a ceramic block with the wiring that interconnected the chips. Much of the back panel wiring in Figure 3 was now part of the chip or of the module on which the chip was mounted.

Each MCM module was plugged into a circuit board that had also evolved into a multi-layer structure fabricated with new manufacturing technologies (8). Figure 7 shows an artist's rendering of a state of the art high performance circuit board from 1981. The

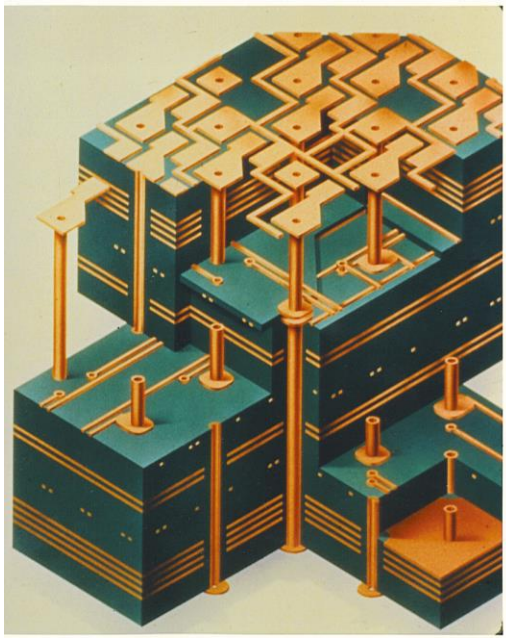

Figure 7. Artist's rendering showing through-vias and other copper conductors that might be found on a high performance printed circuit board from 1981.

board was a composite of 20 layers with overall dimensions of 600 x 700 mm. The board included wiring for power distribution as well as strip transmission lines that brought data and instructions to the chips. The requirements of a low resistance and a specified characteristic impedance of the line called for copper conductors with a well-defined rectangular cross-section that was 1.95 mils thick and 3.2 mils wide. (Packaging literature of that period often used a combination of metric and English units, depending on the parameter being measured. Thus, conductor dimensions might be express in mils; 1 mil = 0.001 inch, or approximately 25.4 microns.) The copper was electrolessly deposited by a process that was specifically developed to provide low resistivity copper and compatibility with the resist used for the through-mask plating pattern.

The Thin-Film Package

Figure 8 shows a cross-section of the MCM highlighting the electrical functions of the module. What is critical for the present discussion are the electrical connections between the chip and the module. Each chip was joined to the MCM by an array of 0.125 mm diameter C-4 connections on 0.25 mm centers. As the number of transistors increased in accord with Figure 5, the number of connections between chip and MCM also increased, thus requiring a denser array of C-4 connections. Making a denser array of C-4 pads on the chip was well within the capability of the chip fabricators; however, the screening process used in MCM production was near the limit of its ability to match the increased density on the MCM. A further evolution in packaging manufacturing technology was necessary.

The proposed solution was to add the 14 level thin film structure shown in Figure 9 to the multi-chip module. This structure would need to have metallurgy on its top surface

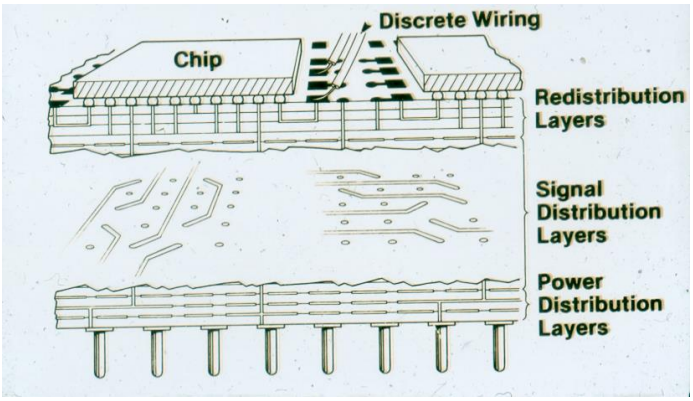

Figure 8. Schematic drawing of a Multi-Chip Module high-lighting the electrical functions of the various levels of the module.

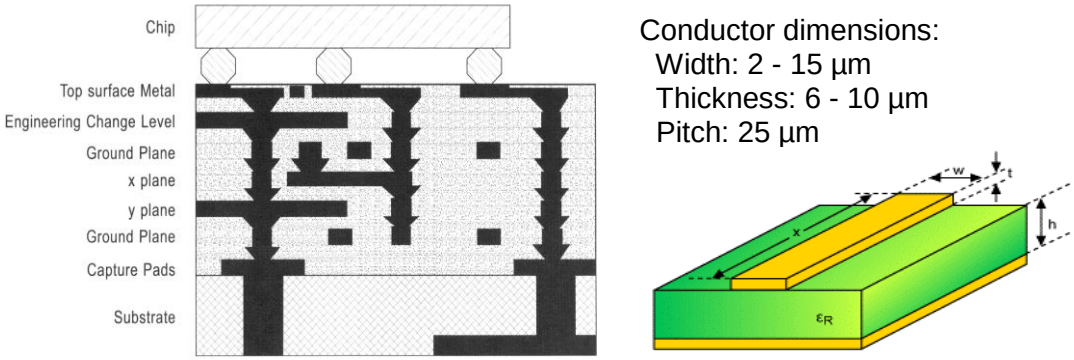

Figure 9. Schematic representation of 14 levels of thin film wiring between the chip and the MCM. Dimensions of the strip line conductors within these levels are shown at right.

that matched the density of C-4 pads for the next generation of circuit chips and it would need to provide appropriate transmission lines to carry data pulses to and from the chips. Dimensional requirements for the internal wiring in structures that would meet these requirements are shown on the right side of the Figure 9. Lift-off was chosen as the process to form the patterned wiring.

Fabrication Process Options

Since the choice of the right process is one of the most crucial steps in manufacturing a product, it is instructive to take a closer look at the options for producing the thin film package. Figure 10 summarizes the characteristics of the commonly used processes in fabricating thin film structures for electronics (9). The choice is dictated by the material being patterned and the critical dimensions, especially thickness, of the structure being fabricated.

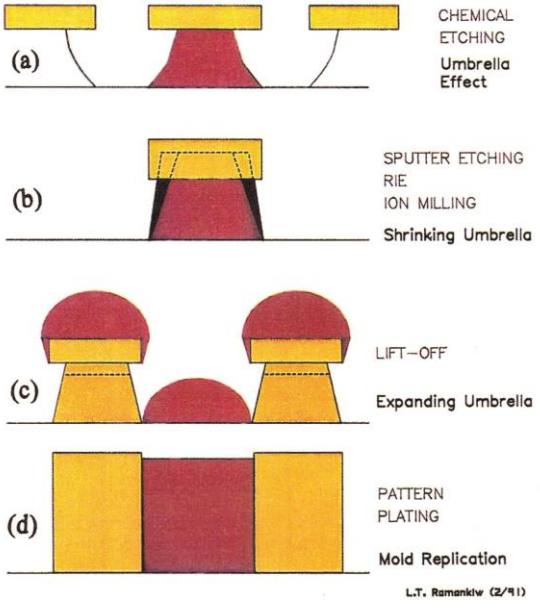

Figure 10. Distortions introduced by patterning processes commonly used in thin film electronics manufacturing.

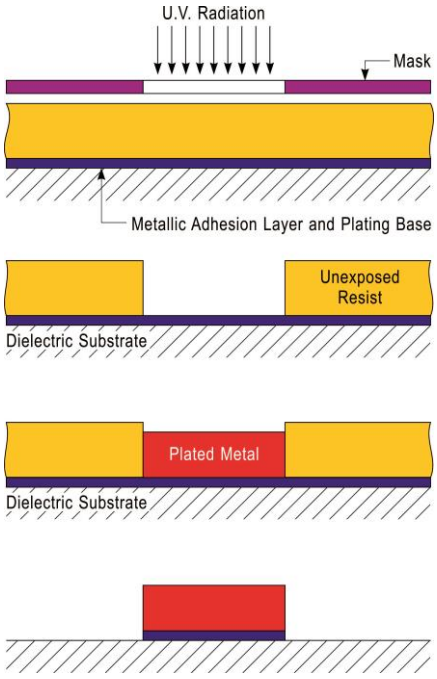

Figure 11. The through-mask plating process.

Chemical etching has been the preferred process for patterning because it is relatively easy to implement and often has the lowest cost of implementation. However, lateral etching, which becomes more severe as the thickness increases, limits chemical etching to patterns with relatively large lateral dimensions in relatively thin films. Other subtractive processes such as sputter etching, reactive ion etching and ion milling may have advantages in some applications. However, the tooling is generally more expensive than for chemical etching equipment, and faithful reproduction of the resist pattern is limited by erosion of the mask during the etching process.

Lift-off is an additive process in which the part is covered by a resist layer with openings for the desired wiring pattern. Special processing is used to produce a slight overhang into the pattern openings at the top of the resist layer. The adhesion layer and conductor material are then evaporated over the entire surface, and the resist is dissolved in a solvent to release and float away all the unwanted material that was deposited on top of the resist. The slight overhang in the initial resist pattern insures a break in the deposit that allows the solvent to reach the underlying resist. The limitation on the lift-off process stems from the deposition of material on top of the mask. This deposit tends to extend the mask over the pattern openings, thus narrowing the opening and reducing the line width as deposition proceeds.

The only process that can faithfully reproduce a lithographic mask down to atomic dimensions is through-mask plating, which is illustrated in Figure 11. The process starts with the evaporation or sputter deposition of a thin metallic adhesion layer and a conductive plating base (total thickness about 2000 Å). A layer of photoresist whose thickness is somewhat greater than the thickness of the pattern being built is applied and

processed to leave openings for the desired pattern. The part is now plated to the desired thickness, the photoresist is removed, and the seed and adhesion layers that were protected by the resist are etched away. The remaining pattern is a precise replica of the openings in the original resist pattern.

Lift-off was not an unreasonable process choice for the thin-film package. The engineers who chose lift-off had little experience with electroplating, but they had considerable expertise with evaporation processes, an essential part of lift-off technology. Since wiring structures could be built by lift-off, it was good engineering practice to start their packaging program with a technology that they understood. The authors of this paper and several of their colleagues at the Watson Research Center, who had developed through-mask plating into a manufacturing technology for the thin film head, however, saw plating as the most appropriate way to meet the requirements of the thin film package. The Research group established a close relationship with the development and manufacturing engineers who were pursuing lift-off technology and proceeded to demonstrate the use of through-mask plating to build the identical package. As will be discussed in the concluding section, through mask plating was the process that went into the production line.

It should also be noted that as development and manufacturing engineers gained expertise in plating technology, the preferred processes for creating patterned conductors was narrowed down to subtractive etch and pattern electroplating. The choice depended on the dimensions of the structure, and engineers in IBM's East Fishkill facility created the chart in Figure 12 as a guide for choosing between a chemical etching process and through-mask plating. (10)

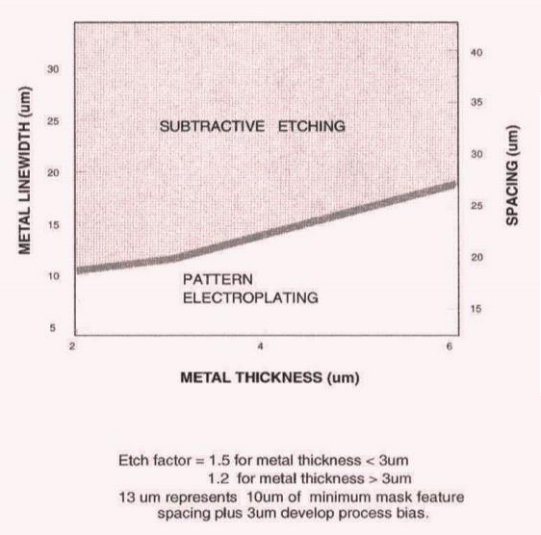

Figure 12. The optimum choice between chemical etching and through-mask plating as the manufacturing process depends on the pattern dimensions. This chart helps IBM engineers to make the choice. (10)

Through-Mask Plating for the Thin Film Package

Any application of through-mask plating has to be customized for the specific structure being built. For the multilevel thin film package, the process was designed to fabricate the wiring and vias for each level in a series of steps illustrated in Figures 13. The wiring pattern (A) was formed using the initial steps of the through-mask plating process in Figure 11, but the resist and seed layer were not removed. A second layer of

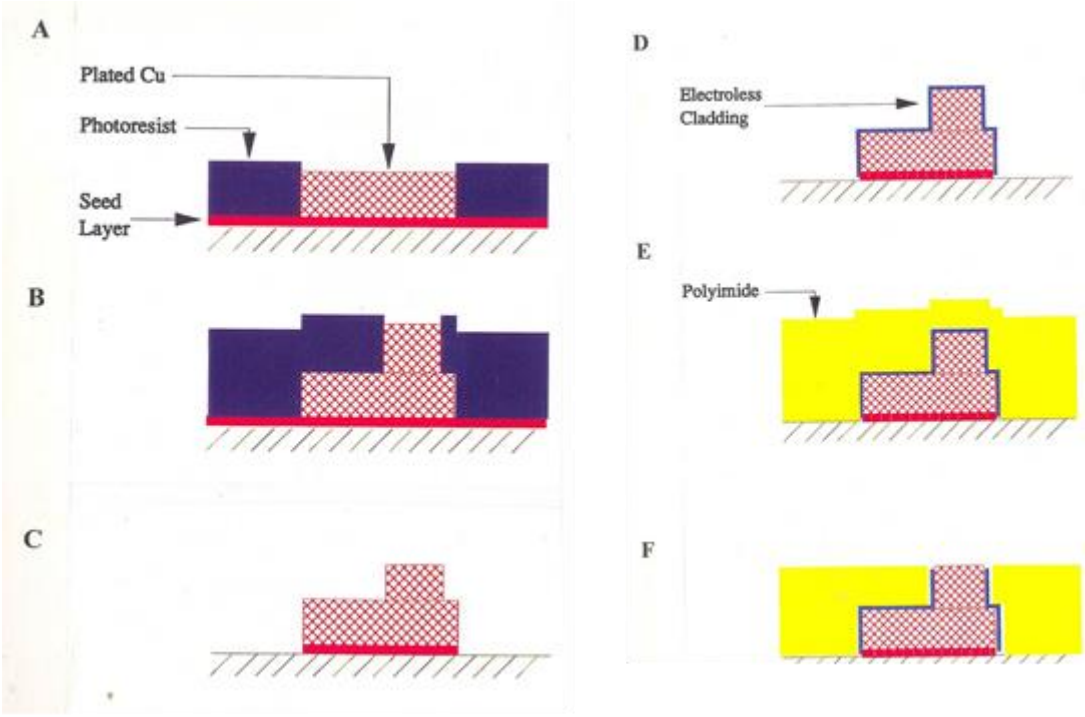

Figure 13. Process steps used to fabricate an electroplated copper conductor level and an electroplated via level in the thin film package. This series of steps was repeated to build subsequent levels.

resist was applied and patterned with openings for the vias, which were then plated (B). The resist, adhesion and seed layers were then removed, leaving the wiring and via structure in Figure 13C. The next step was to form the polyimide dielectric layer. However, as the part goes through the various thermal processing cycles, the polyimide absorbs and releases moisture that could react with the Cu at the Cu-polyimide interface. It was therefore necessary to introduce a coating of cobalt-phosphorus (CoP) to protect the copper. An electroless deposition process was used to form the CoP, after which, polymide was applied and cured in sufficient thickness to just cover the vias (E). Fabrication was completed with a kiss polish step to open the vias and create the planar surface on which to repeat this process for the next level. (11, 12)

Figure 14 shows scanning electron microscope photos of the conductive elements in the completed package test vehicle structure taken on a sample where the polyimide dielectric was removed by ashing in an oxygen plasma. The test vehicles included chains of 3000 via links with diameters of 15, 18.4, and 23 µm. Once the process was established, the average resistance of a via-link within the chain was consistently between 6.5 and 7.5 milliohms, depending on the diameter. For a given diameter, via-link resistance measurements were within 0.5 milliohms of each other from part to part.

The test vehicle also included patterns to measure the resistivity of the copper, the isolation resistance between conductors, and the pulse propagation characteristics of the transmission lines that were built into the structure. The measured resistivity was consistently between 1.6 and 1.7 µohm-cm, which is essentially that of bulk copper. Isolation resistance was measured between parallel conductors that had an effective length of 6 cm and a separation of 29, 33, or 36 µm. All the measurements ranged from a

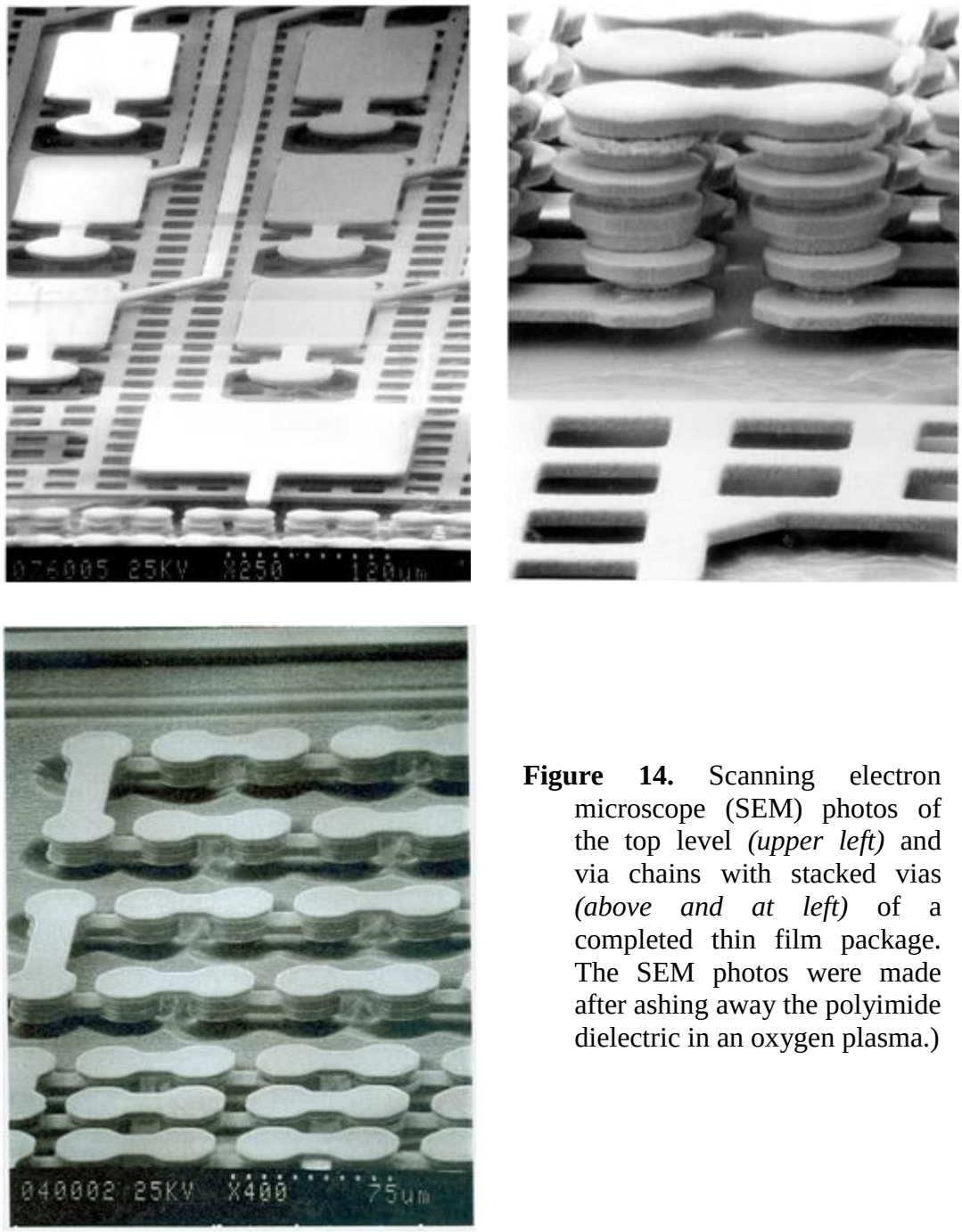

Figure 14. Scanning electron microscope (SEM) photos of the top level *(upper left)* and via chains with stacked vias *(above and at left)* of a completed thin film package. The SEM photos were made after ashing away the polyimide dielectric in an oxygen plasma.)

few gigaohms to tens of gigaohms. Since deficiencies in virtually any step of the fabrication process can degrade the isolation between conductors, the high values of isolation resistance are an indication that the individual process steps were sufficiently well understood and controlled to avoid problems. The measured characteristic impedance and propagation delay in 3.12 and 5.29 cm long strip line structures showed good agreement with the design values. The increase in rise time for pulses with an initial rise time of 35 picosecond transmitted through these lines was well within the requirements of the intended application.

It should also be noted that probing the metal structure with tweezers or other rough handling after the polyimide was removed to take the SEM photos did not cause any noticeable deflection or damage to the structure. The structure was completely self-supporting, indicating very good metal-to-metal bonds between individual layers.

Through-Mask Plating Enters the Package Production Line

Why did the manufacturing engineers, who were experts in physical vapor deposition, choose electrochemical technology over lift-off to manufacture the thin film package?

Certainly, the merits of electrochemical technology and the structure it produced were important considerations.

- Electroplated copper had a lower resistivity than the evaporated copper that was deposited in the lift-off process. The plated copper also had a higher ductility and a lower tensile stress, which enhanced the reliability of the product. (13)
- Electroplating provided faithful reproduction of the resist pattern, allowing designs with closer packing of conductors. Faithful reproduction also provided maximum filling of the lines and vias to give maximum cross-sectional area and thus minimum resistance for a given pattern.
- The plating process using the paddle cell was reproducible from tool to tool and was readily scalable to larger substrates. A unique feature of the paddle cell is the fact that agitation is produced locally at the cathode, where it is needed. By designing an appropriately sized paddle and sweep mechanism to move the paddle parallel to the substrate, uniform deposition has been obtained in applications ranging from very small MEMS and NEMS structure to large 300 mm x 600 mm solar panels. (1) The lift-off process, on the other hand, requires the evaporated material to arrive at the substrate within five degrees of normal incidence. As the substrate size increases, source-to-substrate distance in the evaporator must correspondingly increase, leading to a more expensive installation, wasted materials that deposit on the walls of the evaporation chamber, and higher operation and maintenance costs.
- A thin film package line built around the electroplating process offered greater through-put at lower installation cost than a line that used lift-off.

Also contributing to the acceptance of electroplating for production of the thin film package was the success of the magnetic thin film head, the mass production of which became possible with the invention of a process that was based on electroplating. Electroplating, which had been regarded as shop art that was not applicable to the precision production of micro-electronic devices, was cast in a new light by the success of the head.

What may have been the most critical element in bringing electroplating into production line for the thin film package, however, was the interaction of research, development and manufacturing personnel who worked closely together from the outset to arrive at the best possible manufacturing process. In particular, the research group understood the difference between a “laboratory-capable” tool and one that was

"manufacturing capable." They knew that to insure a viable manufacturing process, they could not simply hand-off the laboratory process to the manufacturing group; they would have to actively participate in putting the process on the production line.

The list of inventors on the patent for the vertical paddle cell, the key production tool for the thin film package, (Figure 15) is an example of the close interaction of research, development and manufacturing engineers in implementing the manufacturing process. The tool was designed for automated handling of the modules, and it was done in a way that did not compromise the inherent advantages of the paddle cell that were essential for the reproducible production of thin film structures that met performance specifications. The fact that the plating process for the thin film package was developed with a continual eye on how the product would be manufactured was an important factor in the ultimate adoption of electroplating as the production process. It was also helpful that one of the authors (L.T.R.) had previously worked with some of the manufacturing engineers to develop plating processes for multi-level ceramic package production, thus giving the manufacturing group confidence that the proposals for using through-mask plating were backed by people in the research lab who had an appreciation of manufacturing concerns.

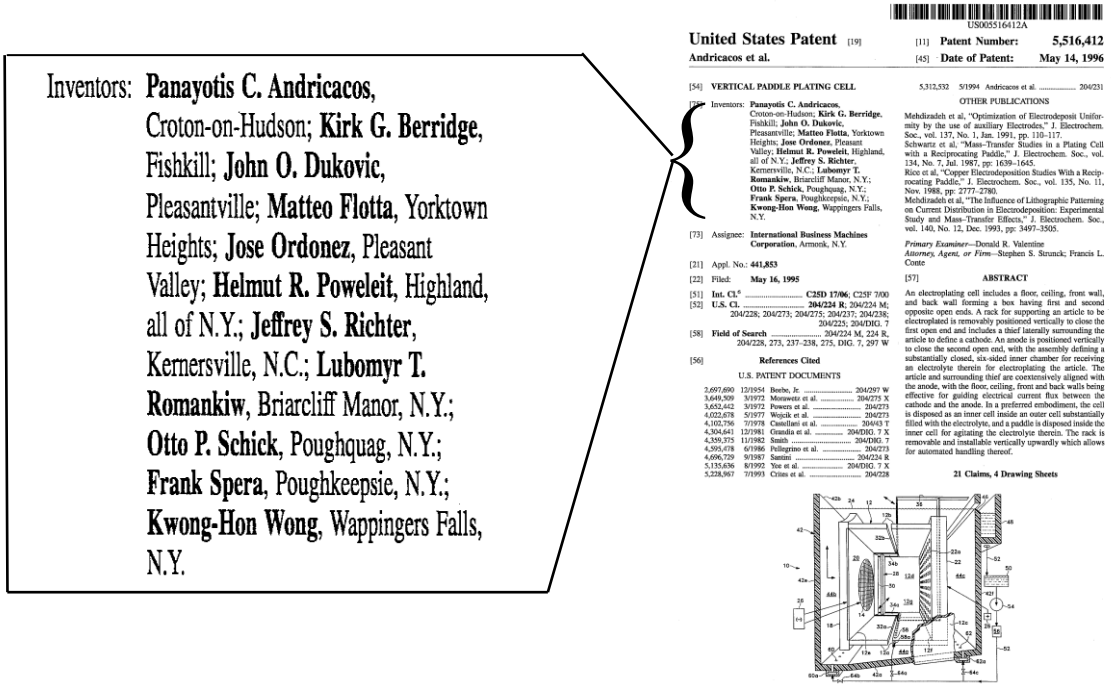

Figure 15. First page of U.S. Patent 5,516,412 for the vertical paddle cell that was designed for automated operation on the thin film package production line. The highlighted list of inventors from the research, development and manufacturing areas, each of whom contributed his own expertise to the equipment design, illustrates the importance of the interdisciplinary effort that brought the thin film package into production.

In summary, there were two essential factors that brought through-mask plating into the manufacturing line for the thin film package:

- The test modules produced in the research laboratory readily met the performance requirements for the thin film package.
- The laboratory process was developed with continual regard for how the process would be implemented on the manufacturing line and with close interaction among research, development and manufacturing engineers.

The plating station as it was implemented on the production line is shown in Figure 16.

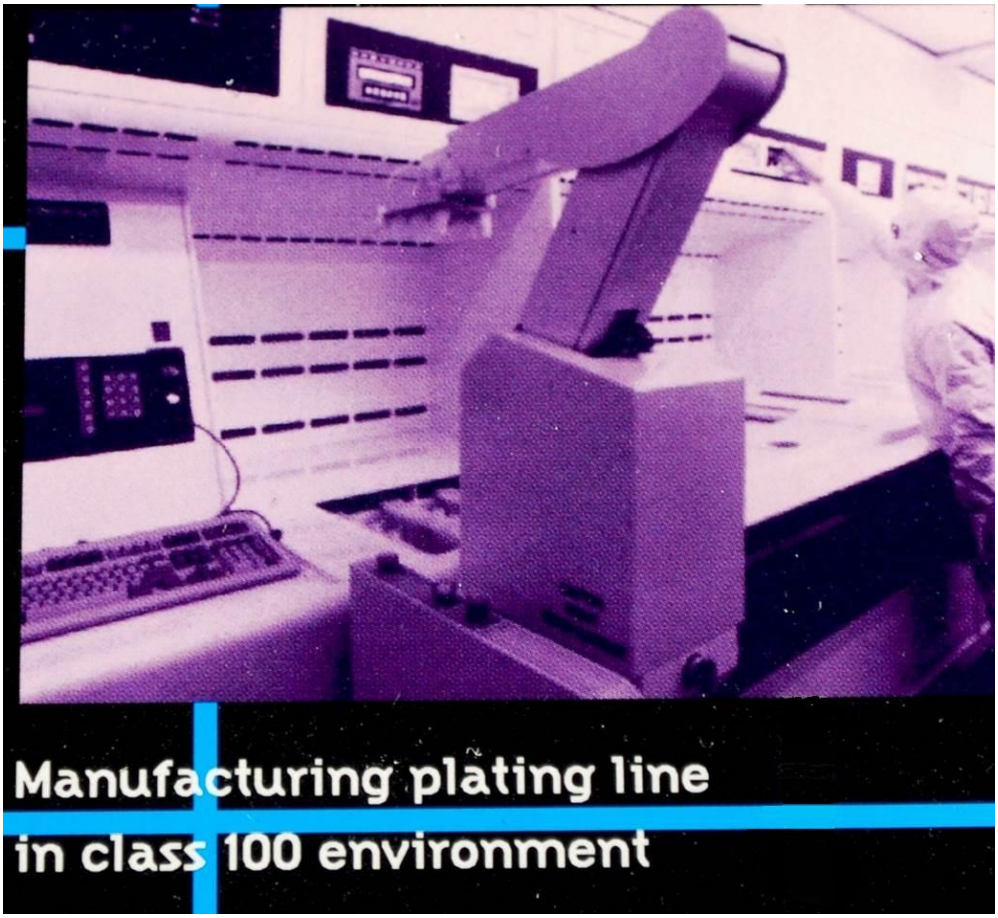

Figure 16. The plating station on the production line for the thin film package. The arm automatically moves the packaging module through the plating and rinse steps involved in fabricating the thin film structures.

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