

# IBM Research Report

## Novel Mass Reflow Method for Organic Substrates

**Vijay D. Khanna, Sri M. Sri-Jayantha**

IBM Research Division  
Thomas J. Watson Research Center  
P.O. Box 218  
Yorktown Heights, NY 10598  
USA



Research Division  
Almaden – Austin – Beijing – Brazil – Cambridge – Dublin – Haifa – India – Kenya – Melbourne – T.J. Watson – Tokyo – Zurich

**LIMITED DISTRIBUTION NOTICE:** This report has been submitted for publication outside of IBM and will probably be copyrighted if accepted for publication. It has been issued as a Research Report for early dissemination of its contents. In view of the transfer of copyright to the outside publisher, its distribution outside of IBM prior to publication should be limited to peer communications and specific requests. After outside publication, requests should be filled only by reprints or legally obtained copies of the article (e.g., payment of royalties). Many reports are available at <http://domino.watson.ibm.com/library/CyberDig.nsf/home>.

# Novel Mass Reflow Method for Organic Substrates

Vijay D. Khanna and Sri M. Sri-Jayantha  
IBM Research, T. J. Watson Research Center  
Yorktown Heights, New York 10598  
vdk@us.ibm.com

## Abstract

The warp of an organic substrate is a major challenge for bond and assembly (B&A) operations. A portable vacuum fixture that eliminates the warp by holding the substrate perfectly flat during the chip attach process is introduced in this paper. Excellent C4 height uniformity with increased B&A yield is achieved by this novel method. The fixture also makes it possible to utilize all electrically good substrates irrespective of their incoming shape. Furthermore, the electrical performance of the substrate is no longer constrained by the need to modify its circuit design to reduce the warp.

The vacuum fixture is designed to be compatible with an industry standard mass reflow oven. The design of the fixture is described along with the manufacturing challenges that were faced. A transient thermal model, leveraged to optimize the thermal mass of the fixture by a factor of two, is presented. The performance of the fixture is compared to other mechanical techniques used for clamping substrates flat. The fixture's unique ability to shape the substrate to match the warp of the chip at reflow temperatures is discussed. Finally, application of the technique to challenging chip-attach cases is explored.

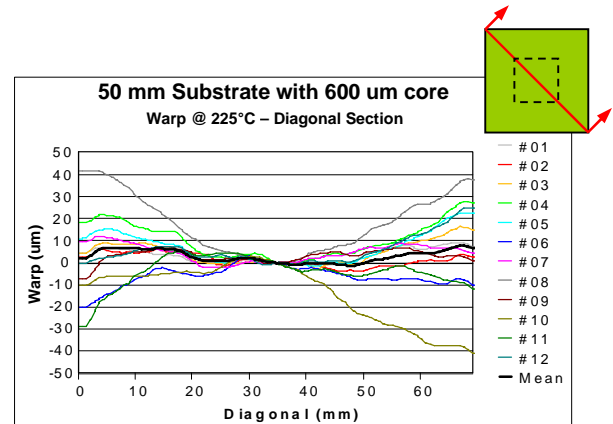
## Introduction

Organic substrates have become pervasive for the packaging of silicon die due to their superior electrical properties, ability to provide fine feature sizes and the low cost of manufacturing them. However these advantages come at the cost of higher package stresses due to a larger thermal expansion mismatch with the die and a notably higher substrate warp.

Attaching flip-chips with high C4 densities ( $>10,000/\text{die}$ ) has become increasingly difficult especially in the presence of this higher warp. Even though there are a number of geometric factors that can affect the manufacturing yields in a conventional reflow process, it has been shown that the substrate warp at reflow has a strong negative effect on chip attach [1]. As chip size and C4 density continue to increase (and C4 sizes decrease) some form of warp control becomes necessary to mitigate C4 non-wet and bridging challenges.

The warp in an organic substrate is caused by the difference in the physical properties (modulus and thermal expansion) between the resin and copper wiring that make up its structure and has a complex dependence on the layout of its various circuit layers [2]. Typically the warp changes with temperature and has a substantial statistical variation (sigma). Fig. 1 shows the measured diagonal cross-sections of 12 substrates at 225°C. Even though the mean warp of this sample is fairly low the variation between the substrates is very large.

The schematics in Fig. 2 highlight the three components of the warp that impact chip-attach. The absolute warp (actual shape) at reflow has a direct effect on C4 non-wets and bridging, the sigma makes chip-attach difficult even for substrates that have a flat sample mean warp and the thermal warp (change in shape



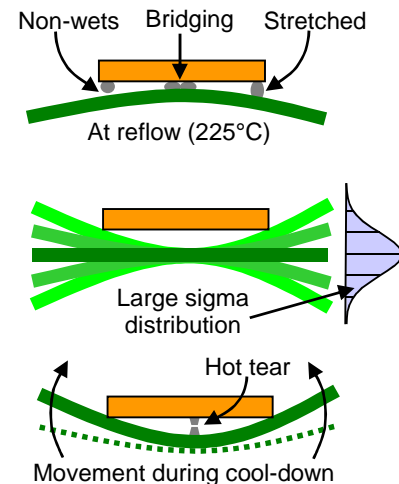
**Figure 1.** A plot of diagonal cross-sections of 12 substrates at 225°C showing the large variation in the samples.

with temperature) creates a movement that can cause defects (hot tears) in the C4s while they transition from molten to solid.

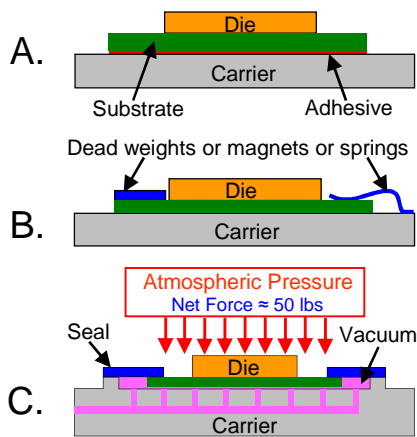
A transition to thinner core or coreless substrates makes the warp metrics worse. While design modifications to the substrates can be used to reduce the warp, such changes do not impact the statistical variation. Design modifications usually also come at the expense of electrical performance. Thus enhancements to the reflow process, which can provide warp control without compromising the substrate design, are very desirable.

## Mechanical Means for Warp Control

A number of techniques have been developed to hold a substrate flat using mechanical means. A prerequisite for all is the need to be compatible with the high temperatures of the reflow process. The schematics of these techniques are shown in Fig. 3. The first is the bonding of the substrate to a carrier that is flat and rigid with a temporary adhesive (Fig. 3A). This technique is extensively used in the thinning of silicon wafers and requires the use of lasers and/or harsh chemicals for the



**Figure 2.** The three components of warp that impact chip-attach – absolute warp, large sigma and thermal warp.



**Figure 3.** The schematics of the mechanical means that can be used to hold a substrate flat during chip-attach.

removal and cleaning of the wafer. The lasers & chemicals are unsuitable for use with the organic resins of the substrate hence alternate methods such as mechanical shearing have to be used. Cleaning of the adhesive residue is difficult so that contamination of the bottom surface of the substrate usually results.

The second technique shown in Fig. 3B is the use of springs, dead weights or magnets to press the substrate flat against a rigid surface. There is no issue of contamination with these methods but they can only apply pressure on the substrate outside the footprint of the chip. This means that an upwardly concave warp may be correctable but not a convex warp. Since most substrates tend to become progressively convex as they are heated, the need to flatten a convex shape is necessary.

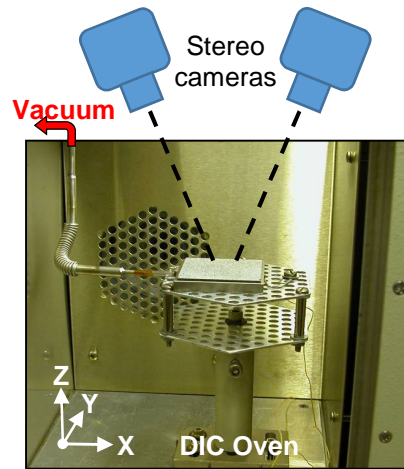
The third technique shown is the use of a vacuum to hold the substrate flat against a rigid surface (Fig. 3C). As depicted by the schematic, the vacuum permeates the complete lower surface of the substrate so that atmospheric pressure pushes down uniformly over its full top surface. This means that both concave as well as convex shapes can be flattened with a vacuum. It was because of this advantage that we made the investment to develop a vacuum fixture.

It should be noted that mention of using vacuum to flatten circuit cards for chip attach has been considered as far back as 1995 but no practical means of achieving the same has been demonstrated [3].

### Demonstration of Vacuum Clamping Effectiveness

The first task was to confirm that vacuum clamping is capable of flattening a substrate and keeping it flat during heating to reflow temperatures. This experiment was performed using a DIC (digital image correlation) system which can measure substrate warp as a function of temperature [4]. The setup is shown in Fig. 4. A 50 mm substrate, 1 mm thick (600 um core), was used for the test. The substrate (bare, with no chip attached) was placed on a vacuum chuck and heated in an oven from 25°C to 225°C at 3°C/minute. Its change in shape (in Z) was measured by the DIC's stereo cameras focused on it through a glass window in the oven wall.

The first measurement was made without any vacuum so that the substrate could warp freely. The blue trace in Fig. 5 shows the mean warp (average of the 4 corners minus the center) as a function of temperature. The substrate starts out with a large concave warp and become less concave as the temperature rises.



**Figure 4.** DIC arrangement to demonstrate that a vacuum can flatten the substrate warp.

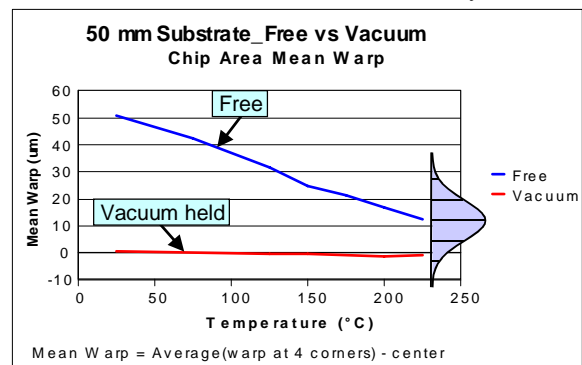
(The bell curve on the right shows the sigma in the warp behavior of the population). When repeated with the vacuum turned on, the warp behavior was very different and is shown by the red trace. The mean warp becomes virtually zero as soon as the vacuum is applied and remains zero during the complete heating-cycle.

*The fact that the mean warp is zero at all temperatures indicates that the thermal warp and the sigma of the warp are also reduced to zero.*

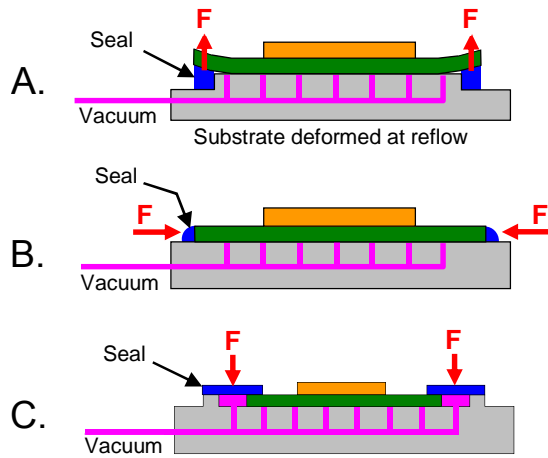
### Design of the Vacuum Fixture

Following the successful demonstration of the vacuum concept, a design effort was launched to make a practical vacuum fixture that could hold multiple substrates flat during the reflow process [5] [6]. Since there is no continuous source of vacuum from the chip placement tool to the exit of the oven, the vacuum fixture was designed with a self-contained vacuum chamber. The chamber allowed vacuum to be applied before placing the chip and maintained it till the oven exit. This was considered necessary since vacuum activation after chip placement can cause the substrate to flex and lead to chip misalignment.

The design was made compatible with conventional mass reflow ovens by making it close in size and shape to the universal tray (135 x 148 mm) used for traditional reflows. This required no major equipment modifications or capital investment for its adoption. A version of the vacuum fixture has also been designed and built to meet the JEDEC tray (135 x 315 mm) specifications. However all of the results presented in this paper have been obtained on the smaller universal tray sized fixture.



**Figure 5.** Warp behavior comparison between an unclamped substrate and one held down by a vacuum.



**Figure 6.** The three options of providing sealing between the substrate and the carrier.

*Need for Sealing:*

During the feasibility demonstration it was observed that the vacuum would leak continuously irrespective of how smooth the mating surfaces were made. Sealing at the periphery of the substrate was necessary to reduce this leakage to a value low enough that would allow the vacuum to be maintained for the duration the fixture travelled through the reflow oven. A higher leakage would necessitate a larger vacuum chamber.

In Fig. 6 are shown the three options of providing sealing between the substrate and the rigid flat surface. Fig. 6A shows the seal placed beneath the substrate with the vacuum pulling the substrate down against the seal. The sealing force pushes upwards on the substrate and causes it to deform permanently when heated. This is because at reflow temperatures the substrate becomes very pliable (the resin is far above its glass transition temperature,  $T_g$ ). This distortion was confirmed experimentally in the DIC setup of Fig.4. One solution was to use a mechanical support to push down on the substrate just above the location of the seals but this made the fixture much more complicated.

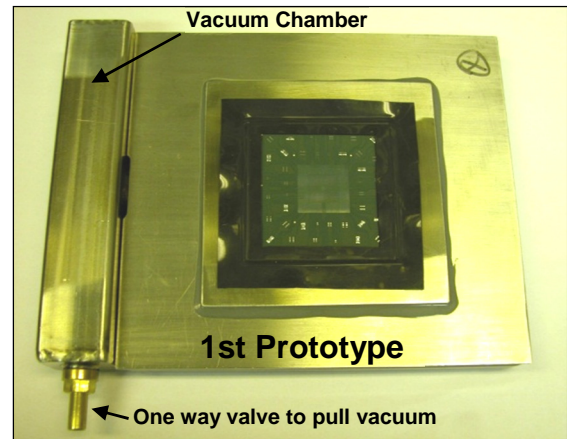
In Fig. 6B the seal is applied at the vertical edge of the substrate with the sealing force pushing inwards. Too large a force can easily cause the substrate to buckle upwards when heated. It was also difficult to achieve good sealing since the square seal tended to leak at its corners. Sealing on the substrate edge is ideal when done with temporary adhesives but that brings up the difficulties of removal and cleaning.

In Fig. 6C the seal is provided on the top surface of the substrate so that the sealing force is pressing it down against the rigid surface. With this arrangement the substrate does not distort at reflow but does require a second sealing edge between the gasket and the rigid surface. As a plus the vacuum can be used to apply the force needed to hold the seal against the substrate and the rigid surface. Due to the simplicity of this arrangement it was chosen for the vacuum fixture design.

*First Prototype:*

The first prototype of the fixture is shown in Fig. 7 and was built out of stainless steel. The vacuum chamber is the square tube on the left side of the fixture. The substrates were placed on the flat surface and the vacuum sealed by a flat rubber gasket (shown in black) being placed over the edge of the substrate. A tube connected the chamber to a hole beneath the substrate.

This prototype was tested with three different 55 mm sized substrates, all using similar 19 mm square sized chips. Two of

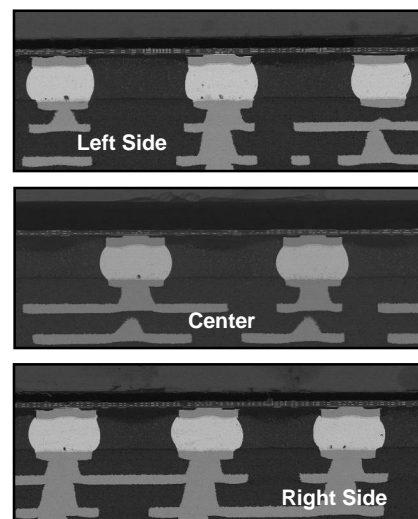


**Figure 7.** Picture of the 1<sup>st</sup> prototype of the portable vacuum fixture showing a vacuum chamber on its left side.

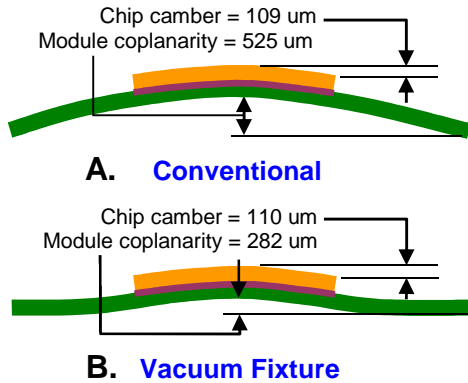
them had a core and were about 1 mm thick while the third was coreless and 450 um thick. Two samples of each substrate were chip-attached with the fixture. After cleaning and underfilling, the modules were x-sectioned and the C4 heights measured. Fig. 8 shows the pictures of a x-section from the left, center and right side of a coreless module. The C4 heights show excellent uniformity. *The delta in the C4 heights for the coreless substrate is reduced by a factor of 10 by using the fixture.* The sections of the other substrates also showed good C4 height control.

There was a second advantage obtained with the use of the vacuum fixture - the modules had a lower coplanarity compared to those made with the traditional reflow process. The schematic in Fig. 9A shows how a traditional module develops a significant camber (chip curvature) upon cooling after chip-attach and how the curvature extends outwards to the edges of the substrate. For the coreless substrate the coplanarity was so large that the module failed its specs.

When processed with the vacuum fixture, the modules had a chip camber that was of the same magnitude as the traditional modules. This indicated that the fixture did not change the final stress state of the chip in any way. However the curvature did not extend to the outer edges of the substrate. Fig. 9B shows how the outer regions were kept flat so that the module coplanarity was halved. These modules easily passed the coplanarity specs.



**Figure 8.** X-sections of a coreless module chip-attached using the 1<sup>st</sup> prototype showing excellent C4 height control.



**Figure 9.** The vacuum fixture flattens the substrate outside the chip footprint to give a lower module coplanarity.

It is proposed that *excessively warped substrates can be flattened to within the module coplanarity specs* when used with the vacuum fixture.

#### Second Prototype:

The success with the first prototype led to a second fixture being designed and built for a CSP (chip scale package) under development. In this package (Fig. 10) the CSP substrate was configured like an organic interposer between a very large chip, 28x23 mm, and a large multi-chip-module MCM carrier (not shown). The CSP substrate had an organic multilayer structure with a 200 um core and was 35x28x0.4 mm in size.

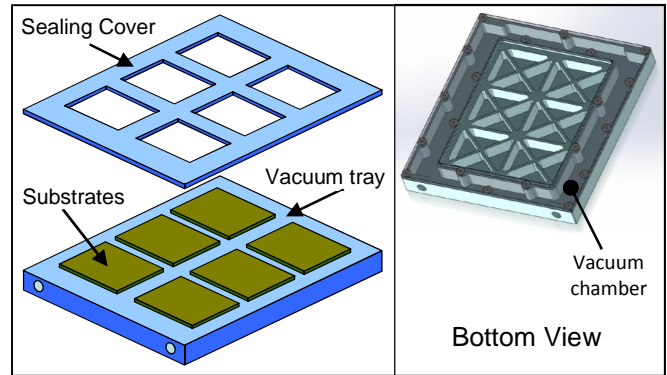
The added requirements for the new fixture were to lower its thermal mass (to reduce its time in the reflow oven) and for it to reflow multiple CSPs simultaneously. The schematic shown in Fig. 11 highlights the design of this new fixture. It was made from aluminum to improve the thermal conductivity and lower its mass and was designed to carry 6 CSP substrates. Vacuum sealing was provided by a thin aluminum seal plate that has FKM rubber gaskets along its outer edges and at the periphery of the 6 openings. Fig. 12 shows the photographs of the fixture and seal plate.

The second prototype was used successfully to chip-attach over 2 dozen CSP modules. Not a single case of C4 non-wets was observed. This was in sharp contrast to the traditional reflow process which had given approximately 25% rejects due to non-wets. The root cause was the high warp of the thin CSP substrate. The warp was eliminated with the use of the vacuum fixture and was corroborated by x-sections that showed a very uniform C4 height control (Fig. 13).

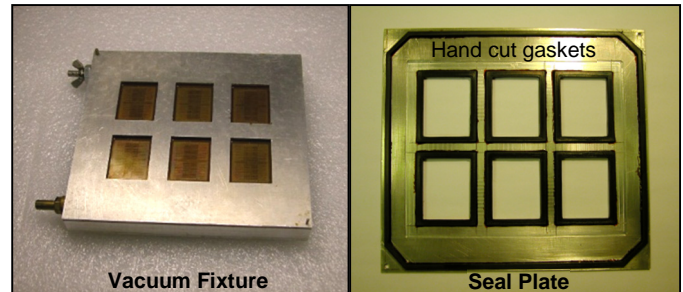
There were two further improvements needed in the design to make this fixture fully acceptable to the process engineers. The first was to reduce the thermal mass further since this fixture required the reflow oven to run at half the belt speed of



**Figure 10.** The CSP module assembled on the 2nd Prototype



**Figure 11.** 2<sup>nd</sup> Prototype can accommodate 6 CSP substrates at a time. The vacuum chamber runs along the full periphery.



**Figure 12.** The left picture shows the 2<sup>nd</sup> prototype with 6 substrates. On the right is a bottom view of the seal plate.

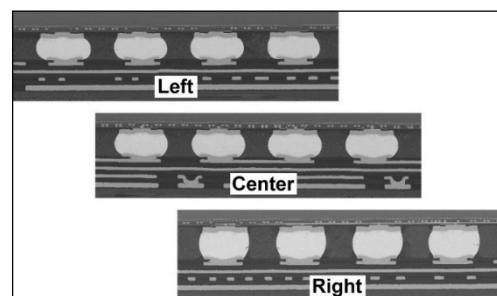
the traditional process. Secondly, a central channel was needed at the bottom of the fixture to make it compatible with the automatic feed mechanism of the chip placement tool.

#### Transient Thermal Modeling:

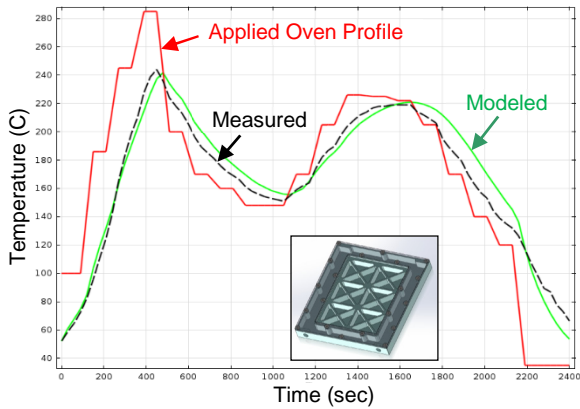
A transient thermal model of the fixture was built using Comsol [7] to understand how conduction and convection modes contributed to the temperature rise near the substrate surface. Design parameters such as wall thickness, fin-length etc. were prioritized to optimally reduce its thermal mass.

The response of the fixture to the programmed temperature profile of the oven (shown in red) was calculated for the slow oven speed. The model's thermal parameters were adjusted till a good match was obtained between the calculated temperature response and that measured on the fixture (Fig.14).

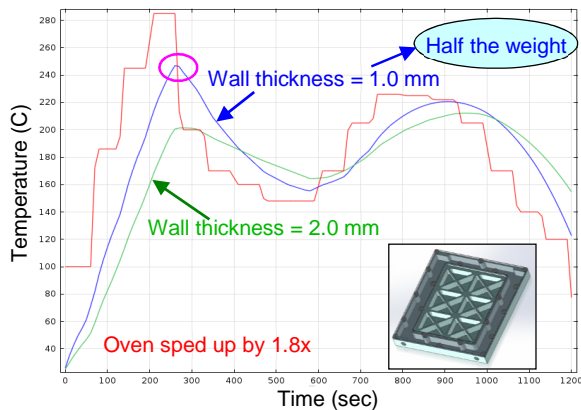
The model was then used to study the impact of reducing the wall thickness of the fixture from its original 2 mm. The results showed that the thermal response was nearly linear with the thickness. Reducing the walls to 1 mm lowered the thermal mass sufficiently to allow the oven to be sped up by a factor of 1.8 while maintaining the peak reflow temperature (Fig. 15). This reduced the process times to acceptable values.



**Figure 13.** X-sections showing the uniform C4 height control obtained from the 2<sup>nd</sup> prototype.

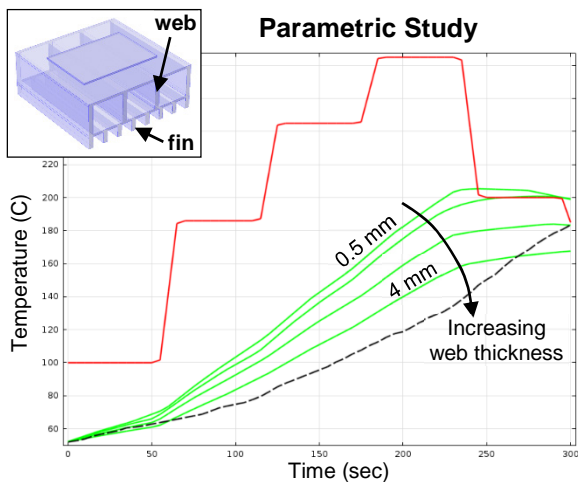


**Figure 14.** Thermal response of the fixture as a function of time in the oven. Model matches the measured results well.



**Figure 15.** Reducing fixture's wall thickness to 1 mm allows oven to be sped up while maintaining the peak temperature.

An independent parametric study was conducted to see the impact of modifying various physical dimensions of the fixture. The inset in Fig. 16 shows an isometric of a hypothetical fixture which included webs within the vacuum chamber to conduct heat from the lower surface to the top and fins at the bottom surface to improve heat absorption from the hot air of the oven. The parameters that were independently varied were the length, thickness and number of the webs and fins. The height and width of the vacuum chamber were kept constant. The plot shows a typical result of the thermal response as a function of time.



**Figure 16.** Typical parametric study results showing the effect of web thickness. The inset shows the model's cross-section.

The results can be summarized as follows -

1. Decreasing the web thickness from 4 to 0.5 mm increased the peak temperature by 40°C. This is because the thermal mass decrease had a greater impact than the loss in conduction.
2. Increasing the number of webs from 4 to 8 had practically no effect. The higher heat conduction was nullified by a higher thermal mass.
3. Decreasing the fin thickness from 4 to 0.5 mm increased the peak temperature by 18°C. Since the surface area of the fins did not change by much, the increase was mostly due to a decrease in the thermal mass.
4. Increasing the number of fins from 4 to 8 had practically no effect. The higher heat absorption due to increased area was nullified by the increase in thermal mass.
5. Increasing fin length from 5 to 20 mm increased the peak temperature by 20°C. The improved heat absorption was partially nullified by the increase in thermal mass.

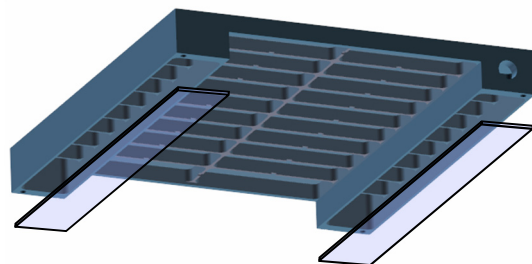
This modeling confirms that the approach taken to improve the thermal response of the first prototype (by reducing its wall thickness from 2 to 1 mm) was correct. A further reduction in thickness was not considered because of the need to maintain the rigidity of the fixture.

#### Final Prototype:

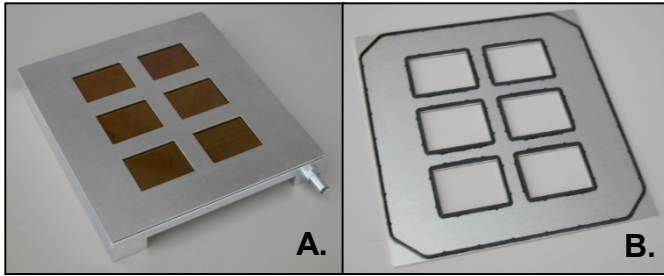
The base of the final prototype is shown in Fig. 17 which gives an isometric view of the bottom side (the top side is just a flat surface). It was made from aluminum and has a wall thickness of 1 mm throughout. The center of the bottom was recessed to make it compatible with the chip placement tool. Ribs were included in the center region to add rigidity to the top surface. The vacuum chambers are the two cavities on both sides of this central region. The chambers were closed with two aluminum plates (shown detached for clarity).

The base was made by N.C. machining a block of aluminum. Ideally a low cost process such as die casting would be used but requires large production volumes to justify the high set-up costs. The two plates had to be attached with a joint that survived repeated exposure to the high reflow temperatures. Aluminum brazing was tried but it proved difficult to obtain a good vacuum tight joint. In the end the plates were attached with laser welding. This gave excellent vacuum tight joints but introduced a warp in the structure that required a special process to eliminate.

An essential approach of the design was to make the base of the fixture common to all applications. For that reason the top surface of the base was made flat. Substrates are positioned on this surface using a thin template attached to the top surface. Each new application requires that only the template and seal plate be changed.



**Figure 17.** A bottom isometric view of the final prototype. The plates form two vacuum chambers on either side.



**Figure 18.** Left picture shows a final prototype with 6 substrates installed. On the right is a view of the molded seal plate.

The final prototype is shown in Fig. 18A fully assembled with 6 CSP substrates in place and the seal cover on top. The weight of this final version ended up being less than half the weight of its predecessor. The seal cover was made by Darcoid [8] using an injection process to mold the rubber directly onto the plate. A photograph of the seal plate is shown in Fig. 18B.

*Gasket Adhesion:*

The seal plates with the FKM rubber performed very well in holding vacuum and surviving multiple exposures to the high reflow temperatures. However they tended to strongly adhere to the counter surfaces upon cooling. Having to use force to peel the plate from the base and the substrates was undesirable from a component handling viewpoint.

To find a solution, a number of other rubber compositions were evaluated with the help of Darcoid. It was observed that changing from FKM to FFKM or silicone rubber only made the adhesion worse. When different FKM compositions were analyzed it was found that a PTFE impregnated FKM gave the lowest adhesion. This lower adhesion was still too high to be usable so an effort was made to find a surface treatment to reduce it further. Vendor provided treatments were tried but did not work effectively. Eventually a process was developed within IBM that reduced the adhesion by an order of magnitude. This treatment along with the PTFE filled FKM rubber is now the preferred sealing solution.

**Results from using the Vacuum Fixture**

The final version of the fixture has been used with multiple substrate applications with great success. Some of them are listed below.

*CSP Module:*

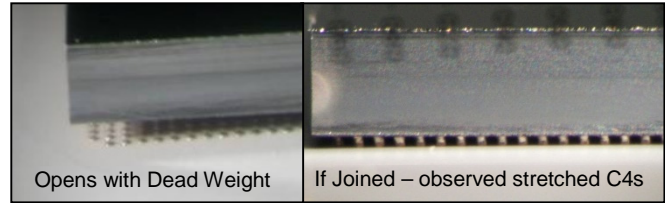
The CSP development team has used this new fixture to chip-attach nearly 150 modules till now. In all cases there were no incidents of non-wets and the C4 height control was excellent. Some modules from these builds were evaluated for reliability and passed the DTC and HAST tests with comparable results to the modules from the traditional process.

*Coreless Module for OEM:*

A module with a 50 mm coreless substrate and a large chip was giving significant rejects due to C4 bridging at one of the chip corners. The use of dead weights or springs were not successful in resolving the problem. When the vacuum fixture was used the bridging problem was eliminated.

*Experimental Coreless Substrate:*

A coreless substrate was used as a test vehicle to evaluate different top surface materials. The asymmetry resulted in the substrates having significant convex warp at reflow. Chip-attach



			Chip Join (defects)		
Cell	Top Surface	Quantity	Weights	Springs	Vacuum
1	A	24	3 / 9	1 / 9	0 / 6
2	B	24	0 / 9	3 / 9	0 / 6
3	C	24	2 / 9	4 / 9	0 / 6
4	D (POR)	12	0 / 6	0 / 3	0 / 3

**Figure 19.** The table shows that only the vacuum fixture gave zero defects. The photos highlight some of the defects.

without some form of warp control was not possible. The use of mechanical springs and dead weights were tried but did not give 100% yields. Even when the C4s joined they were highly elongated at the die corners. When the vacuum fixture was used the defects were completely eliminated and the C4 heights were uniform. These results are summarized in Fig. 19.

*Experimental CSP Substrate:*

An alternate CSP substrate was designed using a different materials set for the build-up layers to improve its high speed electrical performance. The layers were asymmetric and this resulted in a significant convex warp at reflow. Chip-attach with the traditional process was not possible. Due to the substrate being only slightly larger than the chip, warp control could only be provided by the vacuum fixture. Out of the 50 modules built there was only one reject – due to a chip misplacement error at the placement tool.

*CSP Substrate with very fine C4 Pitch:*

It is desirable to reduce the pitch and size of the C4s. To test the manufacturability of finer pitches, a set of CSP substrates and corresponding chips were made with a C4 pitch of 130 and 92.8 um. Subsequent chip-attach experiments showed that at the intermediate pitch of 130 um the traditional mass reflow methods could be made to work but at the 92.8 um pitch only the vacuum fixture would give reliable results. The only alternative was to use the more expensive technique of TCB (thermal compression bonding).

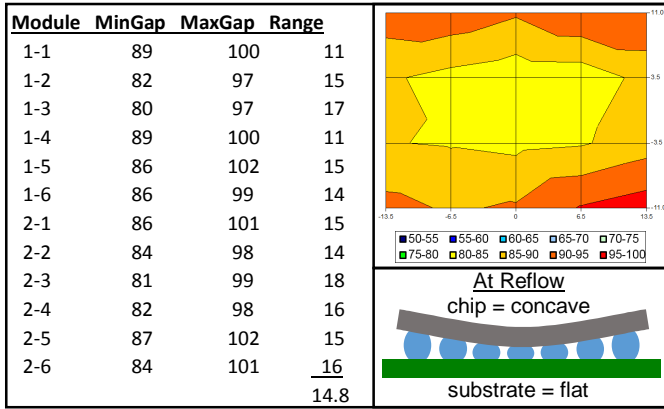
**Future uses for the Vacuum Fixture**

The following are some applications in which the vacuum fixture could provide an improved B&A solution.

*Shape Matching of the Substrate to the Chip:*

The need for shape matching is illustrated by Fig. 20. This shows the C4 height distribution of some of the CSP modules built using the vacuum fixture. A differential measurement technique developed at IBM was used. The table shows the height variation for 12 modules and is in the order of 14 um. The contour plot shows how the C4 height varies across the chip surface. Typically the heights were lowest at the center.

A measurement of the warp behavior of the chip showed that it became downward-convex by about 10 um when heated to reflow temperatures. Since the vacuum fixture was holding the substrate very flat, this curvature of the chip at reflow was showing up as the C4 height variations. This is illustrated by the schematic in Fig 20.



**Figure 20.** C4 height data for 12 CSP modules built with the vacuum fixture. Chip warp can explain the 14 um variation.

The small curvature of the chip may not be significant when the C4 heights are many times its curvature height. However for future chips that use smaller C4s or copper columns with 10-20 um of solder, the chip curvature at reflow could hinder the yield of the joining process.

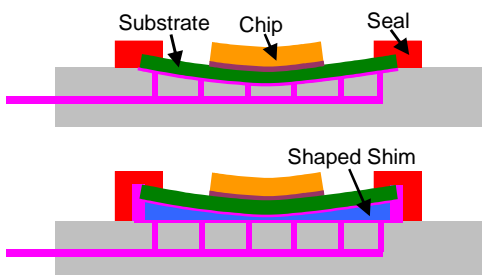
The vacuum fixture can be used to solve this challenge. The fixture uses vacuum to force the substrate to conform to the surface beneath it. If the shape of this surface is made a mirror image of the chip curvature at reflow, the substrate can be made to match the shape of the chip at the critical point of joining. How this can be achieved is shown in Fig. 21. Either the surface of the base can be machined or a shaped shim can be inserted between the substrate and the flat base.

Shape matching could allow *the successful chip attach of very small solder volume interconnects* using existing mass reflow equipment.

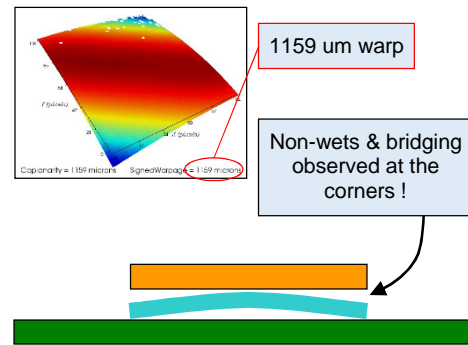
### 2.5D Module Assembly:

Most silicon interposer development falls under the umbrella of 2.5D module assembly. Silicon interposers are so thin that they nearly always have very large warps. Fig. 22 illustrates what happens when a free standing interposer is sandwiched between the chip and substrate and then reflowed. In most cases the warp of the interposer results in bridging and highly stretched, if not open, C4s. Typically this type of assembly requires the use of temporary carriers to keep the interposer flat, the subsequent removal of which makes the process more complicated.

The vacuum fixture has the potential to alleviate this problem. Fig. 23 shows how an interposer could be attached to the chip with the fixture. One would need to make the interposer slightly larger than the chip so that an edge seal could be used. A perforated plate could also be employed to provide space for C4s that may be on the lower surface of the interposer. After reflow and



**Figure 21.** Schematics showing how the vacuum fixture can provide substrate shaping to match the warp of the chip.

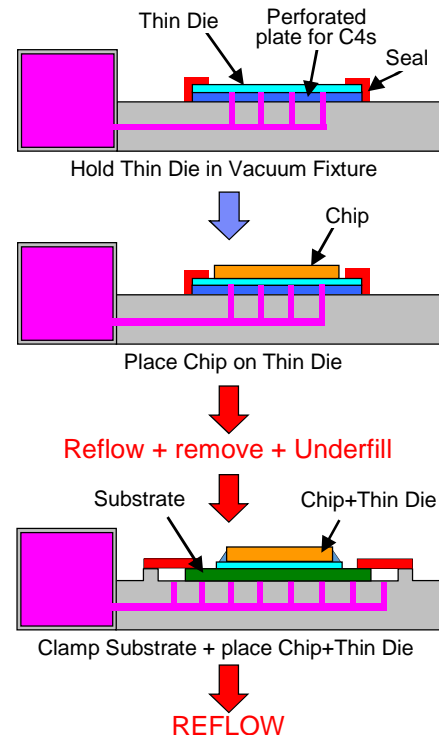


**Figure 22.** Schematic showing how the warp of an interposer chip can cause defects during chip attach.

underfilling this sub-module, it would be finally attached onto the substrate. A vacuum fixture could hold the substrate flat during reflow to ensure excellent C4 height control.

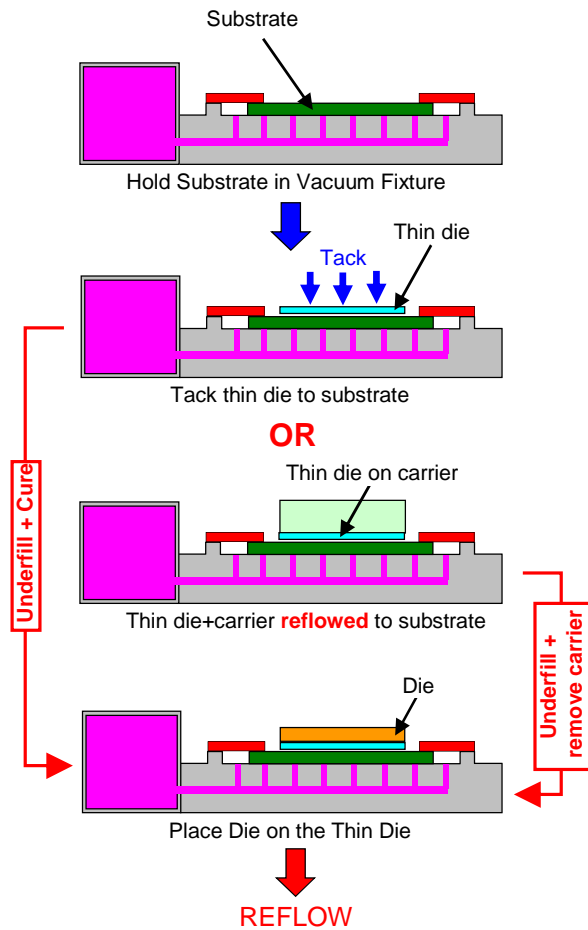
Another approach would be to assemble the interposer onto the substrate first and then attach the chip. The potential use of the vacuum fixture for this case is shown in Fig. 24. The substrate is held flat in the fixture and the interposer placed on top, either with pressure or ultrasonic tack welding, and then underfilled and cured. Without a fixture the substrate would likely flex and break the tacks before the underfill had fully cured. Alternately the interposer is attached to a temporary carrier to keep it flat and then placed on top of the substrate (with a vacuum fixture for C4 height control). After reflow and underfilling the carrier is removed.

Finally, the chip is attached to the interposer-on-substrate sub-module. This sub-module has a tendency to warp due to the CTE mismatch between the interposer and substrate and so requires a vacuum fixture to hold it flat. The tacks made earlier are made permanent during this final reflow.



**Figure 23.** Sequence showing a vacuum fixture being used to attach an interposer to chip to substrate during 2.5D assembly.





**Figure 24.** Sequence showing a vacuum fixture being used to attach an interposer to substrate to chip during 2.5D assembly.

### 3D Module Assembly:

3D assembly uses an extension of the techniques used in 2.5D assembly and faces many of the same challenges. The use of a vacuum fixture to help with 3D assembly would depend on the ability to provide sealing. As noted earlier, even very smooth surfaces (polished silicon on silicon) exhibit enough leakage that a seal is required.

One possible approach could be to make each successive chip slightly smaller than the chip below it and use the exposed edge to provide the sealing. The process would build the structure from top down with a reflow and an underfill step between each successive chip addition.

As an alternative the tack welding approach could be used to build up successive layers of the package on a substrate held flat and stationary by the fixture. Underfilling and curing could be done as each layer was attached or when the complete stack had been built.

## Conclusions

The vacuum fixture has produced 100% yield with excellent C4 height control every time it has been used. The potential of this technique to extend the usability of mass reflow to challenging chip-attach cases has been successfully demonstrated. The fixture makes it possible to utilize all electrically good substrates irrespective of their incoming shape and eliminates the need to modify (or compromise) substrate circuit design to reduce the warp. There is also potential for its use with 2.5D/3D assembly.

The use of the vacuum fixture is intended to delay the need to transition from a low cost mass reflow process to the use of TCB (thermal compression bonding). TCB is very versatile but has the disadvantage of being very expensive to install and operate. In addition, the throughput of a TCB is about one tenth that of mass reflow requiring nearly 10 TCB machines to replace each reflow oven.

## Acknowledgments

The authors would like to acknowledge the support and contributions from their colleagues at IBM, East Fishkill:

1. Charles Reynolds, *CSP Program Lead*, for his belief in and support for the capability of this technology.
2. Mark Kapfhammer, *Bond & Assembly*, for his many invaluable hours spent on running the chip-attach experiments.
3. Brian Quinlan, *Substrate Development*, for the experiments and data on the new experimental substrates.
4. David Lewison, *Bond & Assembly Development*, for the C4 height distribution measurements.

## References

1. V.D. Khanna and Sri M. Sri-Jayantha, "Impact of organic substrate warp on C4 non-wets," *IEEE Trans. CPMT*, vol.1, no. 12, pp. 1947-19xx, Dec. 2011.
2. L. Valdevit et.al., "Organic substrates for flip-chip design: A thermo-mechanical model that accounts for heterogeneity and anisotropy," *Microelectronics Reliability*, vol. 48, no. 2, pp. 245-260, Feb. 2008.
3. Akiteru Rai, "Method for Mounting Semiconductor Chip on Circuit Board," *US Patent 5,447,886*, Sep. 5, 1995.
4. "Aramis" 3D Deformation Analysis System, GOM Optical Measuring Techniques, Germany, [www.gom.com](http://www.gom.com).
5. V.D. Khanna and Sri M. Sri-Jayantha, "Stress reduction means for warp control of substrates through clamping," *US Patent 8,685,833*, Apr. 1, 2014.
6. V.D. Khanna & Sri M. Sri-Jayantha, "Vacuum Carriers for Substrate Bonding," *US Patent Application # 13/959,867*, filed Aug. 6, 2013.
7. Comsol Inc., 1 New England Executive Park, Burlington, MA 01803.
8. Darcoid Nor-Cal Seal, 950 Third Street, Oakland, CA 94607.