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SMART-P2 Requirement Specification

Version 2.0 - November 23, 1998*

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*This report replaces the version issued as RZ 2930 “Smart Requirement Specification” (June 2, 1997)

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Abstract

The architecture and function of the highly integrated and scalable mixed-signal VLSI chip called 'SMART' will be described. 'SMART' performs the physical media-dependent and transmission convergence sublayer functions for OC-3/STM-1 to OC-48/STM-16 transmission. 'SMART' is capable of handling traditional DS-N/E-N transport as well as cell (ATM) or frame (PPP) termination for campus/wide-area networks.

The 'SMART' architecture is based on a re-usable functional building block that encapsulates VC4 container into OC-3c/STM-1 frames as defined in the ITU-T, ETSI, ANSI and Bellcore standards. The novel modular scalability concept of the architecture allows interconnection of *N* such identical functional blocks (macros) in parallel to support transport rates ranging from OC-3/STM-1 up to OC-NC/STM-NC. Other functions such as Cell or Frame Delineation, VC4 Cross Connect and Automatic Protection Switching, Telecombus, UTOPIA L1 & L2 are integrated into 'SMART' as functional modules (macros) that can be programmed by the user via the microprocessor port. The scalability of the 'SMART' is not limited to macros interconnection only within a chip: a scheme is defined to operate up to four such chips in parallel to support OC-48/STM-16 transport. The analog functions of the line interface unit, consisting of clock recovery, clock synthesis, and serial-to-parallel converters, are integrated into 'SMART' VLSI to achieve cost and performance objectives essential to build highly integrated, next-generation higher-order SONET/SDH systems.

A 'SMART' VLSI has been built which contains four such SONET/SDH macros, four cell and frame delineation blocks, modified UTOPIA L1 & L2, 4-Telecom Buses, VC4 Cross Connect, and Automatic Protection Switching functions. The 'SMART' VLSI also integrates analog functions for the 4-155 and/or 1-622 line interface units. A single 'SMART' VLSI chip can be configured to handle 4-OC-3/STM-1 or 1-OC-12/STM-4 transmission. Four of these devices working in parallel with external LIU functions can handle OC-48/STM-16 transport for cell, packet, and traditional transmission applications. The lab testing of 'SMART' VLSI, because of the novel implementation techniques and guidelines, has shown that noise, i.e. coupling from high-speed digital functions to the analog circuits, is minimized and as a result the jitter generation and tolerance meet the stringent ITU and ANSI requirements for public networks.

What qualifies 'SMART' as a next-generation SONET/SDH networking chip? In our view, its modular scalable architecture for single or multiple chips and the high integration of analog and high-speed digital functions which allows the OEMs to build cost-effective OC-3/STM-1 to OC-48/STM-16 systems for wide-area and/or campus networking solutions. These systems can effectively and simultaneously transport and/or deliver cell, packet or voice traffic to the networking users for emerging high-speed services.

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Acknowledgments

SMART is the product of joint research and development between the IBM Zurich Research Laboratory, the IBM Essonnes Device Development Laboratory, the IBM T.J. Watson Research Center, and TranSwitch Corporation, Shelton, CT. The credit for realizing an integrated device with the distinctive features and flexibility of SMART goes to the entire team. In this context, we would like to acknowledge the continuous support, dedication and the many contributions to the design of the chip by our partners from TranSwitch: John Gilsdorf and Joe Pereira, our colleagues from Essonnes: J.-C. Le Garrec, P. Girard, V. Guerre, P. Hauviller, D. Louis, J.-P. Nuez, P. Mone, D. Plassat, A. Steimle, G. Taroni, V. Vallet, from Watson: M. Beakes, J. Ewen, B. Parker, D. Pearson, S. Reynolds, A. Widmer, and from Zurich: P. Buchmann, R. Clauberg, T. Engbersen, C. Landry, W. Lemppenau (now with Fachhochschule Gelsenkirchen), R. Luijten, H. Schindler, and D. Webb. The test teams from TranSwitch: Rohinton Dehmubed, Rachel Rubackin, and Mark Smith, and from Zurich: P. Bächtold, P. Dill, F. Gramsamer, H. Schindler, and H. Seitz did an outstanding job in developing the SMART test and certification environment and in characterizing the device. Representative for the people in manufacturing and testing the chips in Burlington we would like to thank S. Bueti, D. Hall, and J. Jasmin.

INTRODUCTION

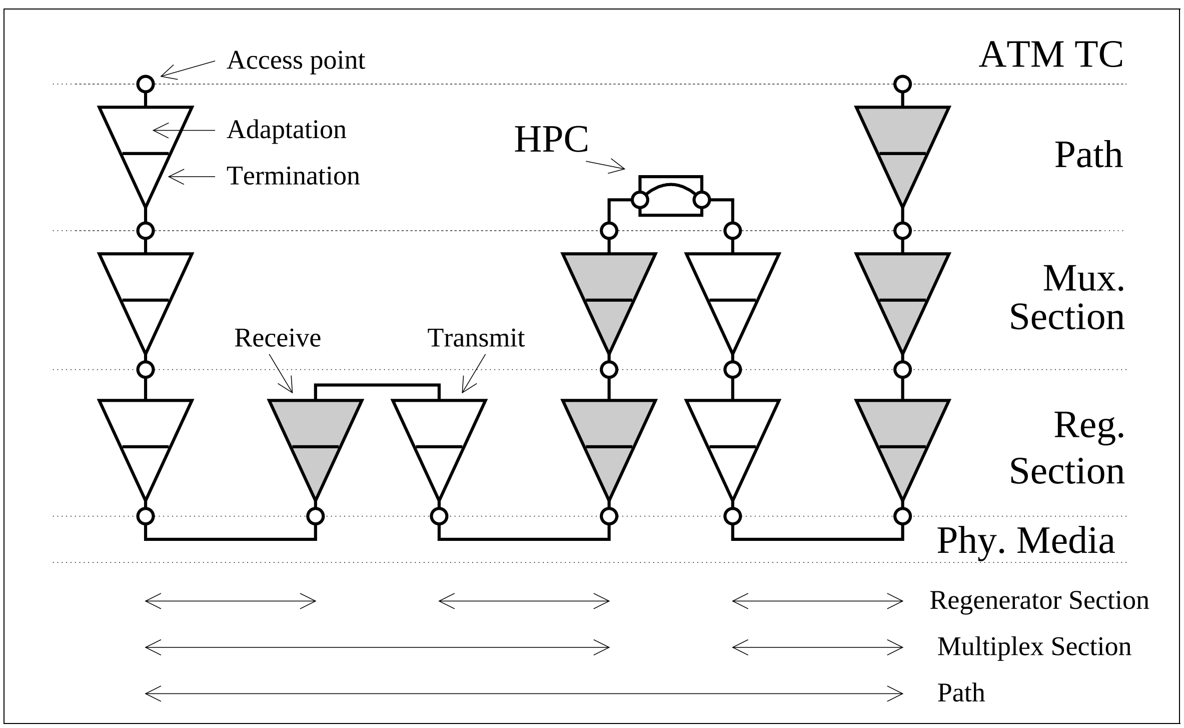
The Synchronous Digital Hierarchy (SDH), and its North-America equivalent the Synchronous Optical Network (SONET), are the globally accepted ITU-T and ANSI standards for data transmission in the public wide area network (WAN) domain. SDH and SONET have been introduced to succeed the Plesiochronous Digital Hierarchy (PDH) with the objective to overcome major limitations inherent to the PDH. In brief, SDH/SONET is characterized by a globally uniform bit-rate hierarchy covering 51 Mbps (SONET OC-1/STS-1), 155 Mbps (OC-3/STM-1) up to 9.9 Gbps (OC-192/STM-64). The global uniformity of the SDH/SONET standard will enable multi-vendor network installations and competitive prizing policies among network element equipment providers. Compared to the PDH, SDH/SONET provides significantly enhanced support for automated network and network element operation, administration and maintenance (OAM). The OAM support spreads from built-in bit-error performance monitoring to automatic protection switching (APS) techniques bypassing network failures in millisecond time frames. Last but not least, SDH/SONET provides integrated means for the cost-efficient implementation of network applications like, for example, add-drop multiplex (ADM) or digital cross-connect (DCC) systems.

With the adoption of SDH/SONET as the recommended physical layer transmission technology for the ATM UNI by The ATM Forum, ASIC manufacturers like PMC Sierra, Fujitsu, NEC, BrookTree, TI, etc., started to provide integrated SDH/SONET framer devices for the mapping of ATM cells into SDH/SONET frames. These framers of the first generation are available today at multi-ten to -hundred dollar price frames for STM-1 (155 Mbps) and STM-4c (622 Mbps) speed rates. They can be used as SDH/SONET path termination front-ends to establish point-to-point transmission links either between ATM terminals and ATM work group switches, or between ATM switch ports.

The SMART chip – a joint development between the IBM Zurich Research Laboratory, the IBM Essonnes Development Laboratory, the IBM T.J.Watson Research Center, and TranSwitch Corp. – represents an SDH/SONET framer of the second generation. While first generation SDH/SONET framer ASICs are applicable to single SDH/SONET levels only (either STM-1/STS-3c or STM-4c), the scaleability concept of SMART allows to selectively map either ATM cell, PPP frame or traditional DS-x / E-x traffic streams into STS-1, STM-1, STM-4 or STM-4c frames with a single chip. SMART provides on-chip support for exploiting the add-drop, digital cross-connect and automatic protection switching functions of SDH/SONET. In addition, SMART is a mixed-signal device with integrated analogue PLL circuitries for clock synthesis and clock recovery at STM-1 and STM-4 (622 Mbit/s) rates. Due to the unique design guidelines deployed for the analogue building blocks, SMART is the first commercially available all-CMOS SDH/SONET framer ASIC that complies to ITU-T and Bellcore requirements for jitter generation and jitter tolerance at STM-1 and STM-4. SMART is applicable not only as CPN path termination, but also as WAN multiplex section or digital cross-connect equipment.

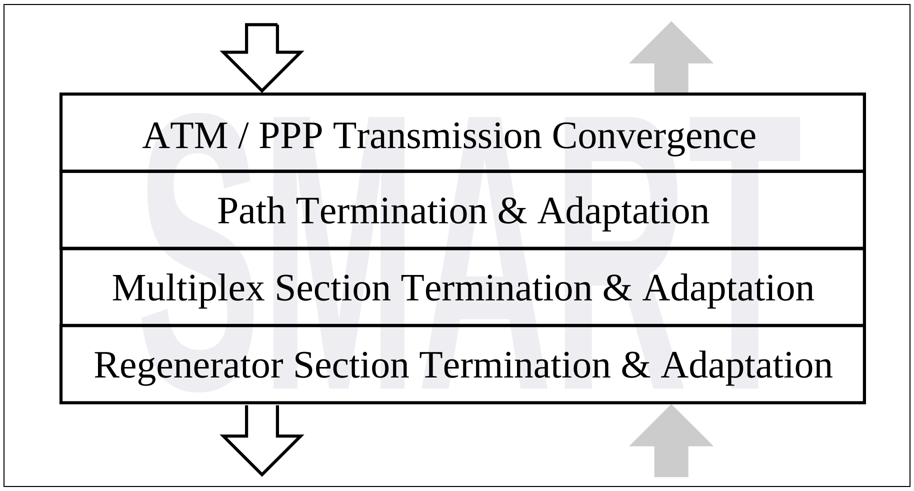
The SDH/SONET Transport Network Model

The figure below illustrates key components of a SDH/SONET-based transport network architecture. According to [G.803], the transport network is described as a layered network model and can be viewed as the physical layer infrastructure for higher-layer services. Essentially, the SDH/SONET transport network is classified into a circuit layer network, a path layer network and a transmission media layer network. The circuit layer network represents the interface to the higher-layer services. The majority of services for WAN transport networks have been and still are the traditional voice multiplex services (e.g., T1, T3 (DS-1, DS-3) lines). However, higher-layer services also include packet switched data services like, ATM and PPP, which are the services this document primarily deals with. The transmission media layer is further decomposed into a multiplex section (MS) layer, a regenerator section (RS) layer and a physical media (PM) layer. According to this layered structure of the transport network, a connection between two path layer access points is referred to as a path. A connection between two MS layer access points is referred to as a multiplex section, and a connection between two RS access points is referred to as a regenerator section. Network element equipment sourcing and sinking the layered stack up to and with the RS layer (PM plus RS) is referred to as a regenerator, equipment sourcing and sinking the stack up to and with the MS layer is referred to as a multiplexer and, finally, equipment sourcing and sinking the stack up to and with the path layer is referred to as path terminator.



Positioning

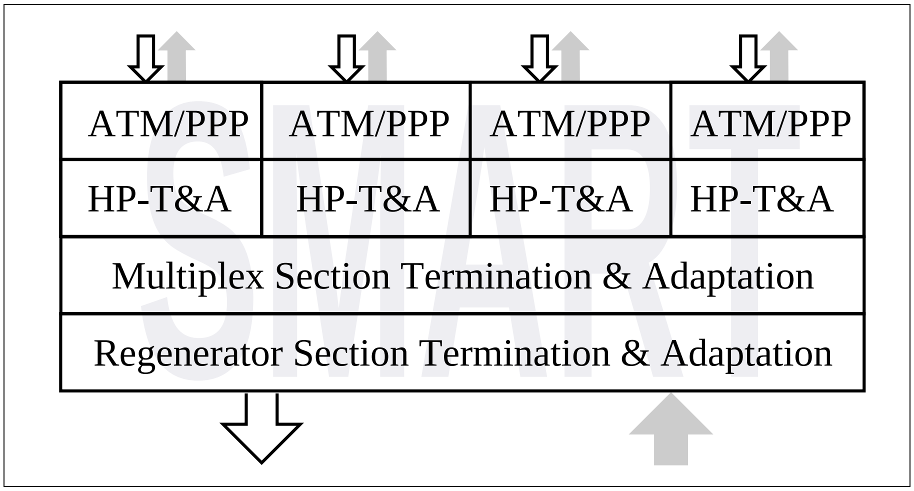
- SMART is a CMOS ASIC device designed for the mapping of ATM cell and PPP frame streams into and out of SDH/SONET transmission frames. SMART implements the SDH/SONET transport layer functions and ATM/PPP transmission convergence layer functions both in transmit and receive direction. SMART is compliant to the ITU-T SDH, Bellcore and ANSI SONET standards, as well as to The ATM Forum UTOPIA and IETF Packet over SONET recommendations (see References).



- The figure above illustrates the stack of functional layers implemented in SMART and their relation to the SDH/SONET network model depicted above. In correspondence with the detailed requirement specifications in the following section of this document, the SDH/SONET transport function has been further divided into a higher-order path termination and adaptation (HP-T&A), a multiplex section termination and adaptation (MS-T&A) and a regenerator section termination and adaptation (RS-T&A) function. Traversing the layers from ATM/PPP towards SDH/SONET is referred to as the transmit direction, whereas traversing the layers from SDH/SONET towards ATM/PPP is referred to as the receive direction.

Unique SMART Features

- SMART is **scaleable in the number and speed rates** of the supported SDH/SONET and ATM/PPP interfaces ranging from 51 Mbps up to 2.4 Gbps. For example, a single SMART chip supports up to four times STS-1 (4 x 51 Mbps), four times STM-1/STS-3c (4 x 155 Mbps ATM/PPP), one times STM-4/STS-12 (4 x 155 Mbps ATM/PPP) or one times STM-4c/STS-12c (1 x 622 Mbps ATM/PPP) interface(s). Four SMART chips operating in parallel support one STM-16/STS-48 (16 x 155 Mbps or 4 x 622 Mbps ATM/PPP) interface. The figure on top of the next page shows an example where four independent ATM cell or PPP frame streams of 155 Mb/s each are mapped into a SDH/SONET STM-4/STS-12 signal. In this configuration SMART has to provide a separate ATM/PPP TC and HP-T&A layer for each of the four cell or frame streams. A complete listing of all interface configurations supported by either a single SMART or by multiple SMART chips is described in the Section “Transport Interface Configurations”.



- SMART provides **both parallel and serial SDH/SONET line interfaces**. The parallel interface can be connected back-to-back to third-vendor serializer and deserializer devices (e.g., for OC-48 application). The serial interfaces provide direct connectivity to commercial laser drivers and optical receivers without the need for external serializer/deserializer or clock recovery components. Characterization of the SMART Testsite has shown that the serial interfaces fulfill the ITU-T, ANSI and Bellcore requirements for jitter generation and jitter tolerance at STM-1 and STM-4 speed rates.

- SMART provides **integrated add/drop multiplex (ADM) and digital cross-connect (DXC)** SDH/SONET transmission networking functionality. The ADM feature can be applied for up to two 155 Mb/s ATM/PPP streams to be inserted/extracted into/out of an STM-4/STS-12 SDH/SONET signal with a single SMART chip. The DXC feature allows the four STM-1/STS-3c received SDH/SONET signals of a single SMART chip to be arbitrarily associated to the four STM-1/STS-3c transmitter lines.

- SMART provides **direct access to the VC-3/4(-Xc)** frames. The VC-3/4(-Xc) frames may either be accessed from external via the Telecom Bus interface, or be internally transferred between the Rx- and Tx-direction. The direct VC-3/4(-Xc) access enables the applicability of SMART as SDH/SONET ADM or DXC multiplex section (MS) termination equipment inter operating with other SDH/SONET equipment in a multi-vendor environment. The direct VC-3/4(-Xc) access is the key feature to terminate and source SDH/SONET lines carrying non-ATM or PPP traffic streams.

- SMART supports the SDH/SONET inherent **automatic protection switching (APS)** capabilities. 1:n multiplex section trail protection is supported for up to STM-16 (multi-chip) operation. 1+1 multiplex section trail protection is supported for two times STM-1 in a single SMART chip.

- The SMART ATM interface is **compliant to The ATM Forum UTOPIA** recommendation. The SMART ATM interface can be configured to support either two 8-bit UTOPIA Level 1 interfaces for ATM streams of up to 155 Mbps (OC-3), or one 16-bit UTOPIA Level 2 interface for multi-PHY operation and ATM streams of 622 Mbps (OC-12c).

- The **SMART PPP interface** reuses the UTOPIA Level 2 interface pins. Four additional pins per direction (Tx and Rx) have been added to support the specifics of PPP frame transport (see Section on “External Interfaces”). The SMART PPP building blocks implement the IETF recommendation RFC1619, RFC1661 and RFC1662 for the transport of IP internet traffic over SONET/SDH. The enhanced 16-bit Fr-UTOPIA Level 2 (Frame-UTOPIA) interface for multi-PHY operation is used both for 155 Mbps (OC-3) and 622 Mbps (OC-12c) PPP frame streams.

SMART Testsite vs. SMART-P2 Product Chip

A SMART Testsite release has been built primarily for model to hardware correlation of the analogue PLL circuitry in the serial SDH/SONET interface modules. This Testsite became available in May ’97. Testing in Yorktown, with TranSwitch Corporation in Shelton, CT, and in Zurich has shown that the SMART Testsite device:

- complies to the stringent ITU-T, ANSI and Bellcore requirements for jitter generation and jitter tolerance in the wide area (WAN) environment,
- the ATM UTOPIA interface can saturate the payload capacity of both four STM-1 or one STM-4c container,
- that the SDH/SONET interface sides talk and understand with the Anritsu SDH/SONET test reference equipment, and
- that multiple SMART board interoperate seamlessly and demonstrated the SDH/SONET specific add/drop multiplex capabilities.

The following functional layers and interface of the SMART-P2 Product release have not been implemented in the Testsite:

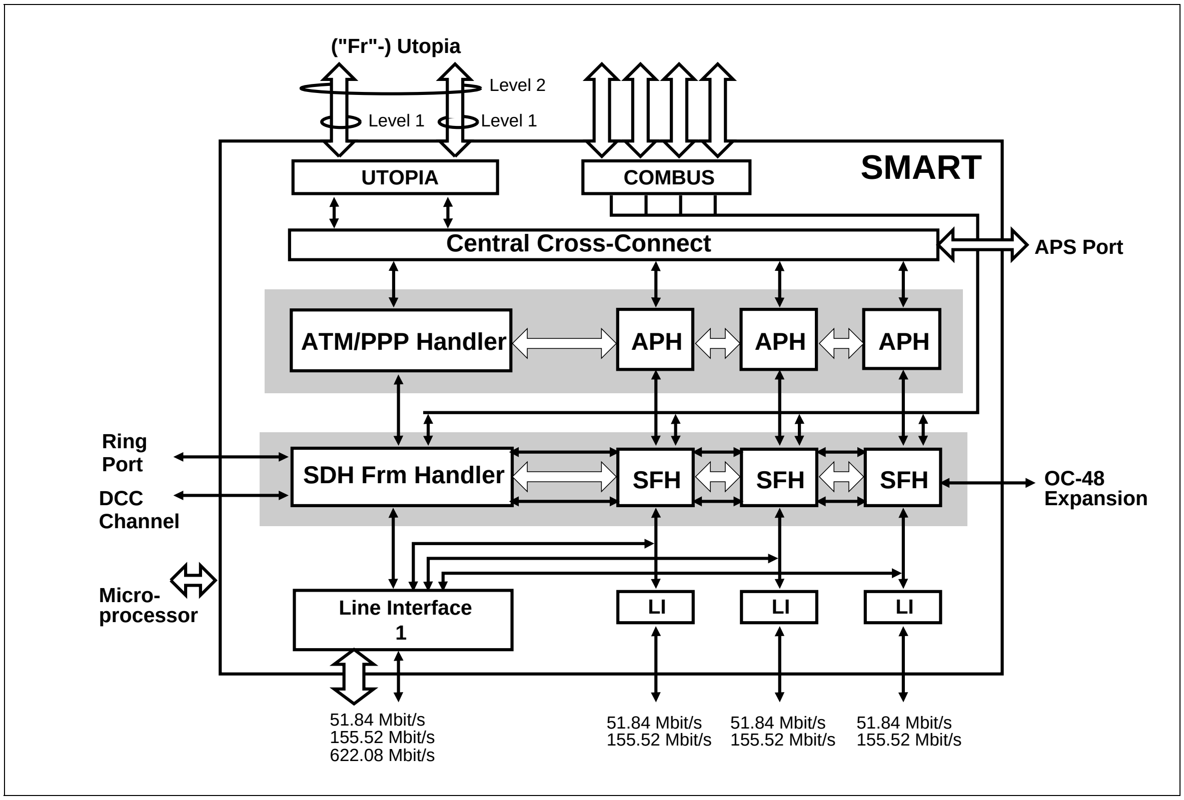
- PPP Packet over SONET/SDH layer with extension of UTOPIA Level 2 interface,
- Telecom Bus interface support for external DS-x/E-x to VC-4 mappers,
- Ring Port,
- inter-chip expansion interfaces (OC-48 support, multi-chip APS).
- chip operation for the Testsite; no 1:16 STM-1 multiplex section trail protection for STM-16 is possible. In addition, 1+1 APS will also not be available in the Testsite.

The RTM (release to manufacturing or RIT) data of the SMART-P2 Product is end April ‘98, with first user hardware devices expected in mid June ‘98. The SMART-P2 Product is a joint development between IBM and TranSwitch Corporation, Shelton, CT. TranSwitch contributed to the design with the PPP layer, and the Telecom Bus and Ring Port interfaces.

Conventions

- Throughout this document, the IBM naming conventions for bit and byte ordering are applied. Within each byte, bit 0 is the most significant bit (MSB) and illustrated at the leftmost position in a bit string or diagram. Within each word, byte 0 is the most significant byte and illustrated at the leftmost position in a byte string or diagram. Note that the IBM naming convention differs from ITU-T and Bellcore conventions (described in Sections 5 of [G.707] and 3.2.1 of [GR-253]) in that IBM numbering starts at 0, whereas ITU-T/Bellcore numbering starts at 1. In The ATM Forum naming convention bit 0 is the least significant bit and illustrated at the rightmost position in a bit string or diagram. Within each word, byte 0 is the least significant byte and illustrated at the rightmost position in all byte strings or diagram. At the transition from parallel to serial data streams (and vice versa), the MSB of a byte is transmitted/received first.

COMMON FEATURES REQUIREMENTS



A block diagram of the SMART-P2 chip is shown in the figure above.

Transport Interface Configurations

1. Table 1 below summarizes the configurations supported by either a single SMART chip, or by multiple SMART chips operating in coordinated fashion. Note, the SMART Testsite chip will support single chip configurations only.

Physical Interface	Number of SDH/SONET lines	Payload mapping	Number of ATM/PPP paths	Number of SMART chips
STS-1	4	STS-1 SPE	4 x 51 Mbps	1
STS-3	1	3 STS-1 SPE	3 x 51 Mbps	1
STM-1/ STS-3c	4	VC-4/ STS-3c	4 x 155 Mbps	1
STM-4/ STS-12	1	4 VC-4/ 4 STS-3c	4 x 155 Mbps	1
STM-4c/ STS-12c	1	VC-4-4c	1 x 622 Mbps	1
STS-12	1	12 STS-1 SPE	12 x 51 Mbps	3
STM-16	1	16 VC-4	16 x 155 Mbps	4
STM-16	1	4 VC-4-4c	4 x 622 Mbps	4

TRANSMITTER REQUIREMENTS

Transmission Convergence Sublayer Functions (TCSF)

2. The TCSF in SMART supports ATM cell, PPP frame and Telecom Bus modes.
   i. In the ATM cell mode, ATM cells are processed according to the ATM transmission convergence sublayer functions as described in [I.432]. More details are given below.
   ii. In the PPP frame mode, PPP frames are processed as described in [R1619, R1661, R1662]. More details are given below.
   iii. In the Telecom Bus mode (transparent circuit switched mode), the TCSF forwards any data unmodified towards the MSA function.
3. The TCSF in one SMART chip supports for ATM, PPP, and Telecom Bus mode either
   i. four individual data streams (up to 155 Mbps), referred to in the following as the non-concatenated mode.
   ii. one data stream (up to 622 Mbps), referred to in the following as the concatenated mode.
   iii. Concatenated and non-concatenated mode support all transport interface configurations (see table above) of the SMART chip. Note: For the TCSF, 4x STM-1 looks like 1x STM-4 or 4x STS-1. Thus, for the TCSF the only distinction to be made is the concatenated versus non-concatenated operation mode.
4. For ATM and PPP mode, SMART provides a four ATM cell (or four PPP chunks) deep elastic buffer FIFO between the external UTOPIA interface and the TCSF. The reading of ATM cells or PPP chunks out of this buffer can be enabled or disabled.

ATM transmission convergence sublayer function

[I.432, I.361] are the relevant standard references for implementing the ATM TCSF.

5. The ATM TCSF provides idle (according [I.432], chapter 4.4) or unassigned (according ITU [I.361]) cells towards the MSA functions if no cells are received from the ATM layer. Four byte registers, written by the microprocessor, provide the header bytes according [I.432, I.361].
   i. The generation of idle/unassigned cells can be enabled or disabled.
   ii. The payload bytes of the idle/unassigned cells can be preset as follows:
      - each byte of a cell has the same value (0-255) that is configurable by the microprocessor ([I.432], chapter 4.4), or
      - increment for each payload byte, start for each cell by a configurable start-value, or
      - increment for each payload byte, start for the first cell by a configurable start-value, cross cell-boundary while incrementing thereafter.

6. The HEC (fifth header byte) is provided according [I.432], Section 4.3.2, for idle/unassigned as well as ATM layer cells. The HEC calculation can be enabled/disabled.

   i. The calculated (good) HEC pattern can be corrupted by configurable PATTERNs, written by the microprocessor, as follows:
      - HEC-corrupted = ((HEC-good XOR PATTERN1) AND PATTERN2) OR PATTERN3, or
      - HEC-corrupted = HEC-good AND UDF2, or
      - HEC-corrupted = HEC-good OR UDF2, or
      - HEC-corrupted = HEC-good XOR UDF2.
      (UDF2: User DeFined 2, according to [UL2], Section 2.6).

7. The scrambling of the cell payload part is according to [I.432], Sections 4.5.1 and 4.5.3.1, for idle/unassigned as well as ATM layer cells. The scrambling function can be enabled/disabled.

8. The ATM TCSF monitors the SOC (Start of Cell) identifier of the UTOPIA interface. In case corrupted cells (cells with wrong length) were read for any reason from the buffer FIFO, the monitor mechanism is used to recover the correct cell alignment.

9. The following events are counted:
   - Number of generated idle/unassigned cells (24 bit). No threshold capability is provided.
   - Number of ATM layer cells read from FIFO (24 bit). No threshold capability is provided.
   - Number of corrupted ATM layer cells read from FIFO (bit).
   - Maskable interrupts are asserted in cases of threshold exceed.

PPP transmission convergence sublayer function

[R1619, R1661, R1662] are the relevant IETF recommendations for implementing the PPP TCSF.

10. The PPP TCSF either performs the mapping functions for PPP byte streams received from the modified UTOPIA 2 interface (Fr-UTOPIA, see section “External Interface”) according to [R1662], or forwards externally delineated HDLC packets transparently to the Transport Layer Function.

    i. The Address field of the HDLC packet shall be set to ”*FF*”$_{hex}$, the Control field to ”03”$_{hex}$, and the Protocol field to ”00*CF*”$_{hex}$.

11. A flag sequence (”7*E*”$_{hex}$) is inserted at the beginning and end of each HDLC packet. If there is no new PPP packet to transmit, consecutive flag sequence bytes are generated ([R1662], Section 4.4.1).

    i. The minimum number of flag sequence bytes between consecutive HDLC packets can be set to either one or two.

    ii. Flag sequence bytes are not generated in external delineation mode.

12. A 16-bit or 32-bit Frame Check Sequence (FCS) is calculated over Address, Control, Protocol, Information and Padding bytes of the HDLC packet (not including the Flag Sequence nor the FCS itself) according to [R1662], Section 3.1.

    i. 16-bit versus 32-bit FCS calculation are configurable.

    ii. FCS insertion and calculation can be disabled.

    iii. FCS insertion and calculation is disabled in external delineation mode.

13. After FCS computation, a byte stuffing procedure is used to escape the Flag Sequence (”$7E$”$_{hex}$) and Control Escape (”$7D$”$_{hex}$). Each Flag Sequence or Control Escape byte within the packet is replaced by a two byte sequence consisting of the Control Escape byte followed by the original control byte exclusive-or’d with “20”x. With other words,”$7D$”$_{hex}$ becomes ”$7D5D$”$_{hex}$, and ”$7E$”$_{hex}$ becomes ”$7D5E$”$_{hex}$.

    i. Byte stuffing is not performed in external delineation mode.

14. If the PPP TCSF experiences a buffer FIFO underflow, an illegal sequence (”$7D7E$”$_{hex}$) is sent and the Abort output (TxABTO) of the Fr-UTOPIA interface gets asserted. Flag Sequence bytes are forwarded to the Transport Layer Function as long as the underflow condition exists. All subsequent chunk transfers from the same packet are discarded.

15. A scrambler shall be used to optionally scramble the HDLC packet before it is forwarded to the Transport Layer Function. The scrambler polynomial is identical to the one used for ATM cell payload scrambling.

    i. Scrambling can be enabled and disabled.

Telecom Bus transmission convergence sublayer function

16. The Telecom Bus TCSF transparently forwards the byte stream(s) received from the Telecom Bus interface(s) to the Transport Layer Function. Two modes of operation can be selected:

    i. In VC-4 mode, the VC-4 or VC-4-4-c section of an STM-N or STM-Nc frame is received via the Telecom Bus interface. In this case, SMART performs pointer processing (generation).

    ii. In AU-4 mode, the entire AU-4 or AU-4-4c of an STM-N or STM-Nc frame is received via the Telecom Bus interface. In this case, SMART performs no pointer processing but takes the H1, H2, H3 bytes as part of the AU-4 from the Telecom Bus interface.

Transport Layer Functions

17. All regenerator section (RSOH), multiplex section (MSOH) and path layer (POH) overhead bytes are stored in SMART on-chip RAM from where they are retrieved for transmission in a SDH/SONET signal. Each byte is also read/write accessible from the microprocessor (that, e.g., hosts the synchronous equipment management function (SEMF)).

Lower-order path adaptation (LPA)

18. In ATM operation mode, ATM cell streams are mapped in the Container-3 (C-3), C-4 and C-4-Xc respectively, as described in Sections 10.2, 10.2.1 and 10.2.2 of [G.707]. The ATM cell byte boundaries are aligned with the Virtual Container-3 (VC-3), VC-4 and VC-4-Xc byte boundaries. Since the C-3, C-4 and C-4-Xc capacities are not integer multiples of the ATM cell length, ATM cells may cross the container frame boundaries.
19. In circuit switched (CS) operation mode, an entire VC-3, VC-4 or VC-4-Xc (consisting of a C-3, C-4 or C-4-Xc with associated POH) is received from the ATM TC layer. This VC-n frame is mapped without additional processing in the LPA and HPT layer in a SDH/SONET frame.

Higher-order path termination (HPT)

Sections 2.8.1 in [G.783], 9.3 in [G.707] and 3.3.2.3 in [GR-253] are the relevant standard references for implementing the HPT function.

20. The HPT functions described in this section are performed only when SMART is operating in the ATM operation mode. In the CS mode, the VC-n received from the ATM TC layer already contains a valid POH. This VC-n frame is mapped without additional processing in the LPA and HPT layer in a SDH/SONET frame.
21. An on-chip stored higher-order path trace identifier is transmitted repetitively in the J1 byte. Thus, the associated path receiver can verify its continued connection to the intended transmitter. Two message formats, of which one or the other can be selected through microprocessor configuration, are supported:
    i. A 16-byte path trace format is defined in Section 3 of ITU-T G.831 and also illustrated in Table 4 of Section 9.2.2.2 in [G.707]. Since the path trace information is of static nature, the microprocessor can pre-calculates the CRC-7 check sum in the first byte of the message frame. The microprocessor then writes the frame into the on-chip RAM from where it is retrieved for transmission.
    ii. Alternatively, a 64-byte free format message format can be stored on chip and retrieved for transmission.
22. A bit interleaved parity 8 (BIP-8) calculation using even parity is performed over all bits of the VC-n before scrambling. The result is placed in the B3 POH byte of the next frame.

23. The higher-order path (HP) signal label byte C2 contains composition or maintenance status information of the VC-4-Xc/VC-4/VC-3. The C2 byte is retrieved from the on-chip RAM for transmission. The default value of C2 is initialized to ”13”$_{hex}$, which indicates that the VC carries ATM cells. Other values for C2 can be set by the microprocessor according to Table 7 in Section 9.3.1.3 of [G.707] or Table 3-2 in Section 3.3.2.3 of [GR-253]. In case of transmission of an “unequipped” SDH/SONET signal, a C2 code of ”00”$_{hex}$ is transmitted.

24. The G1 path status byte conveys back to the path originator the path terminating status and performance to permit duplex path monitoring at either end.

    i. Bits 0-3 of G1 contain the count of interleaved-bit blocks that have been detected in error by the BIP-8 code in B3 of the corresponding HPT receiver.

    ii. In ITU-T (SDH) operation mode, bits 4-6 of G1 contain the VC-4-Xc/VC-4/VC-3 path remote defect indication (HP-RDI). The HP-RDI is set according to Table 8 in Section 9.3.1.4 of [G.707] when either a path alarm indication signal (HP-AIS), a loss of pointer (LOP) condition or a path trace identifier mismatch (HP-TIM) is observed, or when an “unequipped” SDH/SONET signal (UNEQ) is observed on the receive path. Upon termination of above conditions, the HP-RDI is removed.

    iii. In Bellcore (SONET) operation mode, bits 4-5 of G1 contain the STS path remote defect indication (RDI-P). The RDI-P is set according to Table 6-3 in Section 6.2.1.3.2 of [GR-253] when either a path AIS (AIS-P), a LOP-P or a UNEQ-P defect is detected. It is ensured that the RDI-P remains asserted for at least ten frames. Upon termination of above conditions, the RDI-P is removed.

25. The F2, F3 user channel, H4 position indicator, K3 automatic path protection switching and N1 network operator bytes are retrieved from on-chip RAM and inserted in the POH for transmission without further processing. The content of these bytes can be modified by the microprocessor.

Higher-order path connection function (HPC-n)

Sections 2.7 in [G.783], 6.1 and 7.1 in [G.707] are the relevant standard references for implementing the HPC-n function.

26. The HPC-n function assigns higher order VCs of level n (n = 3 or 4) at its input ports (received from the HPT function) to higher order VCs of level n at its output ports (leading to the MSA function). The HPC-n connection process does not affect the higher order VC signal format or characteristic information, but rather changes the logical sequence of the VC-ns within the SDH/SONET frame.

27. The assignment of incoming VC-ns to outgoing VC-ns is defined as the “connection pattern” which can be described by an unidirectional connection matrix $CM(V_i, V_j)$, where V_i indicates the *i*-th incoming VC signal and V_j identifies the *j*-th outgoing VC signal. The connection matrix is configured and read by the SEMF via microprocessor write/read operations.

The HPC-n function is of particular interest for add/drop multiplex (ADM) and digital cross-connect (DCC) applications, where partial or all VC-ns of the receive direction are folded back within the HPC-n layer and assigned to VC-ns in the transmit direction. The subsection “Integrated Add/Drop Multiplex and Cross-Connect Functions” in Section “EXTENDED FEATURES REQUIREMENTS” describes in detail how SMART supports these applications.

Multiplex section adaptation (MSA)

The MSA function maps the higher-order path signal into an administrative unit (AU) which is further incorporated into an AU group (AUG). *N* such AUGs are byte-interleaved to form an STM-N payload. The pointer generation function calculates the offset between the STM-N frame and the VC-4(-Xc) of an AUG. Sections 2.5.1, 2.5.3, 6.1.4.1 and Appendix B in [G.783], Sections 8.1 - 8.1.7.1 in [G.707], and 3.5.1 in [GR-253] are the relevant standard references for implementing the MSA function.

28. In case the MSA function is located in a **VC-n path source termination point** (i.e., ATM operation mode), pointer generation processing is not required. By default, a fixed pointer value (i.e., zero) is carried in the H1, H2 AU-4 pointer bytes. Pointer generation processing in ATM operation mode can be enabled via the microprocessor by setting a configuration register bit.

29. In case the MSA function is located in a **multiplex section source termination point** (e.g., loopback mode for ATM or CS mode operation), pointer generation processing is performed according to the above mentioned references to accommodate clock wander and dynamic VC-n alignment between incoming and outgoing SDH/SONET frames.

    i. Outgoing AU-4 pointer increment events, AU-4 pointer decrement events and AU-4 new data flag (NDF) events are counted in separate 8-bit counters. All counters are read accessible from the microprocessor.

30. Upon microprocessor request, a path alarm indication signal (P-AIS) is generated. The P-AIS results in H1, H2 pointer bytes set to all-’1’s..

Multiplex section protection (MSP)

Section 2.4 and Annex A of [G.783], Sections 9.2.2.9 in [G.707], and 6.2.1.1.6 in [GR-253] are the relevant standard references for implementing the MSP function.

31. SMART supports 1:*N* and 1+1 multiplex section trail protection switching.

    i. In single chip operation, the MSP provides the capacity to perform
    - 1:4 STM-1 multiplex section trail protection, or
    - two times 1+1 STM-1 multiplex section trail protection.

    ii. In multi-chip operation, the MSP can be configured to support
    - 1:N STM-1 multiplex section trail protection, where *N* can be any number in the range of 1 to 15.

iii. The data flow via the chip-external APS interface is parity protected. Parity generation and checking can be configured to odd/even as well as enabled/disabled. Detected parity errors are counted (bit).

Multiplex section termination (MST)

Sections 2.3.1 in [G.783], 9.2.2 in [G.707], and 3.3.2.2 in [GR-253] are the relevant standard references for implementing the RST function.

32. The B2 bytes are allocated in the SDH/SONET signal for a MS bit error monitoring function. This function is a bit interleaved parity $N \times 24$ (BIP-24N, with N denoting the SDH hierarchy level) code using even parity. The BIP-24N is calculated over all bits (except those in the RSOH) of the current SDH/SONET frame before scrambling and placed in the $3 \times N$ respective B2 byte positions of the next frame.
33. The automatic protection switching (APS) bytes are derived from the MSP function (see above section) and placed in the K1 and K2 byte positions of the MSOH.
34. Nine data communication channel (DCC) bytes are received from an on-board HDLC controller via an external 576 kbps serial DCC chip interface and stored in the SMART on-chip RAM. For transmission in the MSOH, the nine bytes are read from RAM and placed consecutively in the D4-D12 byte positions.
35. A synchronization status message is written to on-chip RAM by the SEMF. Table 5 in Section 9.2.2.11 in [G.707] gives the assignment of bit patterns to synchronization levels agreed to within the ITU-T. The pattern is placed in bits 4-7 of byte S1 that is transmitted as part of the MSOH.
36. If a MS-AIS or excessive error defect is detected in the receiver side MST, a MS-RDI is applied within two frames at the data signal output of the transmitter MST. The MS-RDI is defined as a SDH/SONET signal with the pattern “110” coded in bits 4-7 of byte K2. This function can be enabled/disabled by the SEMF via setting an on-chip configuration bit.
37. The order-wire byte E2 is read from on-chip RAM for transmission. The content of the E2 RAM location can be read/written by the microprocessor. No external chip interface is provided for E2.
38. The M1 byte is allocated for use as MS-REI. The byte conveys the number of detected BIP-24N errors in the associated MST receiver back to the adjacent SDH/SONET equipment. For STM-N levels, the count of interleaved bit block errors is restricted to the range of [0, $N \times 24$]. For rates of STM-16 and above, the count is truncated to 255.
39. All MSOH bytes presently reserved for national use or for international standardization are stored on-chip and shall be initialized to ”*AA*”$_{hex}$ or ”55”$_{hex}$. All MSOH bytes are accessible via the SMART microprocessor interface. No on-chip processing is provided for these bytes.

Regenerator section termination (RST)

Sections 2.2.1 in [G.783], 6.5 and 9.2.2 in [G.707], and 3.3.2.1 in [GR-253] are the relevant standard references for implementing the RST function.

40. Frame alignment bytes A1 and A2 are read from the on-chip RAM and inserted in the first row of the regenerator section overhead (RSOH).
41. The SDH/SONET signal is scrambled (except for the bytes in the first row of the RSOH) by a frame synchronous scrambler with the generation polynomial of $1+x^6+x^7$.
42. An on-chip stored regenerator section point access identifier (SAPI) is transmitted repetitively in the J0 byte. Thus, the section receiver can verify its continued connection to the intended transmitter. A 16-byte SAPI frame format is defined in Section 3 of ITU-T G.831. The microprocessor pre-calculates the CRC-7 check sum in the first byte of SAPI frame and writes the frame into the on-chip RAM.
43. Alternative to the SAPI, an STM identifier C1 may be transmitted as a unique identifier indicating the binary value of the multi-column depth coordinate. The intended mode of operation (J0 section trace or C1 insertion) is configurable.
44. A bit interleaved parity 8 (BIP-8) calculation using even parity is performed over all bits of the current SDH/SONET frame after scrambling. The result is placed in the B1 RSOH byte of the next frame before scrambling.
45. The order-wire byte E1 is read from on-chip RAM for transmission. The content of the E1 RAM location can be read/written by the microprocessor. No external chip interface is provided for E1.
46. The user channel byte F1 is read from on-chip RAM for transmission. The content of the F1 RAM location can be read/written by the microprocessor. No external chip interface is provided for F1.
47. Three data communication channel (DCC) bytes are received from an on-board HDLC controller via an external 192 kbps serial DCC chip interface and stored in the SMART on-chip RAM. For transmission in the RSOH, the three bytes are read from RAM and placed consecutively in the D1-D3 byte positions.
48. All RSOH bytes presently reserved for national use or for international standardization are stored on-chip and shall be initialized to ”*AA*”$_{hex}$ or ”55”$_{hex}$. All RSOH bytes are accessible via the SMART microprocessor interface. No on-chip processing is provided for these bytes.

RECEIVER REQUIREMENTS

Transport Layer Functions

49. All regenerator section (RSOH), multiplex section (MSOH) and path layer (POH) overhead bytes are retrieved from the received SDH/SONET signal and stored in SMART on-chip RAM. Each byte is also read/write accessible from the microprocessor.

Regenerator section termination (RST)

Sections 2.2.2 in [G.783], 6.5 and 9.2.2 in [G.707], and 3.3.2.1 in [GR-253] are the relevant standard references for implementing the RST function.

50. LOS received from the SPI is reported to the synchronous equipment management function (SEMF).

51. Frame alignment is performed by searching for the A1 and A2 framing bytes contained in the regenerator section overhead (RSOH) bytes of an SDH/SONET signal.

52. The SDH/SONET signal is continuously checked with the presumed frame start position for alignment. If the frame start position is not properly found for five consecutive frames, an out of frame (OOF) condition is declared and reported to the SEMF.

53. Loss of frame (LOF) processing is performed with configurable timer intervals in the range of 0 to 3 ms. If the OOF condition persists for T_{OOF} milliseconds, a LOF state is declared. Once in the LOF state, this state shall be left when the in-frame condition persists continuously for T_{LOF} milliseconds. A LOF condition is reported to the SEMF.

54. The SDH/SONET signal is descrambled (except for the bytes in the first row of the RSOH) by a frame synchronous descrambler with the generation polynomial of $1+x^6+x^7$.

55. Regenerator section trace processing (J0): The J0 byte is used to transmit repetitively a Section Point Access Identifier (SAPI) so that a section receiver can verify its continued connection to the intended transmitter. A 16-byte SAPI frame format is defined in section 3 of ITU-T G.831. The first byte of the frame contains a frame start marker and the result of a CRC-7 calculation over the remaining 15 bytes of the SAPI frame. The received J0 bytes are checked against an on-chip stored expected SAPI. Regenerator section trace identifier mismatches (RS-TIM) are reported to the SEMF.

56. Alternative to the SAPI, an STM identifier C1 may be received as a unique identifier indicating the binary value of the multi-column depth coordinate c. See Section 9.2.1 in [G.707] for a definition of the multi-column depth coordinate c.

57. The error monitoring byte B1 is recovered from the RSOH after descrambling and compared with the calculated BIP-8 over all bits of the previous STM/STS-N frame before descrambling. The number of B1 bit errors and number of errored blocks (according to [GR-253]) are counted in separate 16-bit counters that can be read by the SEMF.

58. The order-wire byte E1 is recovered from the RSOH and stored in on-chip RAM from where it is accessible by the SEMF. No processing is provided for E1.

59. The user channel byte F1 is recovered from the RSOH and stored in on-chip RAM from where it is accessible by the SEMF. No processing is provided for F1.

60. The data communication channel (DCC) bytes D1-D3 are recovered from the RSOH, stored in on-chip RAM and multiplexed onto an external 192 kbps serial DCC chip interface for back-to-back connection to an on-board HDLC controller.

61. All bytes for national use or future international standardization within the RSOH are recovered and stored in on-chip RAM from where they are accessible via the SMART microprocessor interface. No on-chip processing is provided for these bytes.

62. If LOS or LOF is detected, an alarm indication signal (AIS) is generated within two frames and forwarded to the MST function. The effect of the AIS is that the MST and higher layers shall treat the received SDH/SONET signal as a logical all-ones signal. The AIS is removed within 2 frames upon termination of the LOS and/or LOF failure condition.

Multiplex section termination (MST)

Sections 2.3.2 in [G.783], 9.2.2 in [G.707], and 3.3.2.2 in [GR-253] are the relevant standard references for implementing the MST function.

63. The $3 \times N$(with N denoting the SDH hierarchy level) error monitoring bytes B2 are recovered from the multiplex section overhead (MSOH). A BIP-24N value is computed for the current SDH/SONET frame. The computed BIP-24N value of the current frame is compared with the recovered B2 bytes in the following frame. The number of B2 bit errors and number of errored blocks (according to [GR-253]) are counted in separate 16-bit counters that can be read by the SEMF.

64. Every 16-bit B2 error counter has two threshold flags. These flags can be set such that an excessive error defect (corresponding to a B2 bit error rate of 10^{-3}) and a signal degrade (SD) defect (corresponding to a B2 bit error rate of $10^{-5} - 10^{-9}$) can be detected assuming a periodical reset of the counters with a one second interval. Excessive error and SD defects are reported to the SEMF via interrupts.

65. Automatic protection switching bytes K1 and K2 are recovered from the MSOH and stored on-chip. The K1, K2 bytes are processed by the MSP function as described in the next section below.

66. An MS-AIS defect is detected when the pattern “111” is observed in bits 5-7 of byte K2 in at least three consecutive frames. Removal of the MS-AIS defect takes place when any pattern other than the “111” pattern in bits 5-7 of byte K2 is received in at least three consecutive frames.

67. An MS-RDI defect is detected when the pattern “110” is observed in bits 5-7 of byte K2 in at least three consecutive frames. Removal of the MS-RDI defect takes place when any pattern other than the “110” pattern in bits 5-7 of byte K2 is received in at least three consecutive frames.

68. The MS-AIS and MS-RDI defects are reported to the SEMF via interrupts.

69. If a MS-AIS or excessive error defect is detected, then MS-RDI shall be applied within two frames at the data signal output of the MST in transmit direction. This is achieved by updating the K2 byte (bits 5-7 are set to “110”) in the on-chip RAM of the corresponding transmit function. This function can be enabled/disabled by the SEMF via setting an on-chip configuration bit.

70. The data communication channel (DCC) bytes D4-D12 are recovered from the MSOH, stored in on-chip RAM and multiplexed onto an external 576 kbps serial DCC chip interface for back-to-back connection to an on-board HDLC controller.

71. The S1 byte is recovered from the MSOH and stored in the on-chip RAM. Table 5 in Section 9.2.2.11 in [G.707] gives the assignment of bit patterns to synchronization levels agreed to within the ITU-T. Bits 4-7 of byte S1 carry the synchronization status message and the synchronization quality level that are checked for persistency against previously received messages. In case a modification in the S1 byte is observed for at least three frame cycles, an interrupt is asserted to inform the SEMF. The stored S1 byte can be read by the microprocessor.

72. The multiplex section remote error indication (MS-REI) byte M1 is recovered from the MSOH and the number of reported errors are counted in a 16-bit counter. MS-REI reflects the number of BIP-24N errors the adjacent SDH/SOENT equipment has detected. For STM-N levels, reported errors are counted only if they do not exceed the range of $[0, N\times24]$. M1 values outside this rage are interpreted as zero errors and not counted.

73. The number of locally detected BIP-24N errors is conveyed back to the adjacent SDH/SONET equipment as MS-REI in the M1 byte of the data signal output in transmit direction.

74. The order-wire byte E2 is recovered from the MSOH and stored in on-chip RAM from where it is accessible by the SEMF. No processing is provided for E2.

75. All bytes for national use or future international standardization within the MSOH of the current frame are recovered and stored in on-chip RAM from where they are accessible for a microprocessor. No processing is provided for these bytes.

Multiplex section protection (MSP)

Section 2.4 and Annex A of [G.783], Sections 9.2.2.9 in [G.707], and 6.2.1.1.6 in [GR-253] are the relevant standard references for implementing the MSP function.

76. SMART supports 1:*N* and 1+1 multiplex section trail protection switching.

    i. In single chip operation, the MSP provides the capacity to perform
       - 1:4 STM-1 multiplex section trail protection, or
       - two times 1+1 STM-1 multiplex section trail protection.

ii. In multi-chip operation, the MSP can be configured to support
   - 1:*N* STM-1 multiplex section trail protection, where *N* can be any number in the range of 1 to 15.

iii. The data flow via the chip-external APS interface is parity protected. Parity generation and checking can be configured to odd/even as well as enabled/disabled. A detected parity error is signaled to the microprocessor as a fatal error.

Multiplex section adaptation (MSA)

The STM-N payloads received from the MSA/MSP layer are de-interleaved and the VC-3/4(-Xc)s are recovered using the AU pointers. Sections 2.5.3, 6.1.4.1 and Appendix B in [G.783], Sections 8.1 - 8.1.7.1 in [G.707], and 3.5.1 in [GR-253] are the relevant standard references for implementing the MSA function.

77. The AU pointer bytes H1 and H2 are recovered from the MSOH and stored in on-chip RAM. Interpretation and processing of the H1, H2 byte contents is performed as described in the above mentioned references:

    i. In case of ATM operation mode, the C-3/4(-Xc) payload is extracted from the SDH/SONET signal and forwarded to the HPT based on the received AU pointer offset.

    ii. In case of CS operation mode, the entire VC-3/4(-Xc) is extracted from the SDH/SONET signal and forwarded to the HPT based on the received AU pointer offset.

    iii. AU-4 loss of pointer (LOP) and AU-4 path AIS defects are detected and reported to the SEMF.

    iv. Incoming AU-4 pointer increment events, AU-4 pointer decrement events, AU-4 new data flag (NDF) events and invalid AU-4 pointer defects are counted in separate 8-bit counters. All counters are read accessible from the microprocessor.

78. Note, in contrast to the MSA transmit function, pointer processing in the MSA receive function is mandatory for both ATM mode operation and CS mode operation.

Higher-order path termination (HPT)

Sections 2.8.2 in [G.783], 9.3 in [G.707], and 3.3.2.3 in [GR-253] are the relevant standard references for implementing the HPT function.

79. The HPT functions described in this section are performed only when SMART is operating in the ATM operation mode. In the CS mode, the VC-n received from the MSA layer still contains a valid POH. This VC-n frame is forwarded without additional processing to the LPA and ATM TC layers.

80. The higher-order (HO) path trace byte J1 is recovered from the VC-n POH. The processing of the J1 byte depends on the selected message format:

    i. In case the 16-byte path trace format (which is defined in Section 3 of ITU-T G.831) is selected, the J1 bytes are received until a match with the message start bit and the

CRC-7 code is observed. The following J1 bytes received are compared against the bytes of the expected message trace. In case of a mismatch, a trace identifier mismatch (TIM) defect is reported to the SEMF.

ii. In case the 64-byte free message format is selected, the J1 bytes are consecutively stored in on-chip RAM that is accessible from the microprocessor. No specific processing is performed.

81. The path error monitoring byte B3 is recovered from the VC-n POH after descrambling and compared with the calculated BIP-8 over all bits of the previous VC-n after descrambling. The number of B3 bit errors and number of errored blocks (according to [GR-253]) are counted in separate 16-bit counters that can be read by the SEMF.

82. The C2 path signal label byte is recovered from the VC-n POH and stored in the on-chip RAM.

    i. If five consecutive VC-n frames contain a C2 byte pattern equal to ”00”$_{hex}$, an unequipped defect (UNEQ) is declared and reported to the SEMF. The UNEQ defect is cleared if in five consecutive VC-n frames any C2 byte pattern other than ”00”$_{hex}$ is received.

    ii. The expected signal label is written by the microprocessor into an on-chip configuration register. The expected signal label default is ”13”$_{hex}$ (ATM mapping). If five consecutive VC-n frames contain a C2 byte different from the expected pattern, a signal label mismatch (SLM) defect is declared and reported to the SEMF. For compatibility to old equipment, no SLM defect is generated when a C2 code of ”01”$_{hex}$ (Equipped - non-specific) is received. The SLM alarm is cleared if in five consecutive VC-n frames a C2 byte pattern matching the expected signal label in the configuration register is received. Note, the five frame persistency criterion for SLM defect generation has been adopted from the UNEQ defect detection because this subject is declared for further study in the [G.783] standard.

83. The path status byte G1 is recovered from the VC-n POH.

    i. Bits 0-3 of byte G1 contain the count of interleaved-bit blocks that have been detected in error by the path BIP-8 error monitoring function (B3) in the adjacent path terminator. If a count within the legal range of values between zero and eight is received, it is accumulated in a 16-bit HP-REI counter. Received count values outside the valid range are interpreted as zero errors.

    ii. In ITU-T (SDH) operation mode, bits 4-6 of G1 contain the VC-4-Xc/VC-4/VC-3 path remote defect indication (HP-RDI). The HP-RDI analysis is performed based on Table 8 in Section 9.3.1.4 of [G.707]. A HP-RDI defect is asserted and reported to the SEMF when either bit 4 of G1 is ‘1’ or when bit 4-6 are ‘010’. Note, no persistency criterion for HP-RDI assertion and clearing is specified in ITU-T.

    iii. In Bellcore (SONET) operation mode, bits 4-5 of G1 contain the STS path remote defect indication (RDI-P). The RDI-P analysis is performed based on Table 6-3 in Section 6.2.1.3.2 of [GR-253]. The RDI-P defect is asserted and reported to the SEMF when either bit 4 of G1 is ‘1’ or when bit 4-5 are ‘01’ for five consecutive frames. The RDI-P defect is deasserted when bits 4-5 are set to ‘00’ for five consecutive frames. In addition, Bellcore specifies that RDI-P is terminated when a HP-AIS defect is detected.

84. The F2, F3 user channel, H4 position indicator, K3 automatic path protection switching and N1 network operator bytes are recovered from the VC-n POH and stored in on-chip RAM. No further processing is performed for these bytes.

Lower-order path adaptation (LPA)

85. In ATM operation mode, ATM cell streams are extracted from the Container-3 (C-3), C-4 and C-4-Xc respectively, as described in Sections 10.2, 10.2.1, and 10.2.2 of [G.707].

86. In circuit switched (CS) operation mode, the entire VC-3, VC-4 or VC-4-Xc (consisting of a C-3, C-4 or C-4-Xc with associated POH) is received from the MSA layer and forwarded without additional processing in the ATM TC layer.

Transmission Convergence Sublayer Function (TCSF)

ATM transmission convergence sublayer function

[I.432] is the relevant standard reference for implementing the ATM transmission convergence sublayer functions.

87. ATM cell delineation is performed according to the algorithm described in Section 4.5.1 in [I.432] to correctly identify ATM cell boundaries. Separate 4-bit configuration registers are provided to configure the parameters ALPHA (denoting the number of consecutive incorrect header error control (HEC) bytes received triggering the transition from SYNCH to HUNT state) and DELTA (denoting the number of consecutive correct HEC bytes received triggering the transition from PRESYNC to SYNCH state) in the range 0 - 15 via the microprocessor. The cell delineation state diagram is shown in Figure 13 in Section 4.5.1 of [I.432].

    i. Loss of cell delineation (LOC) is detected when ALPHA consecutive incorrect HEC have been received. The LOC condition is reported to the microprocessor.

    ii. LOC also results in a transmission path far end receive failure (TP-FERF) that is signaled back in the G1 byte of the HPT layer (see Req. 83 ii and iii above) to alert the equipment in the opposite direction of transmission that a defect has been detected along the path.

88. Self synchronizing ATM cell payload descrambling is performed according to Section 4.5.3.1 of [I.432]. The descrambling process can be disabled by the microprocessor through a configuration register modification. With reference to Figure 13 in Section 4.5.1, the descrambler is disabled while in the HUNT state and enabled while in PRESYNC or SYNCH state.

89. ATM cell header check and error detection are performed according to Sections 4.3 and 4.4 in [I.432]:

i. Detection of either idle cells, or unassigned cells or cells with configurable header bytes is supported. The four first bytes of a cell header are compared to four 8-bit configuration registers containing the expected header bytes. Depending on a configuration register setting, idle or unassigned cells are either discarded or forwarded to the ATM interface function.

ii. If the computed HEC is different from the received HEC, a HEC error defect has been detected. HEC error defects are counted in a 16-bit counter.

90. Transmission of the ATM cell flow towards the external ATM interface can be disabled by configuration register setting.

91. SMART can also enter the SYNCH state regardless of the cell delineation by looking at bit 8 of the received data. In this case, the first received start of cell (coded in bit 8) is used to jump into the PRESYNC state and one cycle later into the SYNCH state. This alternative is especially useful when operating in loopback mode (see "Extended Features Requirements" later in this document) where the start of cell bit 8 is set by the TCSF in transmit direction. The HEC errors are still counted, the LOC events are still signaled.

92. The TCSF contains numerous counters that individually can be accessed by the microprocessor. Counter overflow or counter threshold exceed conditions are signaled as maskable interrupts to the microprocessor.

i. Number of cells discarded due to ATM cell FIFO almost full is counted in a 16-bit counter. When LoopBack #1 is active, no counting is performed. In CS mode, the number of discarded bytes due to FIFO almost full are counted.

ii. Number of cells forwarded to the ATM cell FIFO buffer is counted in a 24-bit counter. No threshold capability is provided.

iii. Number of idle cells received from the LPA function is counted in a 24-bit counter. No threshold capability is provided.

iv. Number of detected HEC errors is counted in an 16-bit counter.

PPP transmission convergence sublayer function

[R1619, R1661, R1662] are the relevant IETF recommendations for implementing the PPP TCSF.

90. The PPP TCSF either performs the termination functions for HDLC packets received from the Transport Layer Function according to [R1662], or forwards the packets unmodified to an externally delineation function to the Fr-UTOPIA interface.

91. A descrambler shall be used to optionally descramble the HDLC packets received from the Transport Layer Function. The descrambler polynomial is identical to the one used for ATM cell payload descrambling.

i. Descrambling can be enabled and disabled.

92. The flag sequence bytes (”7*E*”$_{hex}$) at the beginning or between HDLC packets are removed.

    i. Flag sequence bytes are not removed in external delineation mode.

93. Prior to FCS computation, each Control Escape (”7*D*”$_{hex}$) byte is removed, and the following byte is exclusive-or’d with ”20”$_{hex}$, unless it is the Flag Sequence (which aborts a frame).

    i. Byte escaping is not performed in external delineation mode.

94. The PPP TCSF calculates the FCS of the received packet after all Flag Sequences are removed and the Control Escapes are converted. The FCS itself is excluded from the calculation.

    i. 16-bit versus 32-bit FCS calculation are configurable.

    ii. FCS removal and checking can be disabled.

    iii. FCS removal and checking is disabled in external delineation mode.

95. If the PPP TCSF experiences a discontinued packet stream from the Transport Layer Function or an illegal sequence (”7*D*7*E*”$_{hex}$) is received, the packet reception is terminated and the Abort output (RxABTO) of the Fr-UTOPIA interface is asserted.

Telecom Bus transmission convergence sublayer function

96. The Telecom Bus TCSF transparently forwards the byte stream(s) received from the Transport Layer Function to the Telecom Bus interface(s). Two modes of operation can be selected:

EXTENDED FEATURES REQUIREMENTS

Integrated Add/Drop Multiplex and Cross-Connect Functions

SMART provides integrated add/drop multiplex (ADM) and digital cross-connect (DXC) SDH/SONET transmission networking functionality.

96. In order to perform ADM, SMART can be configured to terminate up to two out of N VC-4/VC-3 frames contained in an STM-N/STS-N signal at the ATM (or CS) interface. The remaining VC-4/VC-3 frames are internally transferred from the Rx to the Tx function stack.

97. In order to perform DXC, SMART can be configured to internally exchange the four VC-4 frames of an STM-4/STS-12 signal between the Rx and Tx function stacks.

98. For both the ADM and DXC function, the layer at which the internal transfer between Rx and Tx stacks is performed is configurable:

    i. The internal transfer may be performed within the ATM TC layer. In this case the entire SDH/SONET transport layer functions are performed both on the received and transmitted VC-4/VC-3 frames and the C-4/C-3 payloads (i.e., ATM cell streams) are exchanged between Rx and Tx stacks.

    ii. The internal transfer may be performed after the MSA layer. In this case the SDH/SONET transport layer functions are performed up to the MSA layer only and the entire VC-4/VC-3 frames are exchanged between Rx and Tx stacks. The direct VC-4/VC-3 exchange enables SMART to operate as multiplex section equipment terminating SDH/SONET lines carrying non-ATM traffic streams.

Loopbacks

SMART supports two loopback stages in transmit direction and one loopback stage in receive direction. The loopback stages are implemented in the ATM Transmission Convergence Sublayer function (TCSF) boundaries.

99. Transmit loopback stage #1: Data is looped back towards the receive direction without performing TCSF processing. Two modes of operation are supported:

    i. Mode 1: As soon as the ATM cell buffer FIFO is not empty, the FIFO content is read and provided as is to the receive direction.

    ii. Mode 2: In addition to performing the loopback according Mode 1, the data read out of the FIFO is processed by the TCSF and forwarded towards the MSA function for transmission. Thus, an on-line (on the fly) monitoring loopback operation has been realized.

100. Transmit loopback stage #2: Data is looped back towards the receive direction after performing TCSF processing. Two modes of operation are supported:

   i. Mode 1: The TCSF provides all idle/unassigned or received ATM layer cells towards the receive direction (complete loopback).

   ii. Mode 2: In addition to performing the loopback according to Mode 1, the data provided by the TCSF is forwarded towards the MSA function for transmission. Thus, an on-line (on the fly) monitoring loop back operation has been realized.

101. Receive loopback stage #1: Data provided by the MSA receive direction is folded back towards the towards the transmit direction (line loopback) before performing TCSF processing.

102. Any combination of ATM cell mode/ transparent mode and concatenated/non-concatenated mode can be applied to all the loopback modes.

Ring Port

103. The Ring Port is a way to communicate K1, K2, K3, MS/Path-RDI, and MS/Path-REI information between receive and transmit side of associated Multiplex Section and Higher-order Path Termination sections that are located in different SMART chips. This scenario typically occurs in counter-rotating unidirectional ring applications.

   i. The Ring Port is implemented as a serial inter-chip interface consisting of 1-bit data and associated clock.

   ii. The Ring Port is alternatively used to the chip-internal exchange of K1, K2, K3, MS/Path-RDI, and MS/Path-REI information.

OC-48 Expansion

104. SMART supports OC-48 applications by operating four SMART chips, interconnected through the OC-48 horizontal expansion interfaces, in parallel and using an external SerDes device.

   i. In OC-48 mode, the SMART 8-bit parallel SDH/SONET interface is used. The external SerDes device muxes/demuxes the 32-bit data onto/from a serial 2.4 Gbps data signal with clock.

   ii. The Vitesse VS8023/24 is a OC-48 SerDes device that can be used for this purpose. SMART is compliant to the Vitesse-specific frame pulse identification.

EXTERNAL INTERFACES

ATM UTOPIA Interface

105. The SMART ATM interface is compliant to The ATM Forum UTOPIA interface specifications [UL1] and [UL2]. The SMART ATM interface is configurable to support either:

    i. two independent UTOPIA Level 1 interfaces, or

    ii. one UTOPIA Level 2 interface.

106. The SMART ATM interface provides in receive (Rx) and transmit (Tx) direction FIFO buffers for up to four ATM cells per direction.

107. Each UTOPIA Level 1 interface is characterized by:

    i. 8-bit data bus with configurable odd / even parity, or none,

    ii. cell-level handshake operating with a single physical layer (PHY) device,

    iii. transmission of 53-byte cells synchronized with start of cell (SOC) signal,

    iv. support for one cell stream of up to 155.52 Mbps,

    v. generation of a cell available (CLAV) signal from the PHY.

108. The UTOPIA Level 2 interface is characterized by:

    i. 8-bit or 16-bit data bus with configurable odd / even parity, or none,

    ii. cell-level handshake operates with single- or Multi-PHY device(s),

    iii. transmission of 53-byte cells (8-bit mode) or 54-byte cells (16-bit mode) synchronized with a SOC signal,

    iv. support for four independent cell streams of up to 155.52 Mbps (STM-4 operation) or one cell stream of up to 622.08 Mbps (STM-4c operation),

    v. port polling/selection may be controlled with 1 CLAV signal or 4 CLAV signals (1 per PHY port) for direct status or multiplexed status indication.

109. The microprocessor has read/write access to all SMART ATM interface internal configuration registers, and read access to all counters and status registers.

    i. The following status registers are present for the Rx direction:
    - Status of the 4 Ports (selected or not by UTOPIA Level 2),
    - Selected Port Address by UTOPIA Level 2,
    - Empty flag and programmable almost empty flag for each port.

    ii. The following counters are present:
    - 24-bit ATM cell counter for each Level 1 interface - no thresholds,

- 24-bit ATM cell counter for the Level 2 interface - no threshold,
- 8-bit protocol error counter for Level 2 interface - with threshold,
- 8-bit parity error counter for each Level 1 interface (in Tx only) - with thresholds.

iii. General configuration parameters:
- Parity on/off, odd/even for each Level 1 interface,
- Parity on/off, odd/even for Level 2 interface,
- Port address to support the multi-PHY operation,
- Threshold value for programmable almost empty flag of ATM cell buffer FIFO,
- STM-4c / non-STM-4c operation for 16-bit Level 2 interface.

110. Clocking:

- UTOPIA Level 1 : 0 - 25 MHz (40 ns),
- UTOPIA Level 2 : 0 - 50 MHz (20 ns).

111. The following two tables show the mapping of UTOPIA Level 1 and Level 2 interfaces onto SMART pins:

i. For transmit direction:

SMART pin	**UTOPIA Level 2**	**UTOPIA Level 1 #1**	**UTOPIA Level 1 #2**
TxUClk1	TxClk	TxClk	
TxUClk2			TxClk
TxUData(0:7)	data-byte(15:8)	data-byte(7:0)	
TxUData(8:15)	data-byte(7:0)		data-byte(7:0)
TxPrty	TxPrty	TxPrty	
TxSOC	TxSOC	TxSOC	
TxnEnb	TxEnb	TxEnb	
TxCLAV(0)	TxCLAV(0)	TxCLAV	
TxCLAV(1)	TxCLAV(1)		TxCLAV
TxCLAV(2)	TxCLAV(2)		
TxCLAV(3)	TxCLAV(3)		
TxAddr(0)	TxAddr(4)		TxPrty
TxAddr(1)	TxAddr(3)		TxSOC
TxAddr(2)	TxAddr(2)		TxEnb
TxAddr(3)	TxAddr(1)		
TxAddr(4)	TxAddr(0)		

ii. For receive direction:

SMART pin	UTOPIA Level 2	UTOPIA Level 1 #1	UTOPIA Level 1 #2
RxUClk1	RxClk	RxClk	
RxUClk2			RxClk
RxUData(0:7)	data-byte(15:8)	data-byte(7:0)	
RxUData(8:15)	data-byte(7:0)		data-byte(7:0)
RxPrty	RxPrty	RxPrty	
RxSOC	RxSOC	RxSOC	
RxnEnb	RxEnb	RxEnb	
RxCLAV(0)	RxCLAV(0)	RxCLAV	
RxCLAV(1)	RxCLAV(1)		RxCLAV
RxCLAV(2)	RxCLAV(2)		RxSOC
RxCLAV(3)	RxCLAV(3)		RxPrty
RxAddr(0)	RxAddr(4)		
RxAddr(1)	RxAddr(3)		
RxAddr(2)	RxAddr(2)		RxEnb
RxAddr(3)	RxAddr(1)		
RxAddr(4)	RxAddr(0)		

The table below shows the pin description of the ATM UTOPIA interface:

SMART pin	I/O	Type	Description
TxUClk1	I	TTL	Tx 50 MHz UTOPIA 2 clock
TxUClk2	I	TTL	Tx 25 MHz UTOPIA 1 clock
TxUData(0:15)	I	TTL	Tx UTOPIA data bus
TxUAddr(0:4)	I	TTL	Tx UTOPIA address bus
TxPrty	I	TTL	Tx Parity
TxSOC	I	TTL	Tx Start of Cell indicator
TxNEnb	I	TTL	Tx Enable (active low)
TxCLAV(0:3)	O	TTL	Tx Cell Available
RxUClk1	I	TTL	Rx 50 MHz UTOPIA 2 clock
RxUClk2	I	TTL	Rx 25 MHz UTOPIA 1 clock
RxUData(0:15)	O	TTL	Rx UTOPIA data bus
RxUAddr(0:4)	I	TTL	Rx UTOPIA address bus
RxPrty	O	TTL	Rx Parity
RxSOC	O	TTL	Rx Start of Cell indicator
RxNEnb	I	TTL	Rx Enable
RxCLAV(0:3)	O	TTL	Rx Cell Available

PPP Fr-UTOPIA Interface

112. The SMART PPP interface reuses the ATM UTOPIA Level 2 interface pins, controls and timings. Some pins have been added to specifically support variable-sized PPP packets in addition to fix-sized ATM cells.

    i. The Fr-UTOPIA interface supports either four independent VC-4 (155 Mbps) PPP packet streams (multi-PHY mode), or

    ii. one VC-4-4c (622 Mbps) PPP packet stream (single-PHY mode).

113. Packets are sent across the Fr-UTOPIA interface as 32, 48, or 64-byte blocks (chunks). These chunks are logically equivalent to a cell in ATM mode. Hence, the start of cell (SOC) indicator is used and interpreted as a start of chunk in PPP mode.

114. The PPP interface provides both in receive (Rx) and transmit (Tx) direction, and for each PPP packet stream a FIFO buffer for up to four PPP chunks of a maximum length of 64 bytes.

The table below shows the pin description of the entire PPP Fr-UTOPIA interface. Pins that have been added for the PPP support are shown with white background, pins that are identical to the ATM UTOPIA interface pins are shown with grey background.

SMART pin	I/O	Type	Description
TxUClk1	I	TTL	Tx 50 MHz PPP clock
TxUData(0:15)	I	TTL	Tx PPP data bus
TxUAddr(0:4)	I	TTL	Tx PPP address bus
TxPrty	I	TTL	Tx Parity
TxSOC	I	TTL	Tx Start of Chunk indicator
TxSOFI	I	TTL	Tx Start of Frame indicator
TxNEnb	I	TTL	Tx Enable (active low)
TxCLAV(0:3)	O	TTL	Tx Cell Available
TxEOFI	I	TTL	Tx End of Frame indicator
TxMSI	I	TTL	Tx EOF on Most Significant Byte
TxABTO	O	TTL	Tx Frame Abort
RxUClk1	I	TTL	Rx 50 MHz PPP clock
RxUData(0:15)	O	TTL	Rx PPP data bus
RxUAddr(0:4)	I	TTL	Rx PPP address bus
RxPrty	O	TTL	Rx Parity
RxSOC	O	TTL	Rx Start of Chunk indicator
RxSOFO	O	TTL	Rx Start of Frame indicator
RxNEnb	I	TTL	Rx Enable
RxCLAV(0:3)	O	TTL	Rx Cell Available
RxEOFO	O	TTL	Rx End of Frame indicator
RxMSO	O	TTL	Rx EOF on Most Significant Byte
RxCRCEO	O	TTL	Rx CRC error indicator
RxABTO	O	TTL	Rx Frame Abort

Telecom Bus Interface

115. The SMART Telecom Bus (TB) interfaces consist of four independent interfaces. Each interface is characterized as follows:

    i. 8-bit wide data,

    ii. with synchronous 19 MHz clock (nominal),

    iii. control signals indicating transmission/receipt of C1, J1 bytes and SPE payload section,

    iv. parity protection, and

    v. failure (AIS) indicator.

116. Every TB interfaces supports the transport of one VC-4 (AU-4) container. All four TB interfaces can operate in a coordinated fashion to jointly support one VC-4-4c (AU-4-4c) container.

The following table shows the pin description of the Telecom Bus interface. The #-character represents an integer in the range [1, 4].

SMART pin	I/O	Type	Description
TxCClk	O	TTL	50 MHz clock input
TxNCClk	O	TTL	inverted TxCClk
TxCFrm	O	TTL	Tx Frame reference indicator
TxCC1J1	O	TTL	(reserved for next release)
TxCSPE	O	TTL	(reserved for next release)
TxTB#Data(0:7)	I	TTL	Tx Telecom Bus data bus
TxTB#Clk	I	TTL	Tx Telecom Bus clock
TxTB#C1J1	I	TTL	Tx C1/J1 indicator
TxTB#SPE	I	TTL	Tx Synchronous Payload Envelope indicator
TxTB#Par	I	TTL	Tx Parity bit
TxTB#Fail	I	TTL	Tx Failure indicator
RxCClk	I	TTL	(reserved for next release)
RxCFrm	I	TTL	(reserved for next release)
RxTB#Data(0:7)	O	TTL	Rx Telecom Bus data bus
RxTB#Clk	O	TTL	Rx Telecom Bus clock
RxTB#C1J1	O	TTL	Rx C1/J1 indicator
RxTB#SPE	O	TTL	Rx Synchronous Payload Envelope indicator
RxTB#Par	O	TTL	Rx Parity bit
RxTB#Fail	O	TTL	Rx Failure indicator

SDH/SONET Physical Interface (SPI)

Sections 2.1.1 and 2.1.2 in [G.783], and 3.3.1.1 in [GR-253] are the relevant standard references for implementing the SPI function.

117. The SDH/SONET transport or line interfaces consist of four independent bi-directional line-interface sections (LIS). LIS #1 is configurable for 1-bit serial or 8-bit parallel operation. LIS #2 - 4 operate in 1-bit serial mode only.

Serial line interfaces

The serial line interface serializes the formatted SDH/SONET parallel data and presents the resulting bit stream to the laser driver for transmission over the physical medium. In receive direction, the serial line interfaces regenerate the serial bit streams received from the optical receiver device to form parallel data with associated timing information.

118. On-chip bit and byte clock synthesis is required for transmit direction. All four LIS use the same synthesized transmit clock. The required external reference clock can be 19.44, 38.88, 77.76 or 155.52 MHz.

119. On-chip clock and frame recovery is required for each LIS in receive direction. Each LIS is clocked independently. LIS #2 - 4 have clock-recovery PLLs for line bit-rates of 51.84 and 155.52 Mbps. LIS #1 has a clock-recovery PLL for bit rates of 51.84, 155.52, 622.08 Mbps.

The following table shows a pin description of the serial line interface:

SMART pin	I/O	Type	Description
TxSDat1(0:1)	O	PECL	Tx 622 Mbps serial data
TxSDat2..4(0:1)	O	PECL	Tx 155 Mbps serial data
TxDClkT	O	TTL	Tx divided clock
TxLPow1..4	I	TTL	Tx laser low power indicator
TxSDown1..4	O	TTL	Tx laser shut down request
RefClkT	I	TTL	Tx reference clock; 19.44, 38.88, 51.84 or 77.76 MHz
RefClkE(0:1)	I	PECL	Tx reference clock; 19.44, 38.88, 51.84, 77.76 or 155.52 MHz
RxSDat1(0:1)	I	PECL	Rx 622 Mbps serial data
RxSDat2..4(0:1)	I	PECL	Rx 155 Mbps serial data
RxDClkT1..4	O	TTL	Rx divided clock

Parallel line interfaces

120. External clock and frame recovery is required for the parallel LIS in receive direction. The parallel LIS is clocked independently. The parallel LIS supports line bit rates of 51.84, 155.52, and 622.08 Mb/s.

121. Bit and byte clock synthesis for transmit direction may be on-chip or off-chip. The required external reference clock can be 6.48, 19.44 or 77.76 MHz.

The following table shows a pin description of the parallel line interface:

SMART pin	I/O	Type	Description
TxPDat1(0:7)	O	TTL	Tx 78/19 MBps parallel data
Tx_ByClkInT	I	TTL	Tx 19 MHz reference byte clock
Tx_ByClkInE(0:1)	I	PECL	Tx 78 MHz reference byte clock
RxPDat1(0:7)	I	TTL	Rx 78/19 MBps parallel data
RxByClk1	I	TTL	Rx 78 MHz byte clock
LockDet1	I	TTL	Rx external serializer lock detect indicator
LossSig1	I	TTL	Optical receiver loss of signal indicator
OOF1	O	TTL	Rx external serializer out of frame indicator
FP1	I	TTL	Rx external serializer frame pulse
RSTCRec1	O	TTL	Reset external deserializer

Microprocessor Interface

122. The SMART chip provides a built-in processor interface. It is a MOTOROLA 68360 processor bus type interface (QUICC bus type) with the following specifications:
    - Asynchronous interface with maximum clock frequency of 50 MHz
    - Synchronous interface with maximum clock frequency of 25 MHz; the interface runs with the processor clock in this case
    - Synchronous/Asynchronous mode selectable with separate pin
    - Adaptable to other processor types that allow unlimited wait state insertion (i960C, i80186)
    - Adaptable to processors that only allow a limited number of wait states (PowerPC403), with restrictions to internal clock frequencies
    - Bidirectional data bus width of 8 bits
    - Address bus width of 14 bits
    - Control lines: R/W, ChipSelect, DataStrobe, DataAcknowledge (Ready)
    - Interrupt request capability
    - Memory mapped chip accesses

123. The built-in processor interface provides the following functionality:

    i. Global static configuration parameters, set once at initialization:
        - ATM/CS mode selection for each SDH/SONET line in Tx/Rx direction
        - SDH/SONET transport interface configuration selection in Tx/Rx direction
        - ATM TC layer internal loopback control in Tx/Rx direction
        - External clock recovery circuit reset signals (via chip pins)
        - CS parity control/mode in Tx/Rx direction
        - ATM UTOPIA interface configuration in Tx/Rx direction
        - Type of status indication for UTOPIA Level 2 interface in Tx/Rx direction
        - Association between UTOPIA ATM and SDH/SONET interfaces for data and

control in Tx/Rx
- Selection between section trace and old SDH numbering scheme in C1 byte for Tx/Rx direction
- AU pointer processing control in Tx direction
- Start of frame assertion control in Rx direction (SOF parallel to 1-st, 2-nd or 3-rd A2 byte)
- Parallel SDH/SONET interface module (PIM) mode of operation in Tx/Rx direction
- PIM clock synthesis and selection control
- PIM parallel/serial operation control in Tx/Rx direction
- Frame pattern algorithm selection for each PIM module
- Serial SDH/SONET interface module (SIM) clock frequency selection and control in both Tx and Rx direction
- SIM VCO trim control for 1 Tx and 4 Rx PLLs
- SIM I/O on/off control
- Local and digital wrap control for all SIM modules
- Reset-upon-read control for clock status, handshaking error and SIM status registers

ii. Status registers:
- Clock status of each clock island
- Handshaking errors at each chiplet interface
- SIM status: "PLL locked" indication for 1 transmit / 4 receive PLLs

iii. Chiplet interrupt handling
- Interrupt request (IRQ) status bit for each chiplet, maskable
- Handshaking error status bits for internal interfaces, maskable

iv. Chiplet clock monitoring
- Programmable clock monitor test period
- Clock status bit for each clock island

v. Reset control for individual chiplets

vi. Asynchronous Interfaces to individual chiplets
- Provides access to individual chiplet configuration registers, counters/threshold registers, interrupt/mask registers, status registers, reset registers, command registers
- Handshaking interface with metastability-hardened buffer latches
- Watchdog timer for GPP access timeout (programmable period)
- Interrupt on timeout or handshaking errors

The following table shows a pin description of the microprocessor interface:

SMART pin	I/O	Type	Description
GPPCLK	I	TTL	Microprocessor clock (up to 50 MHz)
GPData(0:7)	I/O	TTL	Microprocessor data bus
GPAddr(0:13)	I	TTL	Microprocessor address bus
GPRnW	I	TTL	Motorola: Read/notWrite; Intel: notWrite
GPDS	I	TTL	Motorola: Data Strobe; Intel: notRead
GPDTACK	O	TTL	Motorola: Acknowledge; Intel: Ready
SMARTSel	I	TTL	SMART chip select
SMARTInt	O	TTL	SMART interrupt request
IntfMode	I	TTL	Interface mode: H = sync; L = async
IntfSelect	I	TTL	Interface select: H = Intel; L = Motorola

Serial DCC Interfaces

124. The SMART chip has four independent DCC interfaces.

   i. Each DCC interface can be configured to support either the DCC channel D1-D3 or D4-D12.

   ii. In transmit direction, the DCC interface comprises:
   - one data input (T1Data1..4), and
   - the associated continuous bit clock output (T1DClk1..4).

   iii. In receive direction, the DCC interface comprises:
   - one data output (R1Data1..4),
   - the associated continuous bit timing output (R1DClk1..4).

The following table shows a pin description of the serial DCC interface:

SMART pin	I/O	Type	Description
T1Data1..4	I	TTL	Tx serial data macro # 1 - 4
T1DClk1..4	O	TTL	Tx clock macro # 1 - 4
R1Data1..4	O	TTL	Rx serial data macro # 1 - 4
R1DClk1..4	O	TTL	Rx clock macro # 1 - 4

Inter-Chip Expansion Interfaces

APS Interface

The following tables show the pin description for the inter-chip expansion interfaces for APS, BIP, and RDI processing which are used in case of multi-chip operation for STM-16 (OC-48):

SMART pin	I/O	Type	Description
TxAPSDat(0:8)	I/O	TTL	Tx APS data bus
TxAPSPar	I/O	TTL	Tx APS parity
TxAPSDAVA	I/O	TTL	Tx APS data valid
TxAPSDARQ	I/O	TTL	Tx APS data request
RxAPSDat(0:8)	I/O	TTL	Rx APS data bus
RxAPSPar	I/O	TTL	Rx APS parity
RxAPSDAVA	I/O	TTL	Rx APS data valid

OC-48 Expansion Interface

SMART pin	I/O	Type	Description
TxExpIn	I	TTL	Tx serial expansion interface input
TxExpOut	O	TTL	Tx serial expansion interface output
RxExpIn	I	TTL	Rx serial expansion interface input
RxExpOut	O	TTL	Rx serial expansion interface output
TxFrmIn	I	TTL	Tx chip synchronization frame pulse input
TxFrmOut	O	TTL	Tx chip synchronization frame pulse output

Ring Port Interface

SMART pin	I/O	Type	Description
TxRingD	I	TTL	Tx serial ring port data
TxRingClk	I	TTL	Tx ring port clock
RxRingD	O	TTL	Rx serial ring port data
RxRingClk	O	TTL	Rx ring port clock

Clock Distribution

125. The clock distribution to the various parts of the SMART chip is controlled by global configuration parameters that the microprocessor writes into the chip BEFORE the reset signals to the individual chiplets are released.

JTAG Boundary Scan, LSSD, System, and Test pins

126. The SMART chip has provisions for Boundary Scan testing and is fully compliant with IEEE Std 1149.1-1994 (JTAG).

The following table shows a pin description of the JTAG boundary scan, LSSD, System and Test interfaces:

SMART pin	I/O	Level	Comment
LSSD_A	I	TTL	LSSD clocks
LSSD_B	I	TTL	
LSSD_C	I	TTL	
SIM_ECL	I	TTL	
TestGRAC	I	TTL	GRA LSSD_C test clock
RI	I	TTL	Receiver inhibit
DI1..2	I	TTL	Data inhibit 1 and 2
LT	I	TTL	Leakage test (default H)
N_FRESET	I	TTL	Flush reset
Test_Mode	I	TTL	Test enable
IOTest	I	TTL	LSSD scan enable
TCLK	I	TTL	JTAG test clock
TRST	I	TTL	Test reset
TMS	I	TTL	Test mode select
TDI	I	TTL	Test data input
TDO	O	TTL	Test data output
NCTY(0:1)	I	TTL	
LSSD_TAP_C1	I	TTL	
LSSD_TAP_C2	I	TTL	
NCTZ(0:1)	I	TTL	
TCSEN	I	TTL	Test enable
PLLTest	I	TTL	Wafer PLL test
MUXDivClk	O	TTL	Wafer PLL test clock output
MUXLock	O	TTL	Wafer PLL test lock indicator

SMART System Pins

SMART pin	I/O	Type	Description
ACHClk	I	TTL	ACH 25 MHz clock
SMARTAddr(0:2)	I	TTL	SMART chip address

Miscellaneous

SMART pin	I/O	Type	Description
Alarm1..4(0:4)	O	TTL	Alarm indicators
RxCAP#P	I	WIRE	On-card CAP pins
RxCAP#N	I	WIRE	
TxCAPP	I	WIRE	
TxCAPN	I	WIRE	
SDatOut	O	WIRE	Analogue diagnostic pins
RClk00	O	WIRE	
VCExt	O	WIRE	
IRefTest	O	WIRE	

Power Supply and Input/Output Requirements

127. The SMART chip is powered with a 3.3 V power supply. With the exception of special PECL clock pins and analog signal pins all I/O drivers and receivers are fully 5.0 V TTL compatible. All drivers are 50 Ohm source-terminated.

128. The SMART-P2 Product will come in 25 × 32.5 mm CBGA dual power supply package with a total of 474 leads. The digital logic and the analogue circuitry of the chip each have separate sets of VDD pins (both sourced with the nominal supply voltage of 3.3 V). On the substrate of the module there are eighth VDD to GND decoupling caps and five VCO caps for the analogue PLLs.

REFERENCES

[I.361] ITU-T, Integrated Services Digital Network (ISDN) - Overall Network Aspects and Functions, (11/95)

[I.432] ITU-T, B-ISDN User-Network Interface - Physical Layer Specification, (03/93)

[G.707] ITU-T, Network Node Interface for the Synchronous Digital Hierarchy, (07/95)

[TD.54] ITU-T, TD 54, Agreed Changes to the Text of Draft Revised Recommendation G.707, (11/95)

[G.781] ITU-T, Structure of Recommendations on Equipment for the Synchronous Digital Hierarchy (SDH), (11/92)

[G.782] ITU-T, Types and Characteristics of Synchronous Digital Hierarchy (SDH) Equipment, (01/94)

[G.783] ITU-T, Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks, (01/94)

[G.803] ITU-T, Architectures of Transport Networks Based on the Synchronous Digital Hierarchy (SDH), (03/93).

[GR-253] Bellcore, GR-253-CORE, Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria, (12/94)

[R1619] IETF, RFC1619, PPP over SONET/SDH, (05/94)

[R1661] IETF, RFC1661, The Point-to-Point Protocol (PPP), (07/94)

[R1662] IETF, RFC1662, PPP in HDLC-like Framing, (07/94)

[UL1] ATM Forum, UTOPIA - An ATM PHY Interface Specification, Level 1, Version 2.01, (03/94)

[UL2] ATM Forum, UTOPIA - An ATM PHY Interface Specification, Level 2, Version 0.95, (06/95)