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Research Report

Single Chip 622 Mb/s SDH/SONET Framer, Digital Cross-Connect and Add/Drop Multiplexer Solution

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Abstract

This paper presents a single chip CMOS solution for 4 times OC-3c, OC-12 and OC-12c SDH/SONET framing with integrated serial line interfaces. Outstanding features of this chip are clock recovery and fulfillment of ITU-T and BellCore jitter requirements for SDH/SONET systems, as well as the large range of functions offered. These functions include ATM and PPP support, digital cross-connect, add/drop multiplexing and automatic protection switching.

Chip Architecture

To optimize cost for Synchronous Digital Hierarchy/Synchronous Optical Network (SDH/SONET) systems (1) we have integrated the whole SDH framing function, including asynchronous transfer mode (ATM) cell and point-to-point protocol (PPP) packet handling, with the serializer/deserializer and clock recovery function on a single VLSI chip in CMOS technology within a nearly standard ASIC methodology. For OC-3c this was done before by other groups (2) while it was never achieved before for 622Mb/s or higher speed signals. At the same time our Scaleable Modular Architecture for SDH/SONET Technology (SMART) (3,4) allows to extend the functionality with digital cross-connect, add/drop and native SDH multiplexing with practically no additional cost in silicon area and our chip fulfills the stringent ITU-T and Bellcore jitter requirements for SDH/SONET systems at 4 x 155 Mb/s and 622 Mb/s with CMOS based technology.

The modular architecture is based on a single macro for processing STM-1 frames. Interconnecting N identical macros allows the processing of STM-N and STM-Nc frames by handling certain functions in a distributed fashion across the N macros while each macro is running with the clock rate for STM-1. Fig. 1 shows our chip based on four such bi-directional macros. Each macro consists of an ATM/PPP handler and an SDH frame handler part. The ATM/PPP handler includes a four ATM cell deep FIFO buffer and performs all ATM cell or PPP packet handling functions. The SDH frame handler includes another buffer stage for clock rate decoupling in digital cross-connect, automatic protection switching (APS), and loop back operations. Other main components of the chip are the four serial line interfaces, an Utopia level 2 interface, a COMBUS interface, a central cross-connect stage, and an OC-48 expansion port. While all other parts are purely digital the line interfaces form a mixed-signal design which is integrated with the digital part in the physical design phase.

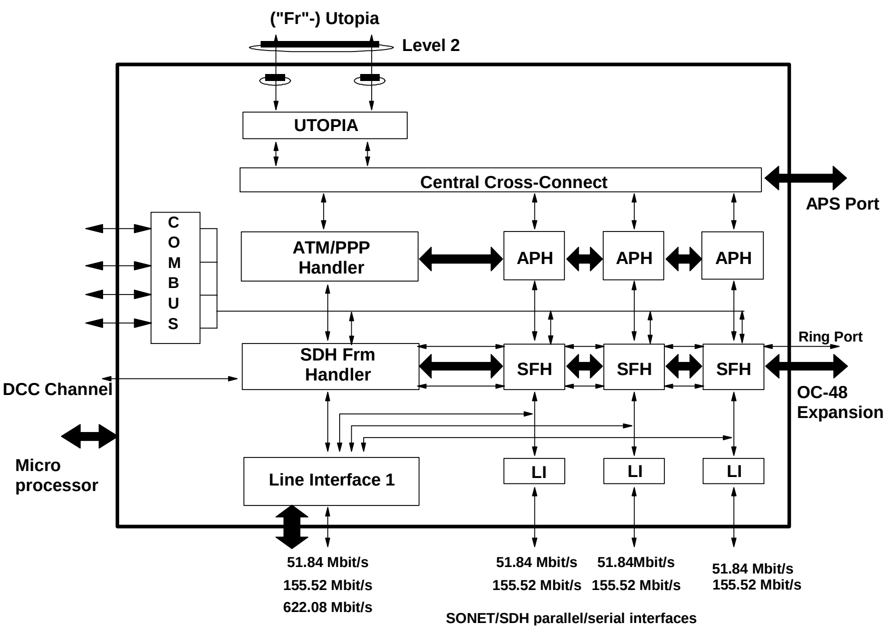

Fig. 1: Chip Architecture

The serial line interface consists of a single custom transmitter clock synthesis macro (TxPLLA), four copies of a custom receiver clock and data recovery macro (RxPLLA), and a small amount of digital logic required for feedback dividers, serializer/deserializer function, SONET frame synchronization, lock to reference indication, automatic vco trim, and PLL test logic. These PLLs are based on designs described in (5) and (6).

The TxPLLA macro is shown in Fig. 2. It provides the high speed clocks required to serialize the parallel data at the four transmitters. It incorporates a digital phase/frequency detector, charge-pump filter, feedforward compensation for stability, and a delay interpolating current-controlled oscillator, (CCO). Three different charge pump filters may be selected; an on chip capacitor, an on module capacitor, (the primary design point), an on card capacitor, or any combination of these.

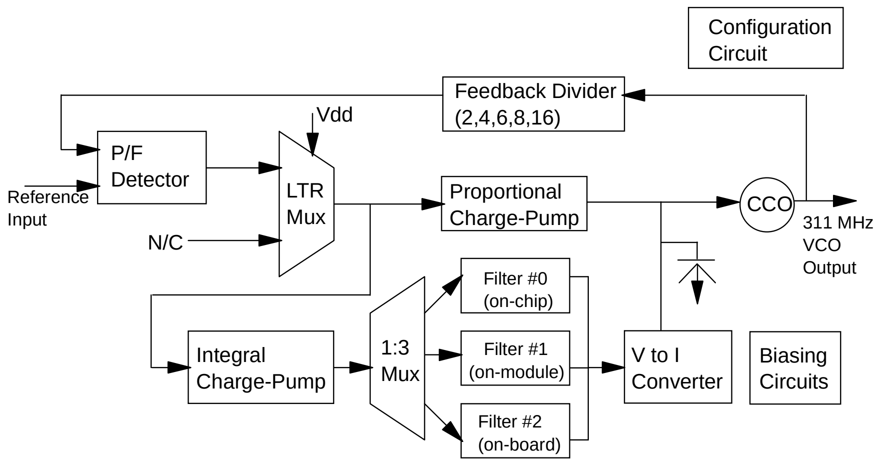

Fig. 2: Block diagram of TxPLLA

The RxPLLA macro is shown in Fig. 3. From the full rate serial data, it recovers half rate clock and data which is sent forward to the digital deserializer logic. The RxPLLA macro uses the same CCO, phase-frequency detector, charge pump and filter as the TxPLLA macro, but also includes a phase detector. The outputs from the phase detector and phase frequency detector are MUXed together into the charge pump under control of the lock to reference status signal.

The principle of the 622 MHz PLL design, which allows fulfillment of the stringent ITU-T and Bellcore jitter requirements in an all CMOS implementation, is to run the circuitry at 311 MHz and use the 0^0, 90^0, 180^0, and 270^0 phase values for either transmitting or receiving the serial data stream.

The Utopia interface allows ATM cell transmission to and from an ATM layer device as well as corresponding transmission of PPP packets for IP over SONET. To support transmission of PPP packets over the Utopia interface, the interface was extended by five ports in each direction. The COMBUS interface allows the direct mapping of VC-4 containers in and out of the SDH/SONET frames by using commercial T3 mapper devices. The central cross-connect stage is needed for transmitting the data between the 2-byte Utopia interface and the four SMART macros with 1-byte data paths each and implements digital

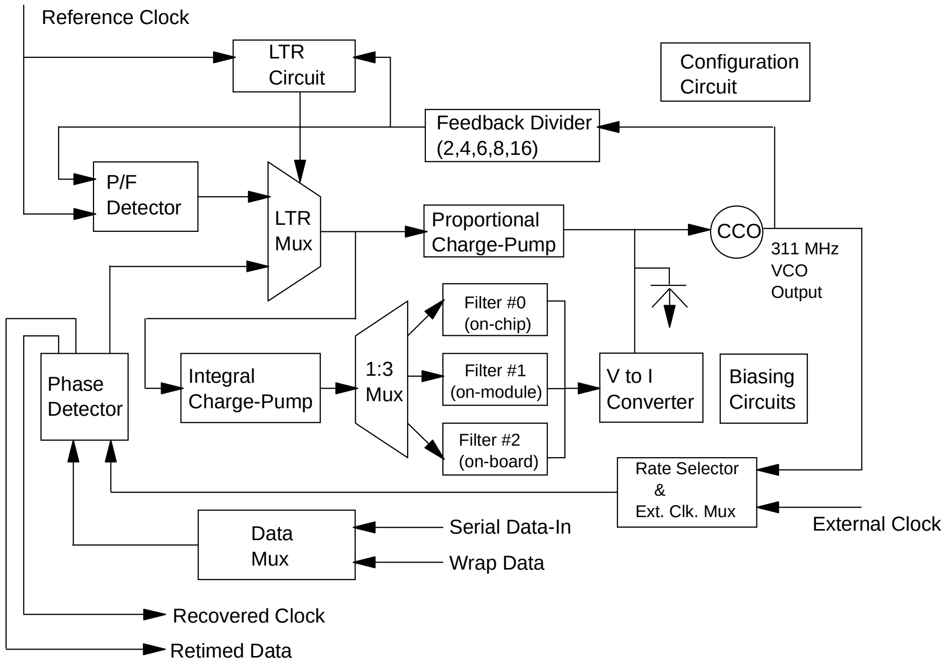

Fig. 3: Block diagram of RxPLLA

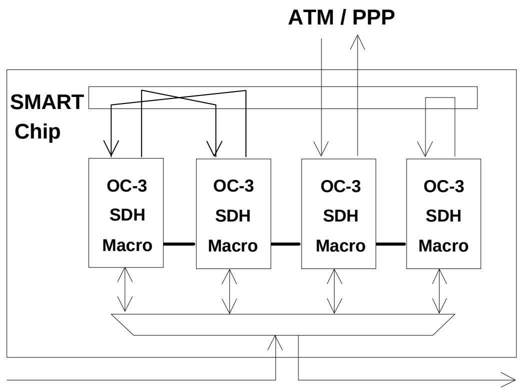

Fig. 4: Digital cross-connect and add/drop multiplexer functions

cross-connect, native SDH/SONET multiplexer and add/drop multiplexer functionality. Fig. 4 shows how the add/drop multiplexer and digital cross-connect functionality is achieved by mapping the output of the receive part of a SMART macro either onto the input of its own transmit part (through going traffic) or onto the transmit input of another macro (digital cross-connect), or connecting the macro to the Utopia or COMBUS interface (add/drop multiplexer). The OC-48 expansion ports allows coupling of four chips to handle OC-48 frames. In this case the port is used to ensure frame synchronization and provide the necessary information for calculating e.g. B1 and B2 overhead bytes to those chip which creates the overhead bytes for the OC-48 frame.

The challenges encountered when designing this complex and large chip are described elsewhere (7).

Measurement Results

The functional operation of the chip was byte processing, correct Utopia interface operation for ATM cells and PPP packets,tested with a large serious of tests which confirmed correct SDH/SONET framing and overhead correct operation of the COMBUS interface and all other units.

Fig. 5 shows a jitter-tolerance measurement with the unit-interval peak-to-peak value versus jitter-frequency according to the ITU-T G.825 standard. The lower limit for the UIPP value according to the ITU-T G.825 standard is shown as dashed line in the figure. The measurement is done with a 622 MB/s STM-4 signal and the input reference clock set to 77.76 MHz. On-chip as well as on-module filters are used for noise suppression. The chip fulfills the jitter tolerance requirement for the whole range of frequencies. Table 1 shows the results of corresponding jitter-generation measurements for STM-4 data for the five reference frequencies of the chip. Comparison with recommendation R5-207 of the BellCore standard and corresponding ITU-T and ANSI standards shows that the requirements for jitter-generation are fulfilled for all reference frequencies.

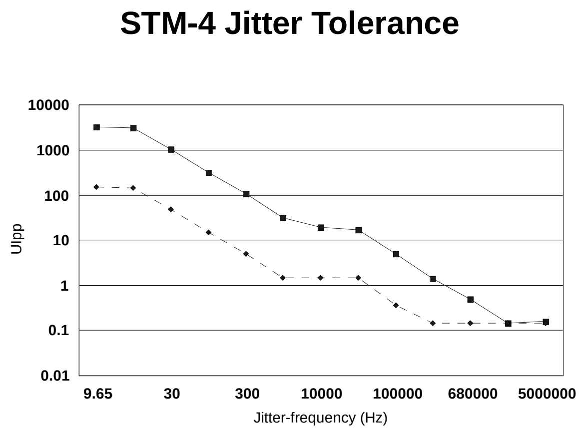

Fig. 5: Measured jitter-tolerance for 622.08 Mb/s

Table 1: Jitter generation for STM-4 with scrambled data

Filter [KHz][MHz]	fr=19.44 MHz [UIpp / rms]	fr=38.88 MHz [UIpp / rms]	fr=51.84 MHz [UIpp / rms]	fr=77.76 MHz [UIpp / rms]	fr=155.52 MHz [UIpp / rms]
LP 5.0	0.096 / 0.012	0.081 / 0.009	0.086 / 0.009	0.089 / 0.010	0.089 /0.010
1.0 5.0	0.094 / 0.011	0.079 / 0.009	0.083 / 0.009	0.087 / 0.010	0.085 / 0.010
250 5.0	0.069 / 0.007	0.065 / 0.007	0.068 / 0.007	0.069 / 0.007	0.068 / 0.007
12 HP	0.137 / 0.012	0.134 / 0.011	0.146 / 0.012	0.145 / 0.012	0.140 / 0.011

Technology Data

The chip is implemented in 0.36 μm, 3.3V CMOS technology (with implanted resistors for the analog part) with a die size of 10.8 x 10.8 mm and a 25 x 32 mm CBGA package with on-module capacitors for filter application. The chip contains 384 signal I/Os and uses 5 metallization layers. The digital part contains about 584000 standard cells and fills 80% of the die area. The power consumption is 2.4 W nominal in OC-12c mode and 4 W nominal in 4 x OC-3c mode.

Conclusion

We have presented a new chip which enables SDH/SONET framing for 4 x OC-3c, OC-12, and OC-12c with integrated clock recovery in an all CMOS implementation while fulfilling the stringent ITU-T, Bellcore and ANSI jitter requirements for such systems. Incorporated functions like digital cross-connect and add/drop multiplexing enable low cost digital cross-connect and add/drop multiplexing systems for 4 x OC-3c and OC-12. The APS support offers on-chip automatic protection switching for 4 x OC-3c. The OC-48 expansion port allows coupling of four chips to handle OC-48 frames in connection with an external serializer/deserializer and clock recovery chip for 2.4 Gb/s.

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