RZ 3257 (# 93303) 07/10/00
Engineering & Technology 4 pages

Research Report

Accurate De-Embedding of CMOS Transistors from On-Wafer Measurements up to 110 GHz using Automatically Characterized CMOS Calibration Structures

Martin L. Schmatz and Thomas Morf

IBM Research
Zurich Research Laboratory
8803 Rüschlikon
Switzerland

Accurate De-Embedding of CMOS Transistors from On-Wafer Measurements up to 110 GHz using Automatically Characterized CMOS Calibration Structures

Martin L. Schmatz and Thomas Morf

IBM Research, Zurich Research Laboratory, 8803 Rüschlikon, Switzerland

Abstract **-** This paper presents a de-embedding sequence for CMOS transistors that is very accurate from DC to frequencies above 110 GHz. In a first step, a combination of on-wafer TRL and LRM calibrations defines a 50Ω reference plane at a distance of less than 10μm away from the device under test (DUT). The calibration method is based on a compact set of on-wafer structures consisting of a thru connection (thru), a nominal short (reflect), a moderate length transmission line (line), and a nominal load (load). The equivalent electrical values of the above structures are automatically determined with high precision during the calibration process and have therefore not to be known prior to the calibration. This allows the method to be applied (but not limited) to CMOS processes tolerating their relatively large process variations and parasitics. It also makes additional off-wafer calibration kits dispensable. In a second iteration step, a de-embedding sequence that relies on the measured Y- and Z-parameters of an open- and a short-circuit is used to take the parasitic influence of the last few micrometers of wire connection between the reference plane and the transistor into account. The described method is utilized for the de-embedding of CMOS test transistors up to a frequency of 110 GHz. The transistors are manufactured on IBM's 0.11 μm Cu11 line and have a transit frequency in excess of 80 GHz, making advanced de-embedding techniques a necessity for the determination of the equivalent circuit elements including the internal noise sources.

Introduction

There are several methods known for the calibration of network analyzers in order to generate a reference plane with a 50Ω reference impedance at the probe-tips of an on-wafer measurement system [1,2,5,7]. However, because the pitch of the probe-tips (100 μm – 250 μm) is large in comparison to the size of typical deep sub-μ test transistors, additional on-wafer mounting structures have to be implemented for the connection of the small transistors to the probe pads [3]. In order to determine the equivalent circuit elements of a transistor, one-, two- or three-step de-embedding algorithms were used to characterize these mounting structures [4]. The problem is that the de-embedding algorithms are limited in their frequency range because they assume that the influence of parasitic series elements during the measurement of the open is negligible, which is only true at moderate frequencies where the geometry of the mounting structures is small compared to the wavelength. For advanced CMOS processes, this assumption results in errors at high frequencies, as is shown in Figure 1.

What would be needed is a calibration method that allows the connection of test transistors with mounting structures that are considerably smaller than the probe-tip pitch and even smaller than the size of a transistor. This would extend the frequency range of the two-step de-embedding algorithm to well above 110 GHz, something the authors have not found in CMOS related literature.

This paper describes such a calibration and de-embedding combination and would show some results for IBM's 0.11 μm Cu11 CMOS process in the conference version of this paper.

De-Embedding Technique

Figure 2 shows a flow chart for the proposed de-embedding technique: The propagation constant γ of an on-wafer low impedance microstrip line (Figure 3) is determined from the measurement of a zero length thru and a 600-μm long transmission line [5]. It is followed by a determination of the characteristic impedance Z_w of the 600-μm line and the complex, frequency dependent impedance Z_{Load} of an integrated resistor from the measurement of a large reflection caused by the nominal short calibration standard and from the measurement of the resistors DC and reflection values [2,6]. This step allows the use of the integrated resistor in the role of a fully characterized match calibration standard for an accurate LRM calibration, including a final transformation of the reference impedance to 50 Ω [7]. The reference plane of this calibration is at the center of the thru connection, visualized in Figure 4 together with the layout of the transistor and the mounting structures. Finally, the influence of the wire between reference plane and transistor is determined by the measurement of an open transmission line and a transmission line with the connection wire shorted after 10 μm. The well-known 'two-step algorithm' [4] is used for that purpose.

Measured results for IBM's 0.11 μm Cu11 CMOS process will be shown in the conference version.

Conclusions

A combined calibration and de-embedding method for CMOS transistor measurement is presented that is accurate from DC to frequencies above 110 GHz. It is based on a TRL/LRM on-wafer calibration followed by a de-embedding algorithm that relies on the measured Y- and Z-parameters of an open- and a short-circuit. Because all calibration structures are automatically determined during the calibration procedure, their characteristic values have not to be known prior to the calibration, which is compatible with CMOS process tolerances. It allows the user to have it's own 'home-made' calibration kit tailored to his needs, without the need to rely on commercial off-wafer standards.

The method is applied to the de-embedding of 0.11 μm CMOS transistors where it allows the accurate determination of the transistors equivalent circuit elements up to 110 GHz.

References

[1] D.F. Williams et al., "LRM probe-tip calibrations with imperfect resistors and lossy lines," 42nd ARFTG Conf. Digest., pp 32-36, Dec 1993

[2] G.F. Engen et al., "Thru-Reflect-Line: An improved technique for calibrating the dual six-port automatic network analyzer," IEEE Trans. MTT, Vol 27, No 12, pp. 897-993, December 1979

[3] A.Fraser et al., "GHz on-silicon wafer probing calibration methods," IEEE 1988 Bipolar Circuits & Technology Meeting, pp 154- 157, 1988

[4] M.C. Koolen et al., "An improved de-embedding technique for on-wafer high frequency characterization," IEEE 1991 Bipolar Circuits & Technology Meeting, pp 188-191, 1991

[5] R.B. Marks, "A multiline method of network analyzer calibration," IEEE Trans. MTT, Vol 39, pp. 1205-1215, July 1991

[6] D.F. Williams et al., "Transmission line capacitance measurement," IEEE Microwave and Guided Wave Letters, Vol. 1, No. 9, Sept 1991, pp 243-245

[7] H.J. Eul et al., "Thru-Match-Reflect: One result of a rigorous theory for de-embedding and network analyzer calibration," Proc. 18th European Microwave Conference, pp 909-914, September 1988

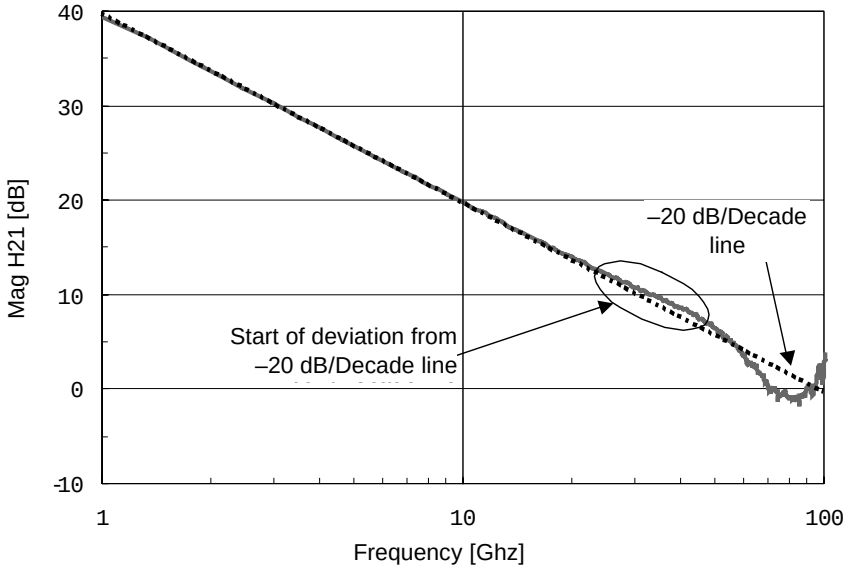


Fig. 1. Visualizing the problems of prior art: Magnitude of the H21-parameter of a 0.11µm NMOS transistor vs. frequency; measured from 1 GHz to 100 GHz and de-embedded based on a conventional off-wafer calibration and a two step de-embedding [4] from a measured open and short; please note the deviation from the -20dB per decade line above 30 GHz due to the inaccuracies of the de-embedding.

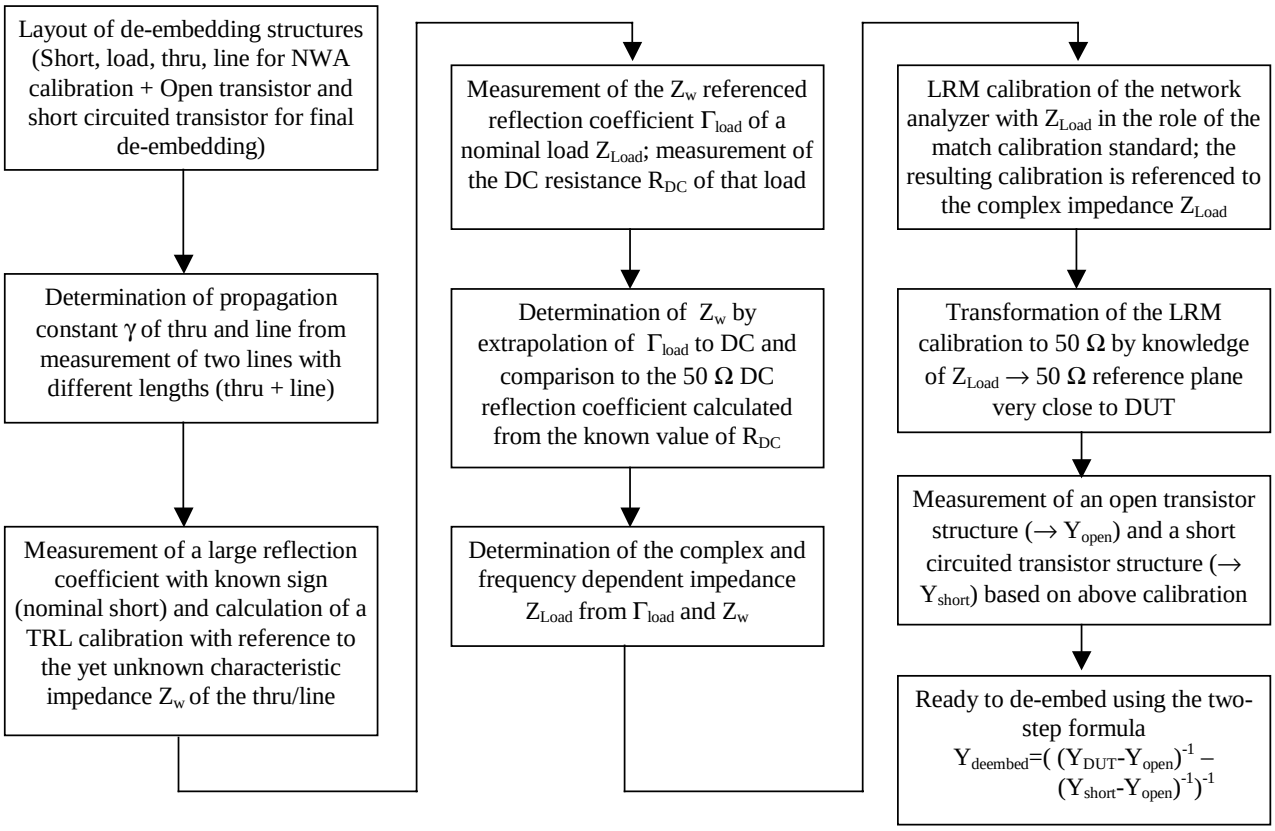
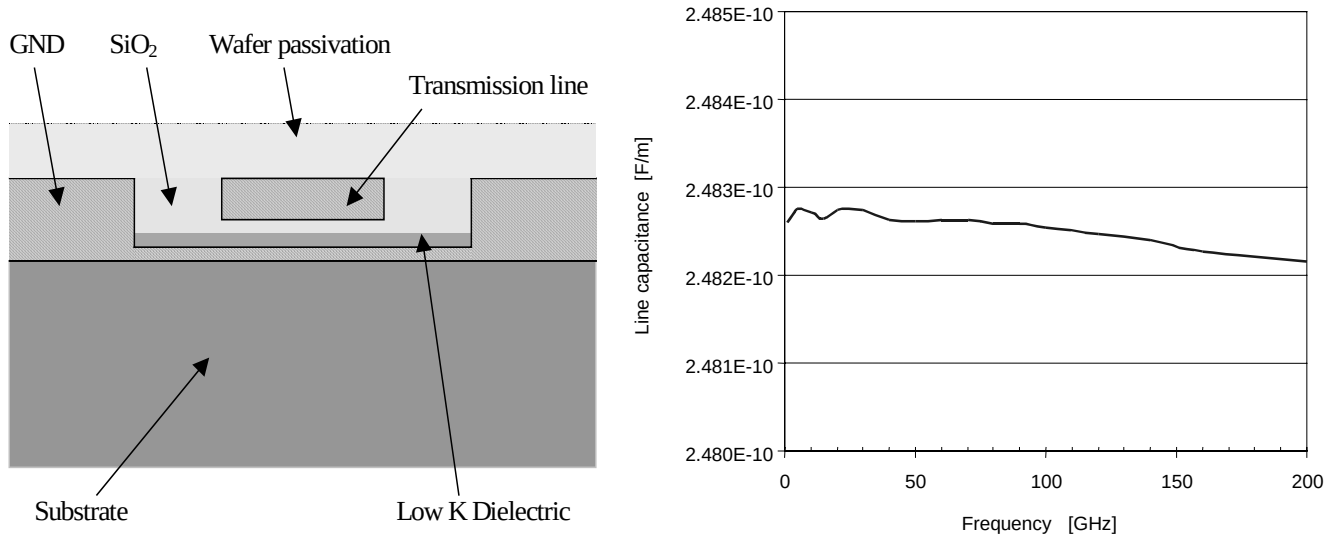


Fig. 2. Flow chart of the proposed calibration and de-embedding sequence



(a) (b)

Fig. 3. (a) Cross section of the transmission line used as calibration line (approx to scale); the transmission line is implemented in the form of a grounded coplanar line with 10μm width, resulting in ~25Ω characteristic impedance at 50 GHz; the low impedance makes sure that the field is concentrated under the line from low to very high frequencies so that the approximation in [6] gamma/Zw/j/omega = C' holds. (b) Simulated line capacitance vs. frequency of the proposed transmission line from electromagnetic field simulations (Agilent HFSS); please note that the normalized change between 1 GHz and 200 GHz is less than 10^{-5}.

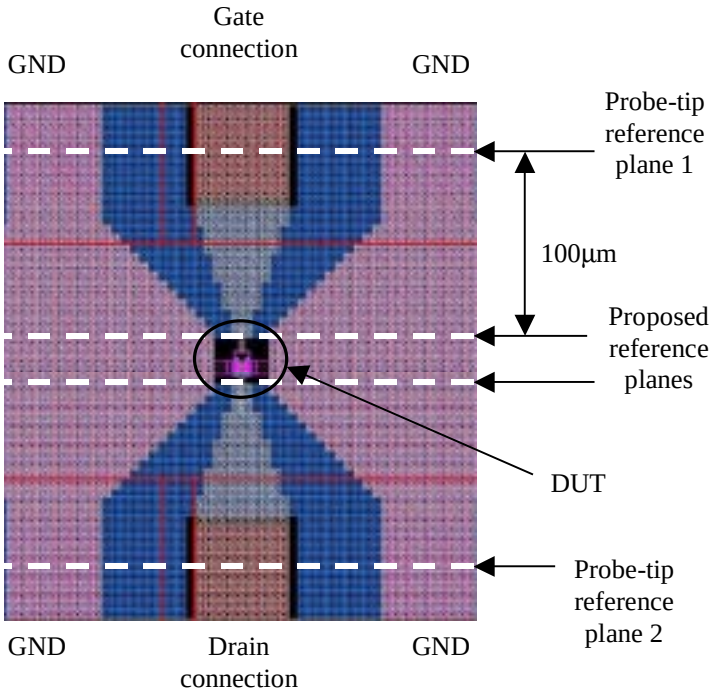


Fig. 4. Layout of a test transistor; As may be seen, the reference plane is shifted by 100 µm from the probe-tip position to the proposed reference plane position. The distance from this new reference plane to the DUT is less than 10 µm (as compared to the more than 100 µm for prior art).