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Research Report

High-Density 3D Interconnect: Merging VLSI-CMOS and VLSI-MEMS Technologies

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Abstract

We have developed robust, wafer-scale, 3D interconnect methods for batch fabrication of System on Chip (SOC) especially suitable for MEMS or VLSI-MEMS applications, and show the robustness of these new transfer methods. This is a major step toward a high-integration SOC system and opens new opportunities for VLSI-MEMS and its integration with microelectronics. It has significant potential for many applications such as heterogeneous device integration (mixed technology), 3D integration and chip stacking. Using the third dimension also has the potential to simplify device architecture and reduce the length and complexity of interconnects.

High-Density 3D Interconnect:
Merging VLSI-CMOS and VLSI-MEMS Technologies

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We have developed robust, wafer-scale, 3D interconnect methods for batch fabrication of System on Chip (SOC) especially suitable for MEMS or VLSI-MEMS applications. This work is part of the development of a highly parallel data storage system based on a scanning probe array called the "Millipede" [1] and aims to interconnect the Millipede cantilevers vertically with their driving electronics fabricated on a separate CMOS electronic circuit. Very high integration density has been achieved even for wafer-scale joining (MEMS and CMOS wafers) thanks to the interlocking nature of the interconnect structure, which provides easy alignment with an accuracy better than 2 μm. Typical integration density achieved is 100 cantilevers/mm^2 and up to 1000 electrical interconnects/mm^2. It is important to note that our method preserves the device orientation. This is crucial for MEMS applications where the MEMS device typically should have access to its environment (e.g. in this specific case, the cantilever tips are in contact with the storage media). Once the CMOS-MEMS joining has been performed, the system is mechanically and electrically stable up to at least 400°C, allowing post-transfer wafer processing. Two technologies have been developed; one is based on through via interconnects [2] and the other on a new approach we call microdevice transfer [3]. The structure of these two types of interconnects is shown in figure 1. In both cases we have obtained very high process reliability with yields of the order of 99.9%.

For MEMS-CMOS joining, both methods use a novel interconnect type consisting of an interlocking polyimide via and metal stud structures [4]. In the case of the through via interconnect the metal stud makes contact on the backside of the MEMS wafer, which has been thinned down to a couple of tens of micrometers. For the microdevice transfer method, the complete wafer is ground and etched away. Only the device itself (in the present case the cantilever) is transferred and the metal studs contact the device directly (on the cantilever anchors). To allow the transfer of such a fragile and flexible structure, the MEMS wafer is bonded to a glass wafer via a polymer layer before being thinned down. Once the silicon membrane or the devices have been transferred to the CMOS wafer, the glass is debonded using laser ablation. Key process steps will be presented such as lamination on glass wafer, through via processing including electroless metal via filling, seed MEMS wafer thinning, MEMS backside processing, post-CMOS processing consisting of metal/solder stud plating, assembling using the stud/polyimide structure for simple and high-accuracy alignment followed by the lamination process providing the mechanical and electrical bonding, the glass debonding process using laser ablation of polyimide at the glass/polyimide interface, and finally cantilever release and cleaning. For a robust transfer process, the relative softness at lamination temperature (~380°C) of the polyimide and the metal/solder stud are the key elements that make it independent of wafer surface topography and cleanness. Figure 2 shows a detailed view of the through via and the polyimide/metal structure in a cleaved wafer used for evaluating the reliability of such interconnect methods. Figure 3 shows the glass carrier wafer after bonding and seed wafer removing; each square contains an array of 4096 cantilevers, each having three interconnect pads (see inset). Figure 4 shows a section of the transferred cantilever array on a wiring wafer as well as a close-up side view where the free-standing cantilever angle control can be seen. We obtained very high yield in terms of mechanical structure integrity after the transfer and in terms of electrical contact (on the order of 99.9%) even with such a delicate structure. The cantilever is typically 70 μm long and 300 nm thick and its tip has sub-20-nanometer radius. We obtained a cantilever angle control of better than 0.1°; no tip degradation was observed even at the

nanometer scale. The electrical contact resistance is well below 1 Ω. The advantages of the two methods will be compared and their potential respective applications will be discussed.

We have shown the robustness of these new transfer methods. This is a major step toward a high-integration SOC system and opens new opportunities for VLSI-MEMS and its integration with microelectronics. It has significant potential for many applications such as heterogeneous device integration (mixed technology), 3D integration and chip stacking [2]. Using the third dimension also has the potential to simplify device architecture and reduce the length and complexity of interconnects.

[1] P. Vettiger et al., IEEE Trans. Nanotechnology 1(1), 2002, 39-55.
[2] H. B. Pogge,et al., abstract submitted to 2003 Symposia on VLSI Technology and Circuits, Kyoto, Japan, June 10-14, 2003.
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[4] H. B. Pogge et al., Advanced Metallization Conf. 2001 (AMC 2001), pp. 129-136 (2001); H. B. Pogge et al., 3rd Int'l Conf. on Microelectronics and Interfaces, Santa Clara, CA, 2002.

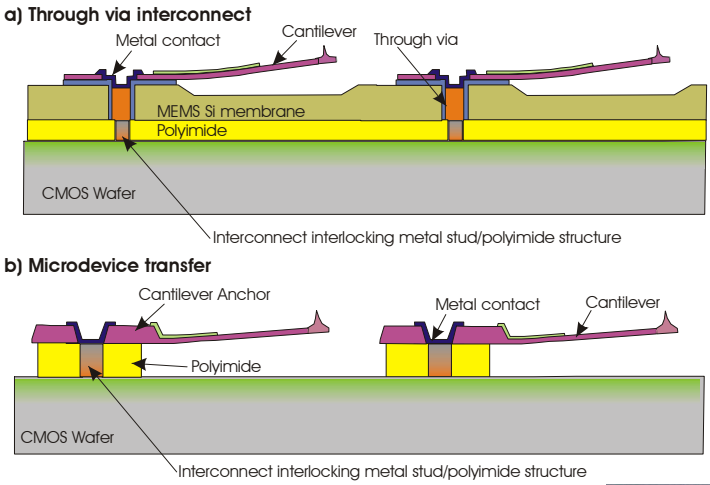

Figure 1: CMOS/MEMS 3D interconnect structures.
(a) Based on through via. The MEMS wafer has been thinned down to a couple of tens of micrometers.
(b) based on microdevice transfer. The metal interconnect stud contacts the device (cantilever) directly.

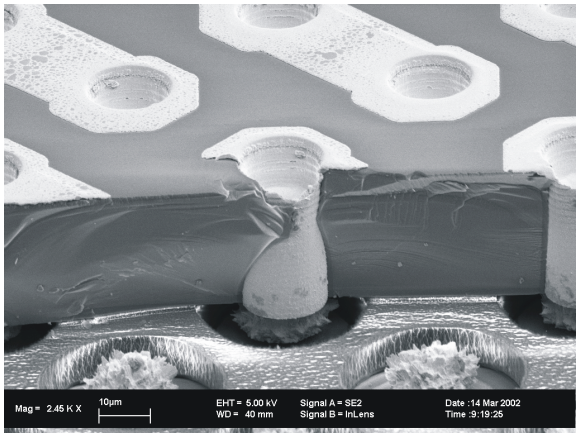

Figure 2: SEM of a cleaved sample showing the through via and polyimide/metal interconnect structure as well as metal wiring connecting vias.

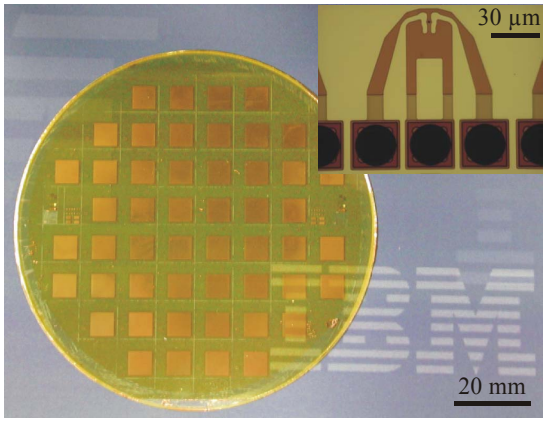

Figure 3: Glass wafer after the cantilever's arrays have been transferred and the seed wafer removed. Each square contains 4096 cantilevers. Owing to its thinness, the structure is transparent. The inset shows the cantilever structure bonded to the glass wafer.

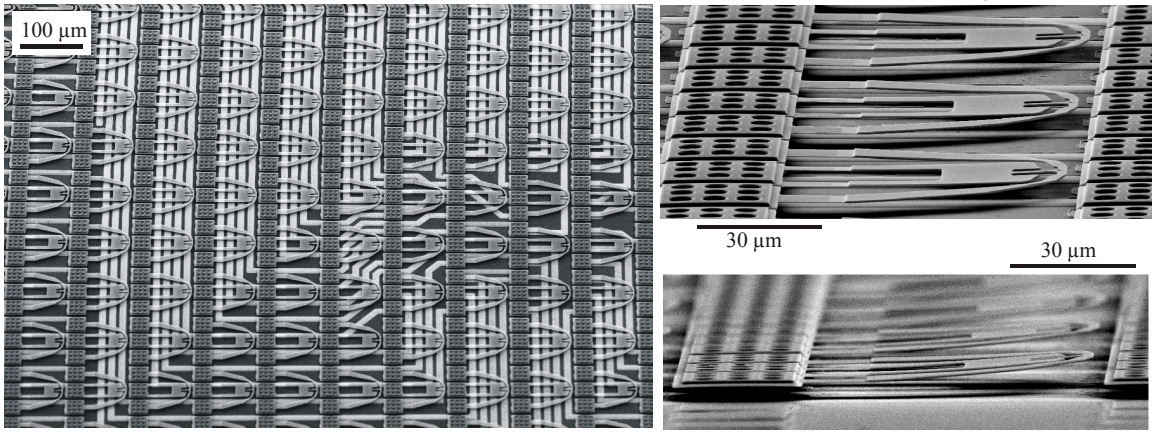

Figure 4: SEM of a section of the cantilever array transferred on a wiring wafer and side view of the transferred free-standing cantilever. High controllability of the cantilever bending is achieved and has been tuned to 3.5 µm.