RZ 3532 (# 99545) 01/19/04
Electrical Engineering 4 pages

Research Report

A C-Band Monolithic Silicon-Bipolar Low-Power Low-IF WLAN Receiver

Corrado Carta*, Martin Schmatz**, Rolf Vogt* and Werner Bächtold*

*Electromagnetic Fields and Microwave Electronics Laboratory (IFH)
Swiss Federal Institute of Technology (ETH)
8093 Zurich
Switzerland
carta@ifh.ee.ethz.ch

**IBM Research GmbH
Zurich Research Laboratory
8803 Rüschlikon
Switzerland

A C-Band Monolithic Silicon-Bipolar Low-Power Low-IF WLAN Receiver

Corrado Carta*, Martin Schmatz**, Rolf Vogt* and Werner Bächtold*

* Electromagnetic Fields and Microwave Electronics Laboratory (IFH), Swiss Federal Institute of Technology (ETH), Zurich, Switzerland
email: carta@ifh.ee.ethz.ch

** IBM Research Laboratory, Rüschlikon, Zurich, Switzeralnd

***Abstract*— This paper presents the design, implementation and measurements of a monolithic low-IF receiver compliant with the main 5 GHz WLAN standards. It consist of a low-noise preamplifier that is simultaneously noise and power matched to the RF source, two matched active single-balanced mixers and two polyphase filters used to generate LO quadrature signals and provide image rejection. Realized in a 47 GHz-f$_t$ commercial BiCMOS technology the circuit exhibits 25 dB of conversion gain, 35 dB of IRR, 8.9 dB of NF, -12.5 dBm and -19 dBm of iIP$_3$ and P$_{1\ dB}$ respectively. To the knowledge of the authors this is the first monolithic implementation of a low-IF C-band receiver achieving sufficient IRR over the three U-NII bands. Power consumption is 19 mW.**

***Index Terms* — Low-IF receiver, BiCMOS, WLAN, IEEE802.11a, HiPerLAN2, Image rejecting mixer**

I. Introduction

In the unlicenced 5 GHz-band there are two competing standards, ETSI HiPerLAN2 [1] and IEEE802.11a [2], and a newer, IEEE802.11h [3], is currently under definition and will use almost the full 5.15-5.825 GHz spectrum. The physical layers make use of the three Unlicensed National Information Infrastructure (U-NII) bands, i.e. two lower bands between 5.15 GHz and 5.35 GHz, and a third band from 5.725 GHz to 5.825 GHz, each 100 MHz wide. The remaining requirements for the RF front-end are similar and a set of properly tightened specifications allows to define a receiver compliant with all those standards.

Due to the 400 MHz gap, most of the previously published works targeted either the two lower bands [4]–[9] or the upper one [10], [11]. The presented receiver covers all the three bands: this is further motivated by the features of the currently under definition IEEE802.11h standard, that will use an extra 5.47-5.725 GHz band, covering almost the full 5.15-5.825 GHz spectrum.

Table I resumes the receiver RF specifications: conversion gain and P$_{1\ dB}$ are result of design choices [8], while the other figures of merit are either explicit in the standard or result of simple elaborations.

Commercial interest justifies the need to keep production cost, physical size and power consumption of such a receiver at a minimum: the low-power single-chip integration on a low-cost silicon-based technology is the apparent solution.

For this work an RF oriented 47 GHz-f$_t$ BiCMOS technology was used: available SiGe HBTs are particularly suitable for low-power applications, due to their high g_m/I ratio, and a few modified features of the process simplify the integration of inductors, while keeping the cost low.

The circuit was designed to fulfill the specifications making use of no external component and minimizing the DC power consumption.

II. System Architecture

The need of high integration reduces the choices for the receiver architecture to low-IF and Direct Conversion (DiCon). In fact the use of DiCon architectures is eased in both IEEE802.11a and HiPerLAN2 by the absence of signal power at the channel center frequency.

The main issue in low-IF receivers is the demanding specification for I-Q signal balance in the RF paths: the image rejection depends on this symmetry. At lower frequencies, implementations without possibility of external tuning achieve image rejection ratios (IRR) in the order of 30-40 dB [12].

The DiCon receiver also needs good I-Q balance, although it can be shown that the requirements are more relaxed [13]. It is, however, affected by a number of other issues, such as 1/f noise of the IF blocks, and susceptibility to second

TABLE I
Receiver RF Specifications

Parameter	Specification	Notes
RF band	5.15-5.825 GHz	Explicit in standard
IRR	32 dB	Alternate ch. rejection
Conv. Gain	25-30 dB	Design choice
NF	10 dB	Explicit in standard
P$_{1\ dB}$	-21 dBm	Design choice
iIP$_3$	-14.5 dBm	Adiacent ch. rejection
In-band emission	$<$-47 dBm	International laws

order distortions. In particular the need for low second order intermodulation leads to the common choice of differential architectures, which increase the DC power consumption.
For this system the low-IF architecture was chosen: a sufficient I-Q balance can be achieved with a careful circuit layout, and the relaxed requirement for the second order distortion allow to avoid differential topologies. Fig. 1 shows the system building blocks. Quadrature LO signals are generated on chip by a two-pole polyphase filter; image rejection at IF is achieved by means of a second poly-phase filter over the IF band from 30 to 50 MHz.
An IF buffer is integrated to simplify circuit characterization in a 50 Ω environment; in a practical application the polyphase filter would be able to drive directly a high-input-impedance channel filter and no IF buffer would be required.

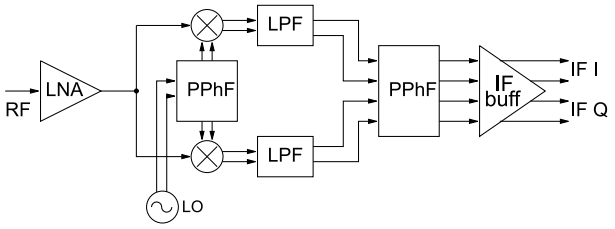

Fig. 1. Block diagram of the implemented system architecture.

III. Circuit Design

A. LNA

The LNA is implemented with a single-ended HBT cascode. The cascode gain cell was chosen due to its better output-to-input isolation and higher output impedance, which makes possible higher gain for a power consumption similar to the single stage counterpart.
Fig. 2 shows the schematic of the amplifier: input noise-and-power matching to 50 Ω is achieved by means of two on-chip inductors and proper choice of T_1 size and biasing [14], while output power matching is realized by L_3 and C. Resistor R is used to lower the high quality factor of the output resonator, in order to achieve the needed bandwidth of 1 GHz. The input impedance was set to properly terminate an external antenna filter, while the output impedance was set to a value convenient to drive the following mixers.
The circuit was designed to provide about 14 dB of power gain, a NF of 2.6 dB, with a current consumption of 2 mA from a 2 V supply.

B. Mixer

The topology chosen for the mixers is the active single-balanced, as shown in Fig. 3. The single-ended topology was preferred over the differential [15] because it provides the same conversion gain for half the current consumption. The main drawback is the lack of isolation from the LO port to the IF: the large LO signal could saturate the following stage, but can be easily filtered by means of non-critical capacitors,

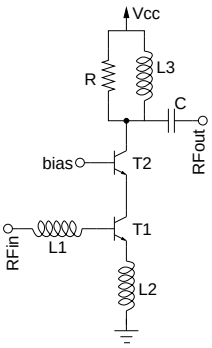

Fig. 2. Schematic of the Low Noise Amplifier.

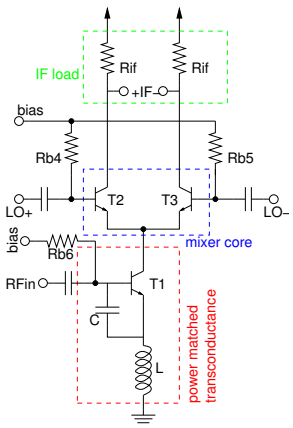

Fig. 3. Schematic of the single-balanced active mixer.

shown in Fig. 1 as low-pass filter.
The mixer core consists of a pair of matched HBTs, whose bias current determines the dynamic range of the whole mixer. In fact, for very low-power implementations, the transistors T_2 and T_3 limit the linearity of this circuit well before T_1. Transistor T_1 has to be inductively degenerated in order to reduce its transconductance and not to overdrive the mixer core. This does not necessarily imply a reduction of voltage gain, because low signal and bias currents allow the use of larger IF load impedances, thus increasing the voltage conversion gain.
As a consequence of the degeneration, the real part of the RF input impedance falls in the range of few hundreds of Ohms; under this condition, the capacitor C is sufficient to provide power matching from the LNA output to the mixer input.
The circuit was designed to provide 14 dB of voltage conversion gain, $P_{1\,dB}$ of -4 dB, with a current consumption of 2.5 mA from a 3 V supply.

C. Polyphase Filters

Both IF and LO polyphase filters were designed using a standard approach, with a cascade of two stages.
For the IF filter, two stages are necessary to achieve sufficient IRR over the 20 MHz of IF bandwidth. In order to reduce signal voltage loss, the resistances increase toward the output [16]: from the mixer output impedance to the IF buffer input each stage drives a higher impedance.
The two stages of the LO filter are identical in order to ensure amplitude and phase balance of the quadrature signals over the 1 GHz LO tuning band.

IV. Experimental Results

A. Fabrication

The circuit was fabricated with the commercial IBM BiCMOS 6HP process [17]. At optimum bias current, the HBTs yield transit frequencies f_t up to 47 GHz and minimum

noise figures NF_{min} of around 1.2 dB at 5 GHz. The process is targeted for RF, analog and mixed signal applications, having a 4 µm thick Analog Metal and a maximum dielectric stack of 10.1 µm for low-loss interconnect. This, together with the deep-trench insulations and patterned poly-silicon shields, allows the implementation of inductors with quality factors up to 19 at 5 GHz.

The circuit has been implemented on a 1.05 mm^2 active area, including the IF output buffer, as shown in the photograph in Fig. 4. Total area shown measures 2.14 mm $\times$ 1.32 mm.

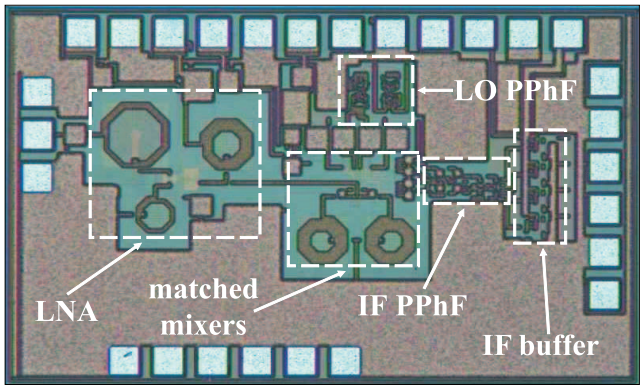

Fig. 4. Chip microphotograph of the low-IF receiver.

B. Measurements

For characterization the chip was mounted on a microstrip test board. The LO differential signal has been generated by means of a 180° microwave hybrid, IF differential output was converted to single ended using a power combiner. The presented results have been processed in order to de-embed the receiver performances from the effect of the chip test environment and the integrated IF buffer, which was characterized independently.

Table II summarizes the measured performance of the prototype over the three U-NII bands; DC power consumption is 19 mW, and LO power is set to 2 dBm.

Fig. 5 shows the measurement results of conversion gain, IRR and NF of the down-converted intermediate band. Fig. 6 shows an iIP_3 extrapolation for the same band.

TABLE II
SUMMARY OF MEASURED RESULTS

U-NII band	[GHz]	$5.15-5.25$	$5.25-5.35$	$5.725-5.875$
Conv. Gain	[dB]	25	25	22.5
IRR	[dB]	33	35	36.5
NF	[dB]	8.2	8.9	10.2
$P_{1\,dB}$	[dBm]	-19.1	-19	-18
iIP_3	[dBm]	-12.2	-12.5	-11.25
S_{11}	[dB]	< -9	< -10	< -14
LO to RF	[dB]	-64	-62	-57

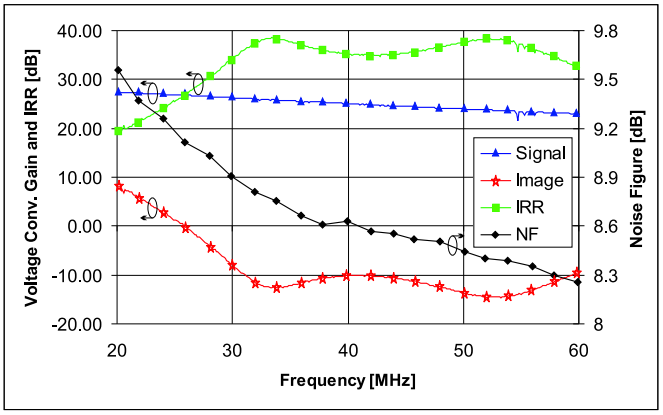

Fig. 5. Image Rejection Ratio of the down-converted middle band, and corresponding Noise Figure.

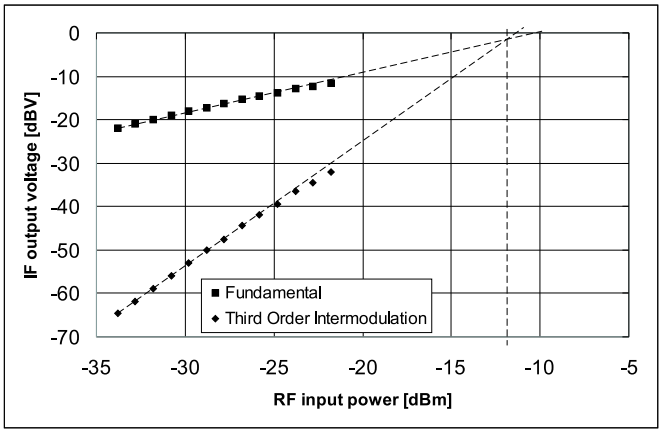

Fig. 6. iIP_3 extrapolation of the down-converted middle band.

Conversion gain, linearity, IRR and LO-to-RF isolation satisfy the given specifications.

The value of S_{11} in the lower band is higher than expected, but still acceptable.

The NF is about 4 dB higher with respect to simulations; in particular, in the upper band, NF is 0.2 dB higher than specified for IEEE802.11a. This value still falls within the 5 dB implementation margin given by the standard definition [2].

V. Conclusions

The design, implementation and characterization of a C-band low-IF receiver has been presented. The measured results meet the specifications for the main two released C-band standards and for a new one currently under definition, with the exception of the NF in the upper U-NII band, which is higher than requested, but still within an allowed implementation margin.

Table III compares this work with the main C-band receivers published: to the best knowledge of the authors, this is the

TABLE III

SILICON C-BAND RECEIVER STATE OF THE ART

Process	Architecture	Bands	Gain [dB]	NF [dB]	iIP_3 [dBm]	Current/Voltage	IRR [dB]	Year	Ref.
Si Bipolar 25 GHz	Low-IF (75 MHz)	1-2-3	17	5.1	-4.5	23 mA/2.2 V (LO and quad)	Off chip	2000	[18]
BiCMOS 22 GHz	Superhet., two external filters	1-2	18	7 (DSB)	-17	18 mA/3 V	—	2000	[4]
CMOS 0.25 µm	DiCon (but IF @ 10 MHz)	1-2	18	3 (DSB)	-11.3	38 mA/3 V (LO and quad)	—	2000	[5]
Si Bipolar 47 GHz	Superhet. with external filter	1-2-3	14	6.9	-5.8	10 mA/1.8 V (LO and buff.)	36	2000	[19]
CMOS 0.24 µm	Low-IF or Di-Con	2	12	5.2 (∼DSB)	-2	3.6 mA/2.5 V(?) (passive mix.)	12	2000	[6]
CMOS 0.25 µm	2×Superhet. (no ext. filters)	1-2	43	6.4	-15	11.6 mA/2.5 V	62	2001	[7]
CMOS 0.25 µm	Low-IF (Weaver)	1-2	26	7.2	-18	32.7 mA/1.8 V (LO and quad.)	50	2002	[8]
Si Bipolar 46 GHz	Superhet. several ext. comp.	∼1	24	3.2	-13	18 mA/3 V (LO and quad.)	35	2003	[9]
BiCMOS 45 GHz	DiCon	3	26.5	5.2	-17.4	23 mA/2.7 V	—	2003	[10]
BiCMOS6HP 47 GHz	DiCon	3	20.2	7.1 (DSB)	-3	31.2 mA/3.75 V	—	2003	[11]
BiCMOS6HP 47 GHz	Low-IF	1-2(-3)	25 (22.5)	8.9 (10.2)	-12	7 mA/3 V	33	—	This work

first low-IF implementation reported achieving sufficient IRR values over all the three U-NII bands making use of no external components. In the comparison of the power consumption it has to be taken into account that many works include an on chip LO generation: the current consumption of a local oscillator and a buffer suitable for this chip is estimated to about 10 mA.

ACKNOWLEDGEMENT

This work was funded by IBM/ETH Center for Advanced Silicon Electronics (CASE).

The authors wish to thank H.-R. Benedikter and M. Lanz (both with IFH-ETH) for their valuable help in characterizing the circuit and preparing the test boards; F. Ellinger (with IfE-ETH) for his excellent suggestions on RF grounding.

REFERENCES

[1] "Broadband Radio Access Networks (BRAN); HIPERLAN type 2; Physical (PHY) layer," ETSI standard, 2001.

[2] "Information technology- telecommunication and information exchange between systems- local and metropolitan area networks- specific requirements part 11: wireless lan medium access control (mac) and physical layer (PHY) specifications amendment 1: high-speed physical layer in the 5 GHz band," IEEE standard, pp. i–83, 2000, 00887490.pdf.

[3] "IEEE Std. 802.11h - 2003," pp. 1–59, 2003, 01243739.pdf.

[4] M. Madihian, T. Drenski, L. Desclos, H. Yoshida, H. Hirabayashi, and T. Yamazaki, "A 5-GHz-band multifunctional BiCMOS transceiver chip for GMSK modulation wireless systems," *Solid-State Circuits, IEEE Journal of*, vol. 34, no. 1, pp. 25–32, 1999, 00736653.pdf.

[5] T.-P. Liu and E. Westerwick, "5-GHz CMOS radio transceiver front-end chipset," *Solid-State Circuits, IEEE Journal of*, vol. 35, no. 12, pp. 1927–1933, 2000, 00890306.pdf.

[6] H. Samavati, H. Rategh, and T. Lee, "A 5-GHz CMOS wireless LAN receiver fornt end," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 5, pp. 765–72, 2000, 00841505.pdf.

[7] B. Razavi, "A 5.2-GHz CMOS receiver with 62-dB image rejection," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 5, pp. 810–815, 2001, 00918919.pdf.

[8] T. Lee, H. Samavati, and H. Rategh, "5-GHz CMOS wireless LANs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 268–80, 2002, 00981280.pdf.

[9] A. Italia, E. Ragonese, G. Girlando, and G. Palmisano, "A 5-GHz monolithic silicon bipolar down-converter with a 3.2-dB noise figure," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2003 IEEE*, 2003, pp. 453–456, 01213983.pdf.

[10] M. Hotti, J. Kaukovuori, J. Ryynanen, K. Kivekas, J. Jussila, and K. Halonen, "A direct conversion RF front-end for 2-GHz WCDMA and 5.8-GHz WLAN applications," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2003 IEEE*, 2003, pp. 45–48, 01213890.pdf.

[11] S. Chakraborty, S. Reynolds, H. Ainspan, and J. Laskar, "Development of 5.8GHz SiGe BiCMOS direct conversion receivers," in *Microwave Symposium Digest, 2003 IEEE MTT-S International*, vol. 3, 2003, pp. 1551–1554 vol.3, 01210432.pdf.

[12] F. Behbahani, J. Leete, Y. Kishigami, A. Roithmeier, K. Hoshino, and A. Abidi, "A 2.4-GHz low-IF receiver for wideband WLAN in 0.6-um CMOS-architecture and front-end," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 12, pp. 1908–16, 2000, 00890304.pdf.

[13] B. Razavi, "Design considerations for direct-conversion receivers," *IEEE Transactions on Circuits and Systems*, vol. 44, no. 6, pp. 428–35, 1997, 00592569.pdf.

[14] D. Shaeffer and T. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," *IEEE Journal of Solid State Circuits*, vol. 32, no. 5, pp. 745–59, 1997, 00568846.pdf.

[15] B. Gilbert, "The MICROMIXER: a highly linear variant of the gilbert mixer using a bisymmetric class-AB input stage," pp. 1412–1423, 1997, 00628753.pdf.

[16] F. Behbahani, Y. Kishigami, J. Leete, and A. Abidi, "Cmos mixers and polyphase filters for large image rejection," *Solid-State Circuits, IEEE Journal of*, vol. 36, no. 6, pp. 873–887, 2001, 00924850.pdf.

[17] J. Dunn, "Foundation of RF CMOS and SiGe BiCMOS technologies," *IBM Journal of Research and Development*, vol. 47, no. 2/3, pp. 101–138, 2003, dunn.pdf.

[18] J. Maligeorgos and J. Long, "A low-voltage 5.1-5.8-GHz image-reject receiver with wide dynamic range," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 12, pp. 1917–26, 2000, 00890305.pdf.

[19] J. Long, "A low-voltage 5.1-5.8-GHz image-reject downconverter RF IC," *Solid-State Circuits, IEEE Journal of*, vol. 35, no. 9, pp. 1320–1328, 2000, 00868043.pdf.