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Research Report

A Multiphase PLL for 10 Gb/s Links in SOI CMOS Technology

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***Abstract* — This paper presents a multiphase PLL designed for a 10×10 Gb/s serial link bundle that is based on a digital CDR receiver. The PLL was fabricated in a 90-nm SOI CMOS process and covers a frequency band of 9.6–12.8 GHz at a supply voltage of 1.7 V. Measurement results showed a peak-to-peak jitter of less than 0.12 UI and a power consumption efficiency of 1.5 mW/GHz per link. An analytical derivation of the PLL's tuning range and the dimensioning of the phase buffer's shunt peaking coil to boost the bandwidth are also included in this paper.**

***Index Terms* — CMOS analog integrated circuits, high-speed integrated circuits, phase jitter, phase-locked loops, voltage controlled oscillators.**

I. Introduction

In high-speed data communication, one technique for high-performance clock and data recovery (CDR) is to use multiphase clock signals to sample the incoming data. This paper describes the design of a multiphase phase-locked loop (PLL) circuit used as clock source in a digital CDR receiver of a serial link [1]. The link architecture specifies that the multiphase PLL be shared by ten CDR receivers. A phase buffer network for the distribution of the sampling phases is therefore also included in the PLL design. Serial link applications at a speed of 10 Gb/s have been targeted by this design. To accommodate a potential coding overhead (e.g. 25% when using a 8b10b line code) a tuning range of 9.6–12.8 GHz was specified. The PLL was fabricated in a 90-nm, partially depleted silicon-on-insulator (SOI) CMOS process [2].

II. Circuit Architecture

A block diagram of the multiphase PLL is shown in Fig. 1. The oscillator in the PLL produces six phases with a spacing of 60º. The phase buffers are grouped into a tree-like topology for each differential phase pair and are specified to drive ten phase rotators used in the digital CDR receivers, each having 40 fF input capacitance per phase. Shunt peaking is used for the buffers of the two-stage tree, whereas the buffer between oscillator and actual buffer tree is of current mode logic (CML)-type only and shows no additional bandwidth-enhancement technique. The same buffer is also used at the input of the 1/16-circuit (div-16) that divides the signal of a differential phase pair and outputs a CMOS-level signal. This signal is then compared to a reference signal (f_{ref}) in a phase-frequency detector (PFD) circuit producing up and down signals for the charge pump, which is connected to a third-order loop filter. The filter's output voltage is finally converted to the tuning voltage range of the oscillator by a level control circuit, which closes the loop.

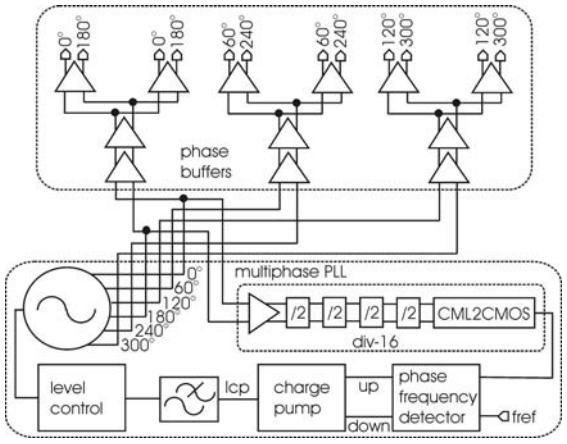


Fig.1. High-level schematic of the multiphase PLL including phase buffers used to operate 2×5 CDR receivers in a 10-Gb/s link macro.

In the following, each building block is discussed in more detail. A block diagram of the ring oscillator producing the different phases is shown in Fig. 2a. It consists of three CML-type delay cells whose schematic is depicted in Fig. 2b. The frequency of oscillation is current-controlled by PMOS load transistors. The transistor pair (*M1a*, *M1b*) is operated into the saturation region and its current I_0 determines the lowest frequency of oscillation. *M2a* and *M2b* are operated into the triode region and their current I_{P2}controls the tuning range of the PLL. The transistor pair (*M3a*, *M3b*) clamps the oscillation signal towards the supply voltage. Figure 2c shows the schematic of the level control circuit. It consists of a simple differential PMOS pair with source

degeneration resistors to increase the linear region and thus to decrease the oscillator gain.

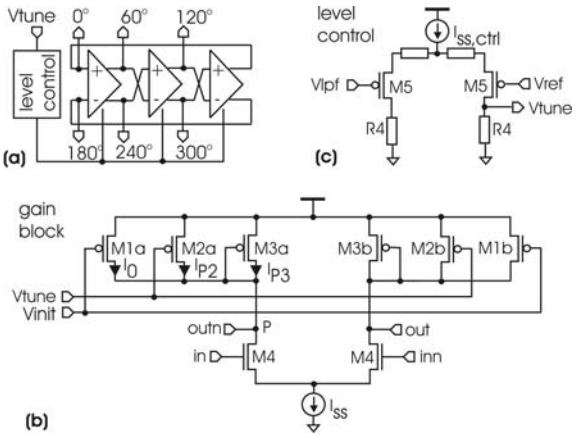


Fig. 2. (a) Ring oscillator consisting of a level control circuit and three delay cells; (b) delay cell; (c) level control circuit.

The tuning range and the gain of the oscillator can be estimated as follows. The oscillator frequency is given by

$$f_{osc} = \frac{1}{2N \cdot \tau} = \frac{1}{2N \cdot R_L \cdot C_L}, \qquad (1)$$

where τ is the delay per delay cell. To a first approximation it is assumed that the load capacitance C_L is dominated by the input capacitance of the differential NMOS pair of the next delay cell and can be written for *M4* operated in the saturation region as

$$C_L \approx \frac{2}{3} W_{M4} \cdot L_{M4} \cdot C_{ox} \ . \qquad (2)$$

The tuning range is thus primarily determined by the variation of the load resistance R_L and can be expressed as

$$tuning\ range = \frac{1}{2N \cdot C_L} \cdot \left(\frac{1}{R_{L,\min}} - \frac{1}{R_{L,\max}} \right) . \qquad (3)$$

To calculate $R_{L,min}$ and $R_{L,max}$, we first write the dc-current equation at the output node *P* in Fig. 2b:

$$I_{SS} - I_0 - I_{P2} - I_{P3} = 0 \ . \qquad (4)$$

As the tail current I_{ss} is constant and the transistor *M1a* is operated in the saturation region with constant current I_0, the relevant variation of the load resistance for the determination of the tuning range comes from changes of I_{P2} and I_{P3}. The load resistance is maximum and the oscillation frequency becomes minimum when the transistor *M2a* is completely turned off ($I_{P2} \approx 0$) and *M3a* carries maximum current. Furthermore, we assume that the output common model level where f_{osc} is minimum equals 2/3 of the supply voltage V_{dd}:

$$V_{CM} = V_{DD} - R_{L,\max} \cdot \frac{I_{ss}}{2} = \frac{2}{3} V_{dd} \ . \qquad (5)$$

The resulting load resistance $R_{L,max}$ is then given by

$$R_{L,\max} = \frac{V_{dd} - V_{CM}}{\frac{I_{ss}}{2}} = \frac{\frac{1}{3} V_{dd}}{\frac{I_{ss}}{2}} \ . \qquad (6)$$

The minimum load resistance $R_{L,min}$ can be determined for the case when the PMOS tuning transistor *M2a* is fully turned on ($V_{GS,M2a} \approx -V_{dd}$). As *M3a* is diode-connected, the minimum voltage drop across the PMOS load transistors is at least greater than the threshold voltage $V_{th,M3a}$ of the transistor *M3a* and $R_{L,min}$ then becomes

$$R_{L,\min} \approx \frac{V_{th,M3a}}{\frac{I_{ss}}{2}} . \qquad (7)$$

Recapitulating the equations above, the tuning range can be written as

$$tuning\ range \approx \frac{\frac{1}{2} I_{ss}}{2N \cdot C_L} \left(\frac{1}{V_{th,M3a}} - \frac{1}{V_{dd} - V_{CM}} \right) . \qquad (8)$$

A brief verification of equation (8) by inserting the parameters used to design the oscillator (I_{ss}=3 mA, N=3, C_L=70 fF, $V_{th,\ M3a} \approx$300 mV, V_{dd}=1.7 V and V_{CM}=2/3V_{dd}) yields a tuning range of 5.8 GHz at a center frequency of 12.4 GHz. It should be noted that equation (8) is only a rough approximation of the tuning range as the model assumed is very simple and the parasitics are also neglected. As will be shown by the measurements, the analytically obtained results are about 20% too high.

As I_{ss} remains constant across the entire tuning range, the output common mode level varies with variations of R_L. This drawback can be eliminated when a replica-biasing scheme is applied to the delay cells [3]. The PLL design presented here does not include such a self-biasing scheme because of circuit complexity reasons.

The gain of the oscillator can be estimated by

$$K_{osc} = \frac{tuning\ range}{V_{dd} - v_{dsat,MN} - v_{dsat,MP}} \cdot \alpha , \qquad (9)$$

where $v_{dsat,\ MN}$ and $v_{dsat,\ MP}$ are the saturation voltages of the NMOS and PMOS tail current transistors in the charge pump shown in Fig. 4 and α denotes the gain reduction factor owing to the source degenerated level control circuit [Fig. 2(c)].

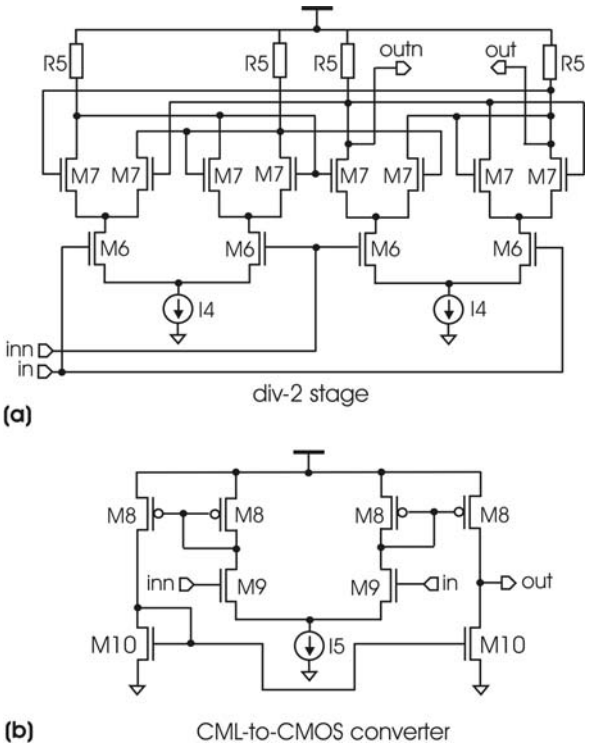


Fig. 3. (a) Divide-by-2 stage used in the 1/16-divider; (b) CML-to-CMOS converter.

The schematic of a divide-by-2 stage used in the 1/16 divider is shown in Fig. 3a. The individual divide-by-2 stages are current and size-scaled by the resistor *R*5 and the tail current *I*4 in order to save power. The CML-to-CMOS converter shown in Fig. 3b, which is used at the output of the 1/16 divider, basically consists of a differential stage whose output currents are mirrored into a complimentary output stage. This yields a rail-to-rail output swing comparator that produces a full-swing, single-ended, CMOS-level signal.

Figure 4 shows the schematic of the PFD and the charge pump. The phase detector implemented here is of a widely used digital PFD type consisting of two edge-triggered flip-flops, which are reset if both outputs are high. It produces up and down pulses to control the charge pump. The minimum width of the pulses when no phase difference occurs at the inputs is set by the delay introduced by the additional inverters in the reset loop.

The charge pump uses constant current sources on both rails and single-pole, double-through (SPDT) switches to route the current either to the output through one cascode-connected transistor (*M*12, *M*15) per polarity, or to the other rail (through *M*11, *M*16). Thus, the current sources are always loaded, which minimizes the switching feedthrough. The charge pump has been designed for a gain of 1.5 mA/rad.

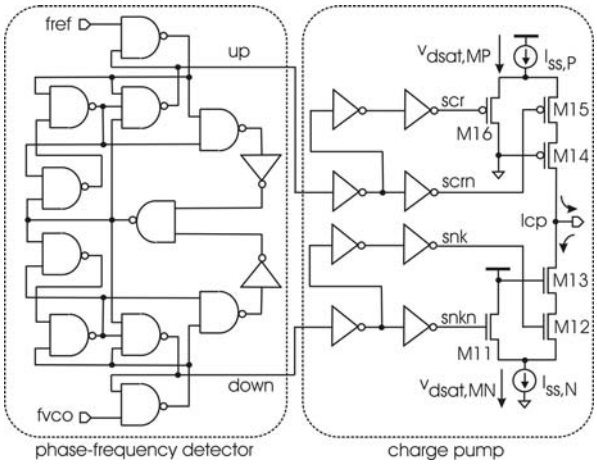


Fig. 4. Phase-frequency detector and charge pump.

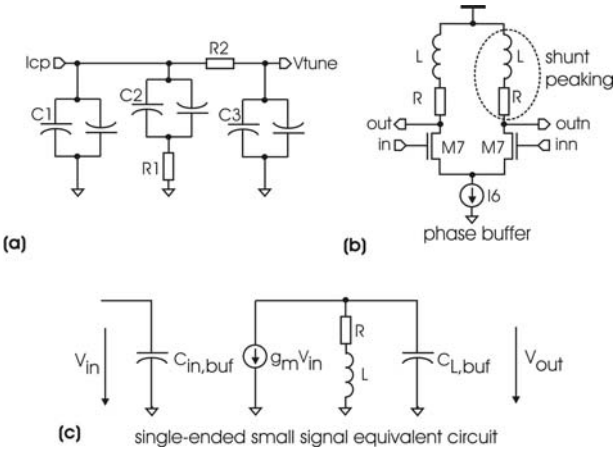


Fig. 5. (a) Third-order loop filter: *C*1 = 31 pF, *C*2 = 452 pF, *C*3 = 3.1 pF, *R*1 = 53 Ω, *R*2 = 186 Ω; (b) Phase buffer with shunt peaking coil; (c) single-ended small signal equivalent circuit.

The passive loop filter designed is of third order. It was specified for a bandwidth of 10 MHz and a phase margin of 56 degrees. To reduce potential leakage currents in the loop filter, thick oxide MOS capacitances naturally used for decoupling have been applied. As shown in Fig. 5a the capacitances were split into antiparallel sections to mitigate the effect of their nonlinear *C*-*V* characteristic. N^+ diffusion resistors are used for the filter resistors as well as for the load resistors in CML topologies [Figs. 3a and 5b].

Figure 5b shows the schematic of a shunt-peaked CML buffer. The introduction of a low-Q inductor *L* in series with the load resistor *R* increases the bandwidth of the buffer [4]. The impact of the shunt-peaking inductor is

analyzed the most easily by writing down the transfer characteristic (normalized to the transconductance g_m) of the small signal equivalent circuit given by

$$\frac{V_{out}}{V_{in}} \cdot \frac{1}{g_m} = \frac{sL + R}{s^2 \cdot L \cdot C_{L,buf} + s \cdot R \cdot C_{L,buf} + 1} \quad , \qquad (10)$$

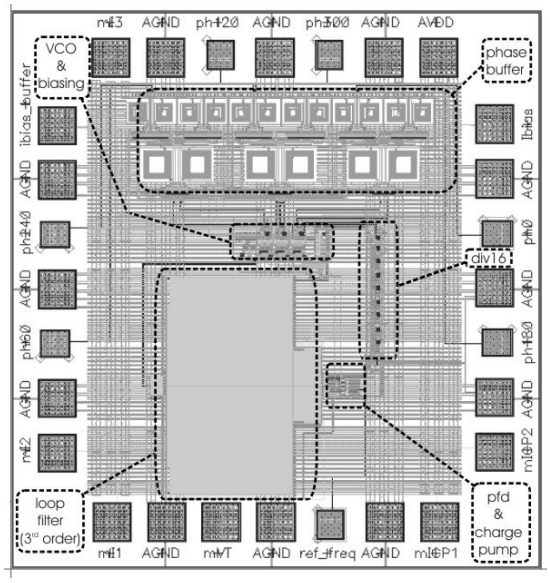
where $C_{L,buf}$ denotes the phase buffer's load capacitance. Compared to the case where no shunt peaking is used (L=0), the introduction of the inductance L inserts an additional pole and a zero. An expression for the maximum bandwidth $\omega_{3dB,\,max}$ can be found by replacing s with jω and setting the magnitude of (9) equal to ½ and solving for $\omega_{3dB,\,max}$:

$$\omega_{3dB,\max} = \sqrt{\frac{4 \cdot L^2 + 2 \cdot L \cdot C_{L,buf} - R^2 \cdot C_{L,buf}^2}{2 \cdot L^2 \cdot C_{L,buf}^2}} \quad . \qquad (11)$$

The optimum L where the bandwidth becomes maximum is obtained by evaluating $\delta\omega_{3dB,\,max}/\delta L$=0. This

Fig. 6. Layout of the fabricated PLL chip. Overall chip dimensions are 1×1 mm^2.

yields



$$L = \frac{1}{\sqrt{2}} \cdot R^2 \cdot C_{L,buf} \quad . \qquad (12)$$

An even higher bandwidth enhancement can be achieved by using more sophisticated inductive peaking configurations (e.g. T-coils) as presented in [5].

The layout of the fabricated PLL is shown in Fig. 6. Except for the supply voltage, only two reference bias currents for biasing the buffer stages and the core PLL must be applied, together with the external reference frequency signal, to operate the chip.

III. Measurement Results

The PLL was tested on-wafer with four high-speed power-ground-signal-ground-signal-ground-power (P-G-S-G-S-G-P) probes. Figure 7 shows the measured maximum oscillation frequency at which the PLL still locks, together with the power consumption efficiency versus the supply voltage. The maximum oscillation frequency of 14 GHz is obtained at a supply voltage of 2.0 V. The power consumption efficiency is defined here as $Vdd \cdot I_{dc}/(f_{max} \cdot 10)$. The factor of 10 in the denominator comes from the specification that the phase buffers feed ten digital CDR receivers. In the frequency band of interest between 9.6 and 12.8 GHz the power consumption efficiency varies from 1.0 to 1.5 mW/GHz. As shown in Fig. 7, by a variation of the supply voltage from 0.9-2.1 V a frequency range of almost 5-14 GHz could be covered.

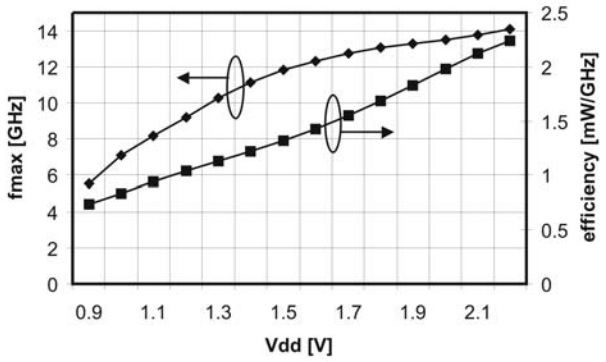


Fig. 7. Measured maximum oscillation frequency and power consumption efficiency versus supply voltage.

A typical frequency spectrum of the PLL measured at 10.24 GHz is shown in Fig. 8. The suppression of the reference frequency spurs is about 35 dB. Figure 9 shows the phase noise measured at 12.48 GHz. The characteristic of the phase noise curve indicates that the actual loop bandwidth is approximately 10 MHz with a peaking of 2 dB. The rms phase error can be obtained by integrating the phase noise curve [6]:

$$\Phi_{\text{rms}} = \frac{1}{2\pi}\sqrt{\int_0^{\infty} L(f)df} \approx \frac{10^{\frac{k}{20}}}{2\pi}\sqrt{\frac{f_c}{2}\left(1+10^{\frac{p}{10}}\right)}. \quad (12)$$

The second term in (12) is an approximation of ϕ_{rms} when only the contribution of the in-band phase noise is considered. With p = 2 dB, f_c = 10 MHz and an in-band phase noise of –85 dBc/Hz, the calculated rms phase error becomes 0.032 UI. A verification measurement in the time domain at 12.8 GHz is shown in Fig. 10. The built-in jitter measurement utilities of the oscilloscope outputs 0.017 UI rms jitter and 0.12 UI peak-to-peak jitter.

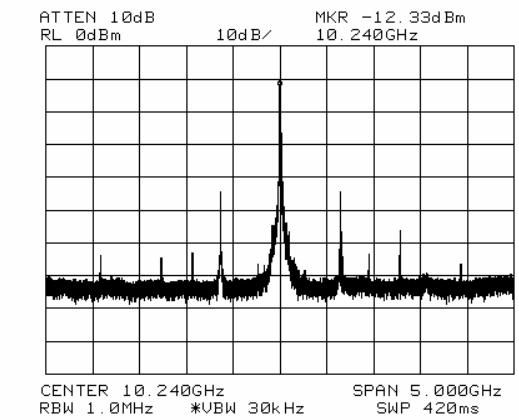


Fig. 8. Measured frequency spectrum at 10.24 GHz and *V*dd = 1.3 V.

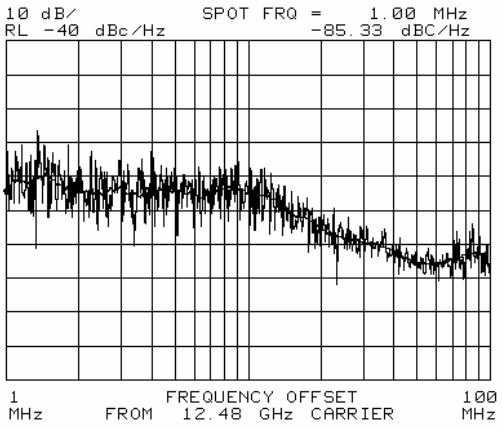


Fig. 9. Measured phase noise at 12.48 GHz and *V*dd = 1.7 V.

Figure 11 shows the PLL's tuning range for *V*dd = 1.7 V. The desired frequency band is completely covered and the tuning range is about 35%. It has been shown that the tuning range increases for lower supply voltages and reaches nearly 1 octave at *V*dd = 1.0 V. The characteristic of the output power level of the phase buffers and the power consumption of the overall circuit across the tuning range is shown in Fig. 12. A relatively constant power level and current consumption of approximately –11 dBm and 114 mA (195 mW/1.7 V), respectively, within the desired frequency band is achieved. Note that the output buffers were designed for a capacitive, high-impedance load and not for being measured in a 50 Ω measurement system.

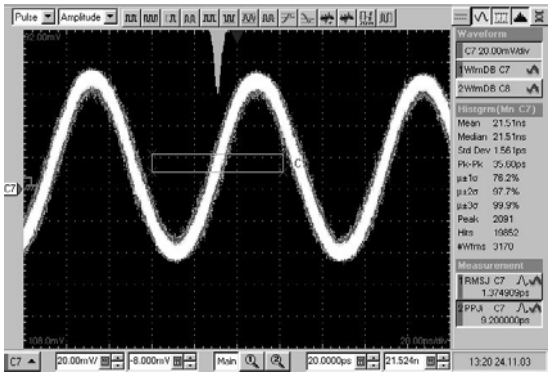


Fig. 10. Time domain waveform at 12.8 GHz and *V*dd = 1.7 V.

Figure 13 shows the step response from 10.0 to 9.84 GHz measured with the modulation domain analyzer HP 53310A. The PLL's output frequency has been down-converted such that it fits the input frequency range of the modulation domain analyzer.

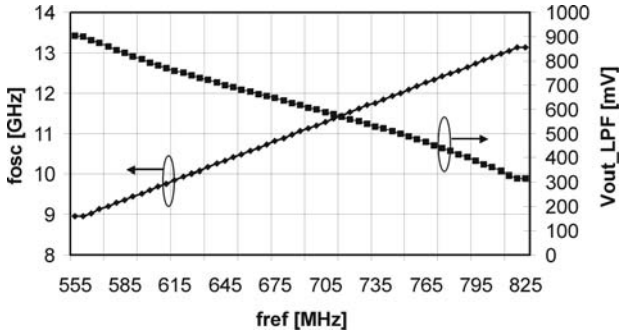


Fig. 11. Measured oscillation frequency and loop filter output voltage versus reference frequency at *V*dd = 1.7 V.

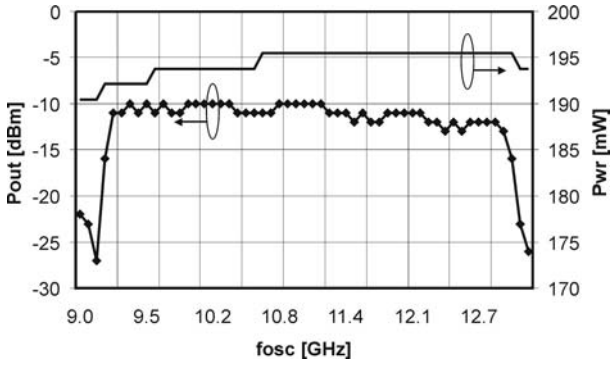


Fig. 12. Measured power level of phase buffer output signal and overall power consumption versus oscillation frequency at *V*dd = 1.7 V.

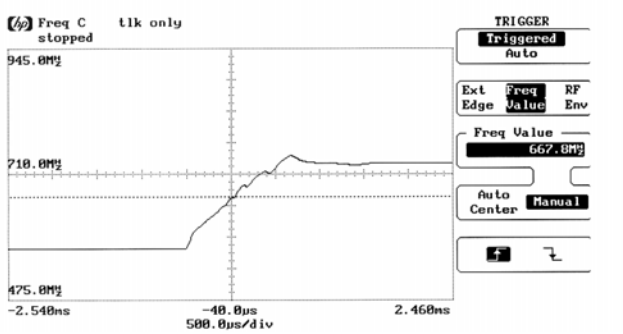


Fig. 13. Frequency step response measured with modulation domain analyzer (vertical axis: frequency; horizontal axis: time).

Individual test circuits of the divider used in the PLL have been designed and measured. Figure 14 shows the single-ended output signal of the div-16 circuit whose high-level schematic is depicted in Fig. 1. The differential 14 GHz input signal generated by an Agilent signal source, and an external 180° hybrid coupler had a peak-to-peak amplitude of 150 mV. The divided output signal was measured with a 25 dB on-chip attenuator, resulting in an on-chip output signal amplitude of 520 mV. The current consumption of the entire div-16 circuit including preamp and differential-to-single-ended converter is 5.0 mA at a supply voltage of 1.0 V.

The first divide-by-two circuit [Fig. 3a] of the div-16 divider has also been measured separately as a test circuit. Figure 15 shows the resulting differential output waveform for an input signal of 20 GHz with 570 mV amplitude. Taking into account that a 34 dB on-chip attenuator has been used to measure the divided signal at 10 GHz, the resulting on-chip output amplitude is 230 mV. The current consumption of the divide-by-two stage at V_{dd}=1.0 V is 960 µA. Measurements at even higher frequencies could not be performed owing to measurement equipment constraints.

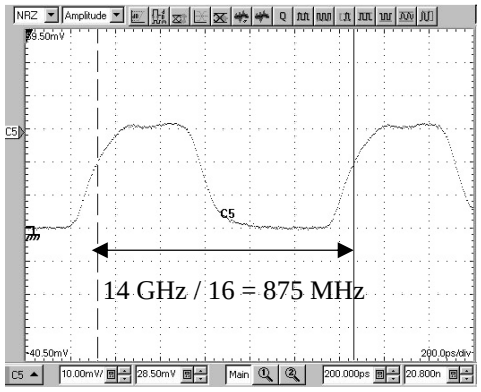


Fig. 14. Time domain output signal of the div16 test circuit used in the PLL [Fig.1] measured at V_{dd}=1.0 V.

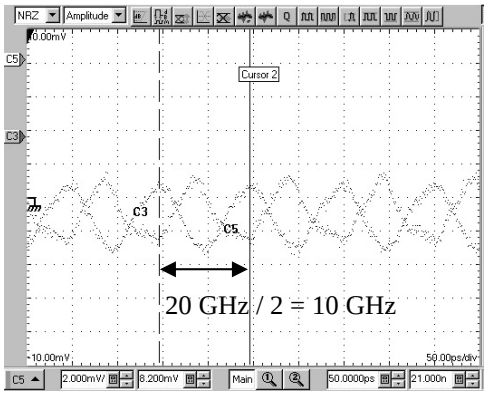


Fig. 15. Differential time domain output signal of the first divide-by-two stage of the 1/16- divider measured as test circuit at 20 GHz [Fig. 3a].

IV. Conclusion

The design of a multiphase PLL for 10 Gb/s links based on digital CDR receivers is presented. The PLL fabricated in a 90-nm SOI CMOS technology covers the frequency band from 9.6 to 12.8 GHz and shows a power consumption of 195 mW at a supply voltage of 1.7 V. The circuit also includes shunt-peaked phase buffers that are capable of spreading the multiphase signal to ten links. The measured rms jitter is around 0.03 UI and the tuning range is greater than 35%. Approximation formulas to estimate the PLL's tuning range and the analytical derivation of the optimum shunt peaking inductance in the CML buffers to maximize the bandwidth were also given.

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Thomas Toifl (S'97-M'99) received MS and Ph.D. degrees from the Vienna University of Technology, Austria, in 1995 and 1999, respectively. In 1996, he joined the Microelectronics Group of the European Research Center for Particle Physics (CERN), Geneva, Switzerland, where he worked on radiation-hard integrated circuits for particle physics detectors. In 2001, he joined the IBM Zurich Research Laboratory, where he has been working on multi-gigabit, low-power communication circuits in advanced CMOS technology.

Martin Schmatz (M'94) received MS and PhD degrees in Electrical Engineering in 1993 and 1998, respectively, from the Swiss Federal Institute of Technology (ETH) in Zurich for work on low-power wireless receiver designs and noise parameter measurement systems. In 1999, he joined the IBM Zurich Research Laboratory, where he established a research group focused on high-speed and high-density CMOS serial link systems and optical link extension of electrical I/Os. Since 2001, he has managed the I/O Link Technology group.