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Research Report

Effect of Body Contacts on High-Speed Circuits in 90 nm CMOS SOI Technology

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Effect of Body Contacts on High-Speed Circuits in 90 nm CMOS SOI Technology

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Abstract— **Silicon-on-insulator (SOI) technology has been successfully used for very high performance VLSI circuits for a few years now. These processes employ partially depleted FET devices with floating bodies. To avoid a time-dependent behavior of these devices in sensitive circuitry, selected bodies can optionally be tied to a controlled potential by means of body contacts. The device then is no longer affected by trapped charges within the channel, thus preventing signal-pattern-dependent variations in V_T.**

The effect of such body contacts on two representative circuits, a CML buffer and a distributed amplifier, has been studied. It is shown that the introduction of body contacts reduces the bandwidth, increases the jitter but also increases the gain of amplifier circuits.

Index Terms— **CMOS analog integrated circuits, SOI technology, integrated circuit design.**

I. Introduction

High-speed I/O front-end circuits of modern telecommunication and datacom systems typically operate at several times the core circuit's clock speed. Often designed as serial links, these circuits have to deal with very broadband data streams. Designers of these circuits face the challenge of pushing the upper band limit ever deeper into the multi-10-GHz regime, while also providing support for long sequences of consecutive symbols without losing synchronization, i.e. simultaneously supporting very low and very high frequency components of the data streams.

Increasing the maximum signal frequency can be achieved by using more sophisticated data/clock recovery architectures and algorithms, efficient channel equalization methods, suitable circuit designs and advanced CMOS process technologies.

The latter include silicon-on-insulator (SOI) technologies which introduce a thin buried oxide (BOX) layer between the body of a FET and the underlying substrate (Fig. 1), thus reducing the area junction capacitance C_J. For digital circuits, a performance increase of 20–35% is possible compared with bulk processes having equal feature sizes [1]. Whether this also holds true for analog circuits depends on circuit topology and on whether secondary effects become predominant. This work investigates these tradeoffs.

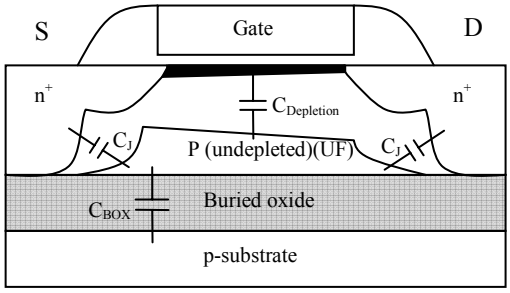

Figure 1. SOI n-FET

Through the BOX layer, the transistor body's undepleted fraction (UF) becomes electrically floating. Depending on its electrical potential, it alters the transistors effective threshold voltage V_T by acting as a back gate. The UF voltage is determined by the preceding states of the device and hence is time- and pattern-dependent [2], [4]. One way to avoid such time-variant device characteristics is by adding a body contact (BC) to tie the UF region to the substrate [6]; however, at the price of the unwanted side effect of increasing the gate and junction capacitance. To investigate the tradeoff between time-variant device characteristics and bandwidth (BW) reduction due to higher parasitic capacitances, I/O building blocks were implemented with and without BC.

II. Test Circuit Selection

Jitter- and BW-sensitive high-speed I/O circuits typically consist of an input amplifier followed by clock data recovery (CDR) circuits. The main concern with these circuits/stages is to keep the jitter contributions as low as possible and to achieve the required broad input BW. To investigate whether the predominant degradation of those performance criteria is caused by a dynamic V_T or by the bandwidth reduction due to the additional BC capacitance, two representative I/O building blocks have been selected and their peak-to-peak jitter and bandwidth compared. The circuits were implemented in variants with and without BCs; i.e., the design and layout of the variants only differ in the presence/absence of BCs.

A. CML Buffer Amplifier

The first stages of the CDR logic are typically significantly less complex than the core logic, but their speed requirements are often much higher. For this reason, current mode logic (CML) stages instead of CMOS circuit topologies are widely

used. A two-stage, frequency-peaking CML buffer was chosen to investigate the impact of BC presence/absence on timing jitter.

B. Distributed Amplifier

For broadband applications up to very high frequencies, distributed circuits may sometimes be preferred over other architectures. Accordingly, an existing distributed amplifier (DA) design has been chosen to study the impact of BCs on the circuit frequency response.

III. CIRCUIT DETAILS

A. Two-Stage CML Buffer

Fig. 2 shows the schematic of the CML buffer investigated.

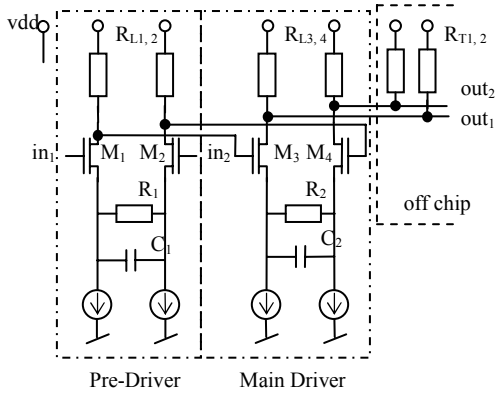

Figure 2. Two-stage CML buffer

The circuit is fully differential and consists of two stages: a pre-driver ($M_{1/2}$) that drives the main driver ($M_{3/4}$). The predriver has small input transistors compared with those of the main driver. In this way, the current drive requirements for the preceding stage can be kept low.

The main driver absorbs the line termination resistors ($R_{T1/2}$) into its load resistance. This has several advantages over providing the entire load resistor internally.

The main advantages of such a configuration are:

(1) The lines are always properly terminated.
(2) No bulky coupling capacitors are required.
(3) External components can be used that usually have lower tolerances than on-chip resistors, which improves the circuit accuracy.

By adding R_1,C_1 and R_2,C_2, differential source degeneration is introduced. This leads to gain peaking and increases the circuit bandwidth.

The components of this circuit and the DC operating point details of the CML buffer are given in Table I.

TABLE I. CML BUFFER PARAMETER VALUES

	Parameter	I_{DC}
$M_{1,2}$	35 µm/80 nm	3.3 mA
$M_{3,4}$	105 µm/80 nm	10 mA
R_1	83 Ω	
R_2	25 Ω	
$R_{L1,2}$	83 Ω	
$R_{L3,4}$	55 Ω	
$R_{T1,2}$	50 Ω	
v_{dd}	1.0 V	26.6 mA

An increase in gate capacitance is expected to have the greatest impact between the two stages. There, the source resistance ($R_{L1,2}$) and the load capacitor (C_{in} of $M_{3,4}$) are both large compared with the input stage ($R_{\text{Measurement Equipemt}} = 50\ \Omega$) and ($C_{in}$ of $M_{1,2}$), resulting in a large RC-time constant. Therefore a considerable degradation in bandwidth of the entire circuit is expected for the circuit variant that uses BCs.

B. Distributed Amplifier

In Fig. 3, the schematic of the DA is shown.

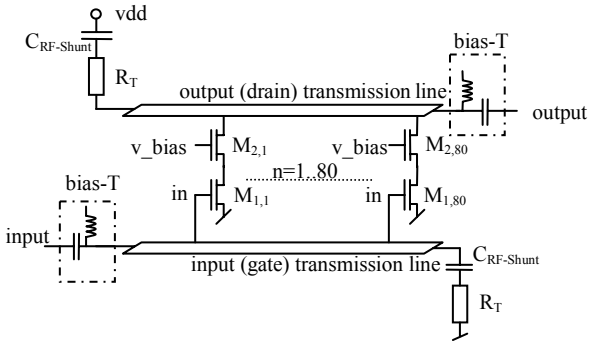

Figure 3. Distributed amplifier

The circuit consists of 80 identical stages, distributed homogeneously along the input and output transmission line. These transmission lines are designed to absorb the input (gate) and output (drain) capacitance equally well and present a real-valued 50-Ω impedance to the input- and output-termination networks [5]. DC supply current and input bias voltages are provided through bias-Ts at the output and input, respectively. To increase gain, reduce the input capacitance (Miller effect) and increase output resistance, the individual gain stages are designed as a simple cascode stages. The total transistor size for the DA is based on the work presented in [3], in which also an excellent noise performance for the DA architecture in this technology is demonstrated.

Owing to layout constraints, only the common source devices ($M_{1,1\text{-}80}$) (Fig. 3) of the gain stages have been provided with BCs. Changes in their gate capacitance are critical, because it is the predominant capacitance in the circuit. In relation to it, the possible effect of BCs on the common gate (cascode) devices ($M_{2,1\text{-}80}$) is expected to be negligible, because their gate capacitance is held at a DC level.

Although this particular design is not well suited for broadband applications, the effect that BCs have on the circuit bandwidth can be very well demonstrated with it. Circuit details and DC operating conditions are listed in Table II.

TABLE II. DA PARAMETER VALUES

	Parameter	I_{DC}
$M_{1,1\text{-}80}$	2 µm/ 80 nm	~1 mA
$M_{2,1\text{-}80}$	2 µm/ 80 nm	~1 mA
R_T	50 Ω	
$C_{RF\text{-}Shunt}$	42 pF	
v_{bias}	1.2 V	
v_{dd}	1.4 V	84 mA

IV. RESULTS

A. CML Buffer Measurements

For the jitter measurements, a periodical input data signal at 5.4 Gbit/s is used.

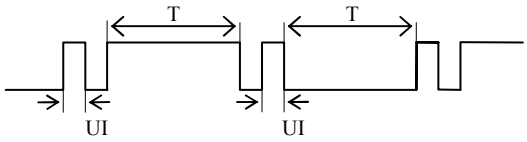

Figure 4. Input signal for jitter measurements

Each sequence of consecutive symbols with length T is preceded by a pulse with one unit interval (UI) duration. T assumes values from 1 UI (= 185 ps) up to 1280 UI (= 0.24 µs) (Fig. 6). The upper boundary of T is only limited by the bias T used, which has a lower corner frequency of 50 kHz.

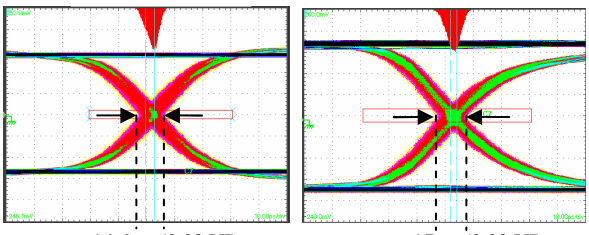

Figure 5. Typical "eye" diagram of the CML buffer without BC (left), with BC (right), T = 40 UI.

Lower gain and lower jitter can be observed for the floating body circuit in Fig. 5.

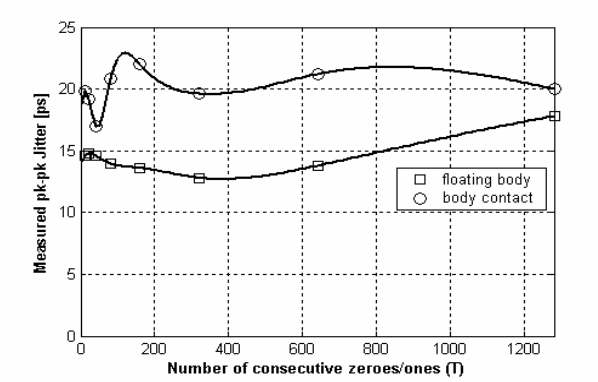

Figure 6. Peak-to-peak jitter vs. number of consecutive symbols (T)

The floating-body circuit always exhibits a better jitter performance up to very long sequences of consecutive symbols (Fig. 6).

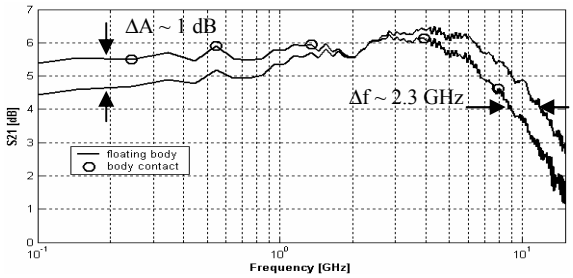

Figure 7. Frequency response of CML Buffer Amplifier (100 MHz to 15 GHz)

The fully differential S-parameter measurements (Fig. 7) again reveal the lower DC gain of the floating-body circuits observed in the time domain (Fig. 5). Its bandwidth however is considerably higher (~20% in this case) than that of the BC circuits.

B. DA Measurements

Fig. 8 shows the single-ended measurements of the DA circuits.

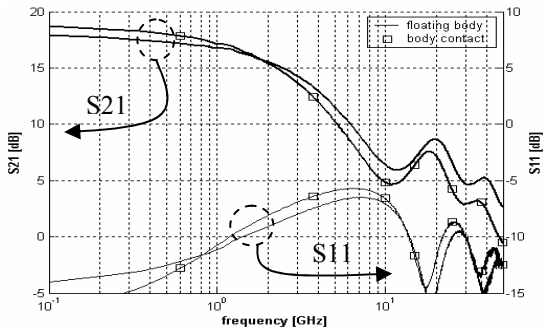

Figure 8. Frequency response comparison for the DA, with and without BCs (100 MHz to 50 GHz)

Confirming the results from the CML buffer, the BC circuit exhibits higher DC gain, and its bandwidth is also considerably reduced.

C. Measurement Summary and Interpretation

Higher intrinsic gain for body contact devices:
Between drain, body and source, a parasitic npn transistor is formed. Devices with BCs turn this bipolar transistor off, whereas those with floating bodies allow it to be partially turned on. Its "collector-emitter" current is controlled by diode leakage, impact ionization and gate-to-body tunneling currents [4]. This transistor degrades the output conductance of the FET (gds) (Fig. 9). Its effect manifest itself in Fig. 5 by the higher amplitude for the BC version as well as in Figs. 7 and 8 by the higher DC gain for circuits with BC.

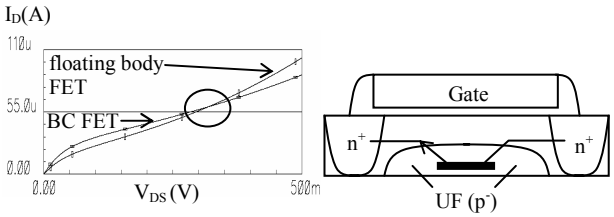

Figure 9. Characteristic IV curve of floating-body vs. body-contact devices and parasitic npn transistor

Lower peak-to-peak jitter for floating-body devices:
Fig. 6 shows the advantage of using floating-body devices over the use of BCs. A reduction in the peak-to-peak jitter on the order of 25% is observed over a broad span of *T*. The convergence of the two series towards higher values of *T* is due to the lower cutoff frequency of the bias *T*, where band-limitation effects predominate over the jitter differences between the circuits.

Higher bandwidth for floating-body devices:
The DA and the CML buffer amplifier show a significantly higher bandwidth for the variants without BCs (Figs. 7 and 8). Taking input and output mismatch into account, i.e. considering the circuit power gain, yields the same results.

V. Conclusions

Two different test circuits in 90-nm CMOS SOI technology have been manufactured with and without body contacts. The parasitic capacitance introduced by BCs substantially reduces the BW of either circuit and degrades the jitter performance of the CML buffer.

When BCs are avoided, the full potential of the SOI technology is available. Performance degradation due to floating bodies leading to time-variable threshold voltages (V_T) could not be observed. This even holds true for very long bit patterns of consecutive symbols.

The use of BCs for the very-high-speed circuits presented exhibits no benefit whatsoever. Because transistors with BCs have a higher output resistance r_{out} at identical bias conditions, they may very well be preferred over floating-body devices for high-gain lower-BW and current source applications or in those circuits where a high r_{out} may be a prerequisite (e.g. control-loop operational amplifiers).

VI. Acknowledgment

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