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Research Report

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Towards electro-optical integration of hybrid III-V on Si lasers into the BEOL of a CMOS technology

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Introduction Interconnects have become a severe bottleneck in today's computing hardware [1]. For large-scale data centers in particular, the interconnect situation is even more severe [2]. The interconnect bandwidth and bandwidth density have to be increased on all system-levels. The ideal technology to increase the density is Si photonics (SiPh). While the integration of most of the SiPh components has been mastered already on a 90 nm CMOS platform [3], the integration of III-V materials to yield directly-modulated lasers still poses a major challenge. This integration is considered as the cornerstone for reaching a complete, yet cost-competitive, SiPh-CMOS marriage. Most concepts shown so far [4, 5] either lack CMOS-compatibility or have device dimensions that hinder the integration of the laser into a standard BEOL. To allow for a common BEOL between SiPh and CMOS, we integrate the III-V material between the FEOL and BEOL, within the first interlayer dielectric ILD0' (Fig. 1). Such integration imposes tight requirements on device dimensions as well as several technological challenges that have to be mastered. We report here on decisive aspects of such integration. This represents a major step towards a full integration of III-V, SiPh and CMOS.

Concept For the integration between BEOL and FEOL, several prerequisites have to be fulfilled. The laser stack needs to be extremely thin (<250 nm). All processes need to be CMOS compatible and have to be adapted for these dimensions, i.e. ohmic contacts (Au-free, shallow alloying), dry etching and current confinement. In our concept, illustrated in Fig. 1a, we insert the laser stack in a new ILD0' (FEOL) that is still below the first interconnect layer M1. Such step allows for a common BEOL between SiPh and CMOS.

Material Epitaxial material in this work was grown by MOCVD on 2" SI-InP substrates. Optimized growth conditions yielded very smooth surfaces (Fig. 2a). The InAlGaAs multiple quantum wells (MQW) exhibit atomically flat interfaces (Fig. 2b). MQW composition and thickness were tuned to obtain a PL peak at 1300 nm (Fig. 2c). The material stack is bonded on pre-processed SiPh structures on an SOI wafer (220 nm Si, 2 μm BOX).

Contacts Transfer length method structures were fabricated using a CMOS-compatible process involving passivation-first, via-opening, sputter metal deposition, dry etch metal patterning and rapid thermal anneal. p-Type contacts on InP:Zn ($2\cdot10^{18}$ cm^{-3}) have been analyzed extensively. A TiN/Ni stack yielded the best result on p-InP (Fig. 3a). Nonetheless, no ohmic behavior has been achieved for any tested combination. To obtain ohmic behavior, a p-$In_{0.53}Ga_{0.47}As$ cap is needed. This cap enables low-resistive contacts for different metal stacks e.g. Ti/Al (Fig. 3b) and Mo/W (Fig. 3c). Most stable results were achieved for Mo/W with ρ_c down to $1\cdot10^{-5}$ $\Omega\cdot$cm^2 and very shallow alloying (Fig. 3d). n-Type ohmic behavior was obtained on InP:Sn ($5\cdot10^{18}$ cm^{-3}). Optimized contacts using Ni and Si resulted in ρ_c between 0.6-$1.6\cdot10^{-7}$ $\Omega\cdot$cm^2 (Fig. 4a). A comparison of the ALD-Al_2O_3/InP (Fig. 4b) and NiSi/InP (Fig. 4c) boundaries indicates in both cases sharp high-quality interfaces.

Dry etch Dry etching was performed via ICP-RIE on either bulk or bonded III-V material. A commonly-used $Cl_2/BCl_3/CH_4/H_2$ etch chemistry was employed to optimize the dry etch on bulk material for a slanted profile and to mitigate trenching (Fig. 5a). However, this dry etch was not successful on bonded material (Fig. 5b). A newly developed Cl_2-based process shows both very smooth sidewalls (Fig. 6a) and etched surfaces on bonded material (Fig. 6b). A full cross-section of an etched stack reveals a sidewall angle of 70º and no trenching (Fig. 7a,b).

Current confinement Current confinement is needed to pump the active region efficiently. In shallow structures, this is more challenging. To allow current confinement in the center of the III-V stack even for thin stacks, lateral oxidation was performed via water vapor annealing. We have achieved a selective oxidation between layers with different Al content (Fig. 7b).

Optical coupling Shallow CMOS-compatible III-V lasers optically coupled to Si have not yet been demonstrated. To prove the feasibility of our concept, thin optically-pumped III-V lasers with feedback in Si were characterized. Lasing operation at 1.3 μm using either racetrack resonators (Fig. 1b, Fig. 8a) or DBRs is demonstrated (Fig. 8b).

Conclusion We have shown a concept for which III-V, SiPh and CMOS share a common BEOL. Epitaxial layer optimization, low-resistive ohmic contacts, optimized dry etch, current blocking layer formation and optically-pumped lasers with feedback to the Si waveguide buried below were shown. The next step is to realize an electrically-pumped laser based on this technology.

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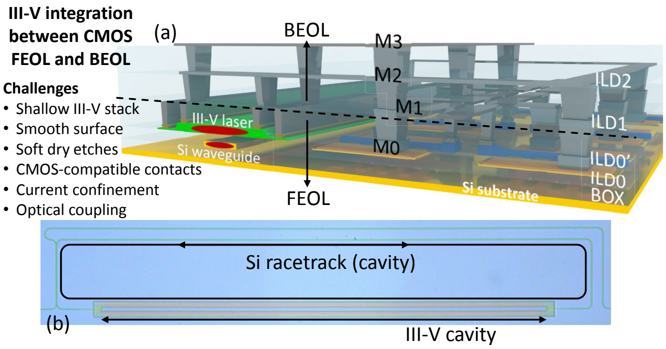
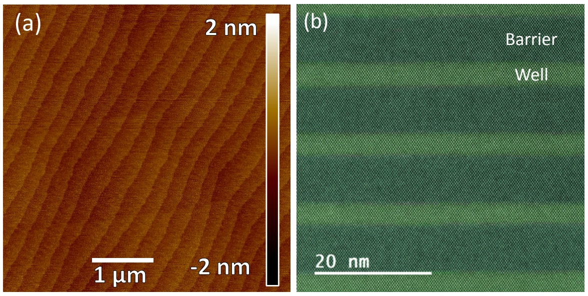


Fig. 1. (a) Illustration of the III-V on Si platform showing an embedded III-V laser between FEOL and BEOL next to a CMOS circuit. Common BEOL can be used. (b) Optical micrograph of a racetrack ring laser (*cf.* Fig. 8a).



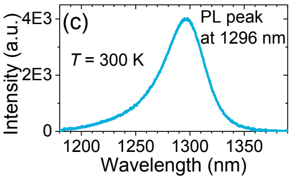


Fig. 2. (a) AFM image of a laser stack surface (rms = 0.1 nm), (b) STEM image of MQW, (c) Room temperature PL peak of the gain medium.

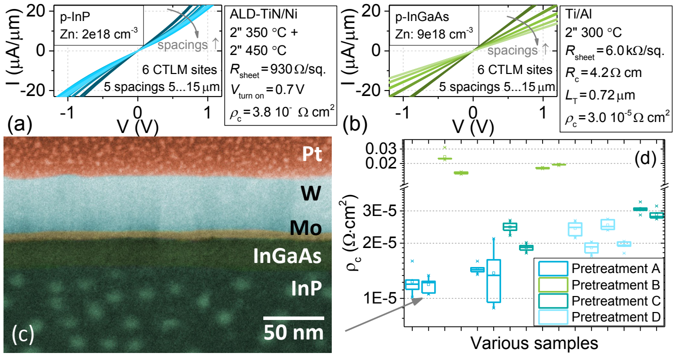


Fig. 3. I-V curves of (a) TiN/Ni contacts on p-InP and (b) Ti/Al contacts on p-InGaAs for five contact separations. (c) CS-SEM of sample indicated by arrow in (d). (d) ρ_c box plots for Mo/W contacts on p-InGaAs with various pretreatments.

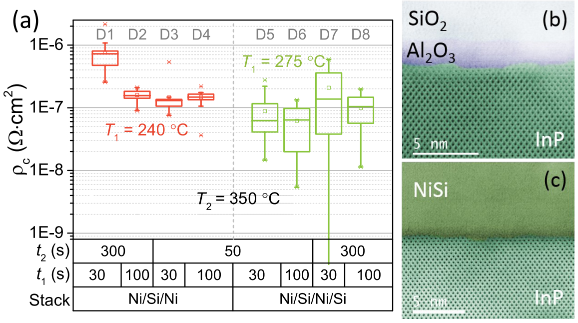


Fig. 4. (a) Box plots of ρ_c for Ni/Si-based contacts on n-InP annealed at various conditions. STEM images of sample D3 in (a) showing the (b) Al$_2$O$_3$/InP and (c) NiSi/InP interface of the same sample. A sharp metal-semiconductor interface is observed.

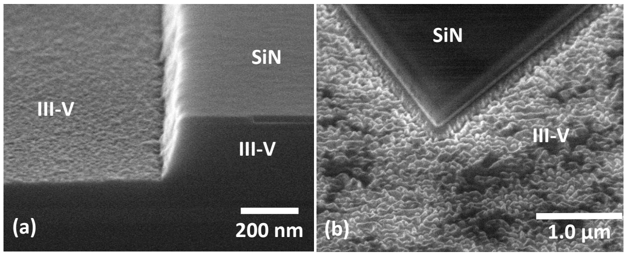


Fig. 5. (a) BCl$_3$/Cl$_2$/CH$_4$/H$_2$ dry etching of a MQW stack on 2" SI-InP (bulk) shows a rather smooth etch surface and only little trenching, (b) the same recipe on bonded material shows very rough etched surface and sidewall.

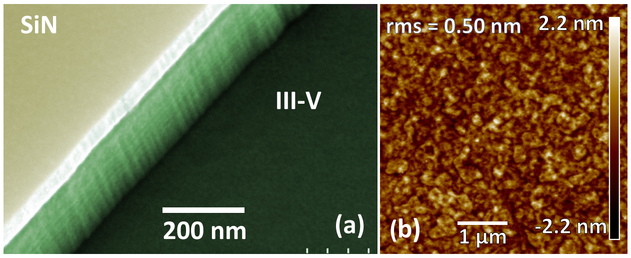


Fig. 6. (a) New Cl$_2$-based etch shows trenching <3%, smooth sidewall and etched surface on the MQW stack bonded on SOI, (b) AFM image of the etched surface showing minimal damage with 0.5 nm rms roughness.

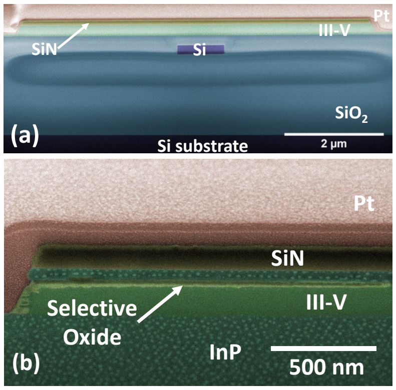


Fig. 7. SEM cross-sections of (a) etched laser stack on bonded material, (Si waveguide is visible below, halo originates from charging) and (b) selective lateral oxidation showing that mainly one layer is oxidized.

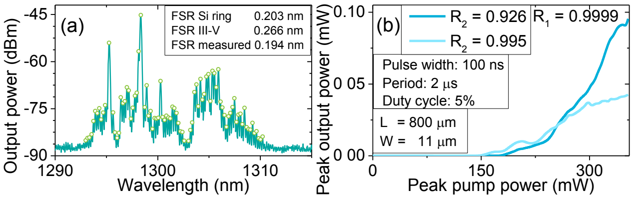


Fig. 8. (a) RT lasing spectrum of an optically-pumped racetrack ring laser showing FSR matching to the Si racetrack (and not to III-V cavity, *cf.* Fig. 1). (b) RT L-I curve of two optically-pumped DBR lasers showing output power dependence on number of DBR pairs. Values are compensated for losses on the detection system.

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