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# Research Report

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# CMOS-Embedded Lasers for Advanced Silicon Photonic Devices

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**ABSTRACT**

Realizing CMOS-compatible integrated lasers on silicon is a crucial step towards cost-efficient, high-functional optoelectronic integrated circuits (OEICs). Here, we report on a concept to embed active optical devices based on a bonded III-V epitaxial layer stack between the FEOL and BEOL of a CMOS silicon photonics chip. Ultra-shallow laser devices are realized with this concept and optically-pumped lasing, coupled to silicon is demonstrated for the first time with such a concept.

**Keywords**: CMOS, III-V–on–silicon, laser, ohmic contacts, dry etching

## 1. INTRODUCTION

Today, datacenters around the world experience massively increasing internal data traffic. Driven by cloud computing, analytics, Internet of Things or server virtualization, the datacenter's total amount of internal traffic can easily surpass its external traffic [1]. Cost-efficient optical interconnects are key to facilitate the necessary high-throughput and low-latency networks, at the required bandwidth and density. For such applications and compared to other photonic integration approaches, silicon photonics (SiPh) offers crucial advantages regarding cost and integration [2]. Today's SiPh chips can be fabricated in CMOS lines, combining all building blocks for transceivers except the laser source. Integration of III-V materials on SiPh for on-chip lasers has therefore become an extensively studied research field. The most important concept for integrating large III-V areas on Si is the heterogeneous integration method using molecular wafer bonding [3]. Based on this concept, active optical devices have been demonstrated, amongst others single-mode lasers [4], [5], and photodetectors [6], [7].

However, most devices shown so far have made use of a several µm-thick III-V layer stack that hinders their integration into a standard CMOS back end of line (BEOL). Such a standard BEOL allows for standard chip assembly techniques that are key to preserve the cost advantage of CMOS chips throughout assembly.

To overcome this drawback and hence, to enable CMOS-embedded active optical devices, we integrate an ultra-thin epitaxial layer stack between the front end of line (FEOL) and BEOL, within the first interlayer dielectric ILD0' (Fig. 1a). This CMOS compatible process allows us to embed active optical devices monolithically into a fully CMOS fabricated chip. This integration scheme represents a major step to reduce assembly and signal routing complexity for future high-speed and high-volume integrated optical technologies. It will bring the functionality of integrated devices to a completely new level, combining CMOS electronics with passive and active optical building blocks.

We report here on the concept and design of our devices alongside with decisive aspects to master the technological challenges of such a tight integration scheme. Optically-pumped lasers are shown to demonstrate the feasibility of our concept.

## 2. CONCEPT AND DESIGN

A schematic cross-section of the laser device, together with the simulated intensity field is shown in Fig. 1b. Photonic waveguides were fabricated in the top Si layer of an SOI wafer. The Si waveguide height is 220 nm. A thin III-V epitaxial layer stack was bonded on top of the processed SOI wafer. The total thickness of this III-V stack is < 300 nm. The III-V layer and the Si layer are separated by silicon dioxide together with a thin layer of alumina that was used to enhance adhesion of the bonding process [3]. A laser cavity was formed by means of fully-etched Bragg mirrors in the Si waveguide with 7 periods on one side and 3 periods on the other side of the gain section. The grating reflectivities are 99 % and 92 %, respectively and the stop-band width is about 500 nm, centered at 1302 nm, as calculated using 3D-FDTD simulations.

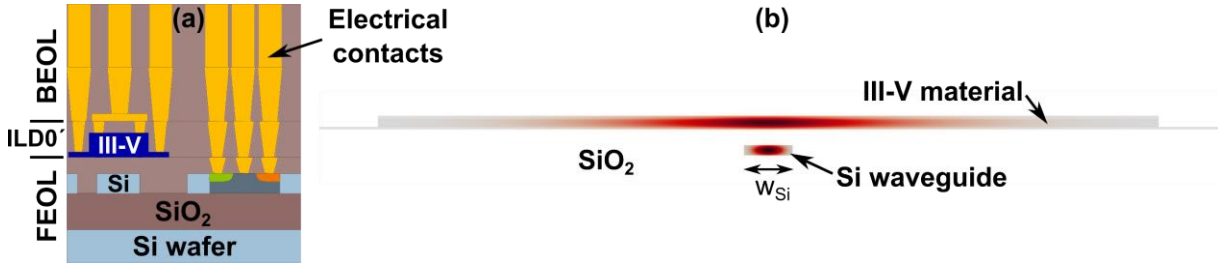


*Figure 1. a) Schematic cross-section of the laser device, integrated between BEOL and FEOL of a CMOS chip. b) Simulated intensity field of the fundamental mode.*

As the laser cavity is defined in the silicon layer and the gain is provided in the III-V layer, low-loss mode-conversion between the two layers is needed. As shown in Fig. 2a, the mode overlap with the III-V material can be fully controlled by adapting the Si waveguide width $w_{Si}$. This is possible by choosing an optimized vertical distance between the Si waveguide and the III-V material. Leveraging this property, efficient adiabatic couplers can be designed based on the concept as described in [8]. Following the authors suggestion in [8], the local taper angle $\Omega(z)$ is inversely proportional to the local beat length $z_b = 2\pi/(\beta_1 - \beta_2)$ throughout the coupler. Here, $\beta_1$ and $\beta_2$ are the propagation constants of the fundamental mode, shown in Fig. 1b, and of the higher order mode having the same symmetry, respectively. This results in a nonlinear taper geometry in the Si waveguide as shown in Fig. 2b. Other design rule concepts [9] reveal similar results.
In addition, once the mode is transferred to the Si layer, the modal field overlap with the III-V material is reduced to 1%. By using tilted facets at the end of the III-V stack, the residual light is efficiently scattered away, overcoming unwanted back-reflections to the cavity.

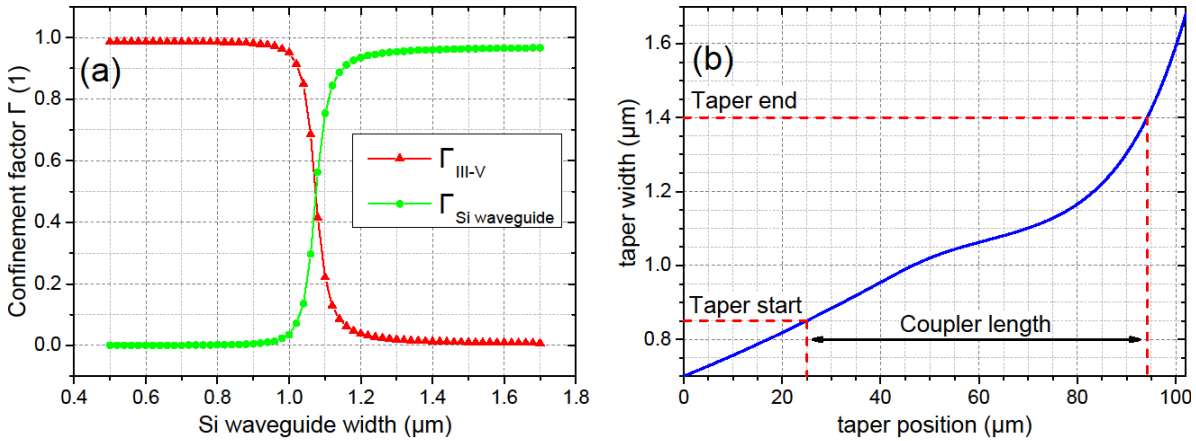


*Figure 2. Design of the adiabatic coupler: a) Calculated mode overlap (confinement factor Γ) versus Si waveguide width for the entire III-V stack (triangles) and the Si waveguide (circles). b) Nonlinear taper geometry for adiabatic couplers, calculated with adiabaticity criterion.*

## 3. FABRICATION

Photonic waveguides were fabricated on a 4" SOI wafer with 220 nm top Si and 2 µm buried oxide (BOX) through electron beam lithography and inductively-coupled plasma – reactive ion etching (ICP-RIE) with HBr. An $SiO_2$ cladding layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) and planarized by chemical-mechanical polishing (CMP). The resulting surface roughness was less than 0.5 nm rms. This enables molecular wafer bonding with high yield [3]. The III-V epitaxial layer stack comprises an InAlGaAs multiple quantum-well (MQW) section (Fig. 3a), sandwiched between a separate confinement heterostructure (SCH) and InP contact layers. It was grown by metal-organic chemical vapor deposition (MOCVD) on a 2" SI-InP substrate. The composition and thickness of the MQW were tuned to achieve a PL peak centered at 1300 nm (Fig. 3b). After bonding the two wafers, the InP substrate was removed by wet chemical etching. The resulting epitaxial layer stack thickness was < 300 nm (Fig. 3c).
Structuring of the III-V material was performed by dry etching via ICP-RIE. A $Cl_2$-based process was developed to achieve very smooth sidewalls (Fig. 4a) and etched surfaces (Fig. 4b). The cross-section of an etched layer stack shows a sidewall angle of 70° and no trenching (Fig. 5a). The commonly used $BCl_3/Cl_2/CH_4/H_2$ etch chemistry in contrast resulted in very rough etched surfaces on our bonded material.

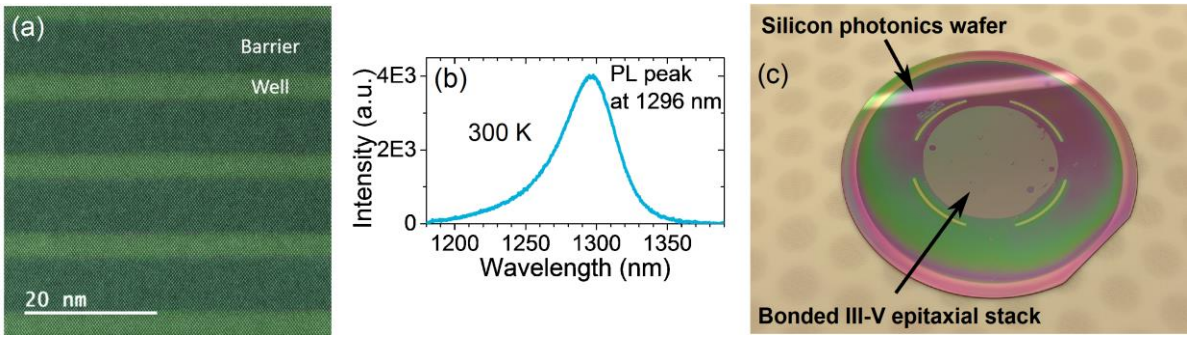


*Figure 3. a) STEM image of MQW with atomically flat interfaces. b) Room temperature PL measurement of the gain material. c) Photograph of the two bonded wafers after InP substrate removal.*

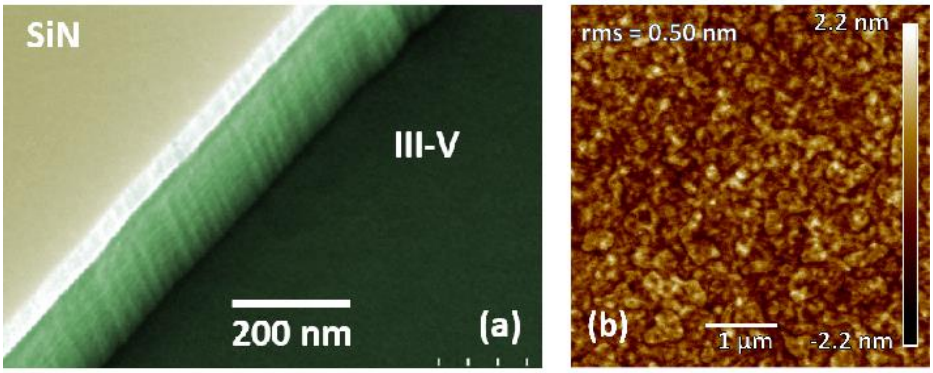


*Figure 4. False-colored SEM image of the dry etched III-V stack, showing smooth sidewalls and etched surfaces. b) AFM image of the etched surface showing a roughness of 0.5 nm rms.*

CMOS-compatible ohmic contacts on InP were developed. Their properties were studied using transfer length method (TLM) structures. After passivating and capping the semiconductor, via-openings were etched and metal was deposited by sputtering. The metal was then patterned by dry etching and finally annealed. Ohmic behavior for n-type contacts on InP:Sn ($5 \cdot 10^{18}$ cm$^{-3}$) was obtained using Ni and Si, resulting in a specific contact resistivity $\rho_c$ between 0.6-1.6$\cdot 10^{-7}$ $\Omega \cdot$cm$^2$. For p-type contacts on InP:Zn ($2 \cdot 10^{18}$ cm$^{-3}$), an additional p-$In_{0.53}Ga_{0.47}As$ cap layer is needed to obtain low-resistive ohmic behavior. A Mo/W metal stack yielded best results with $\rho_c$ of $1 \cdot 10^5$ $\Omega \cdot$cm$^2$.

Current confinement is essential to obtain the necessary overlap of charge carriers with the optical mode. The commonly used $H^+$ implantation in the upper InP cladding layer [10] is not suitable for thin epitaxial stacks. We therefore performed lateral oxidation via water vapor annealing and achieved selective oxidation between layers with different Al content (Fig. 5b). The devices were finally encapsulated with 800 nm PECVD-deposited $SiO_2$.

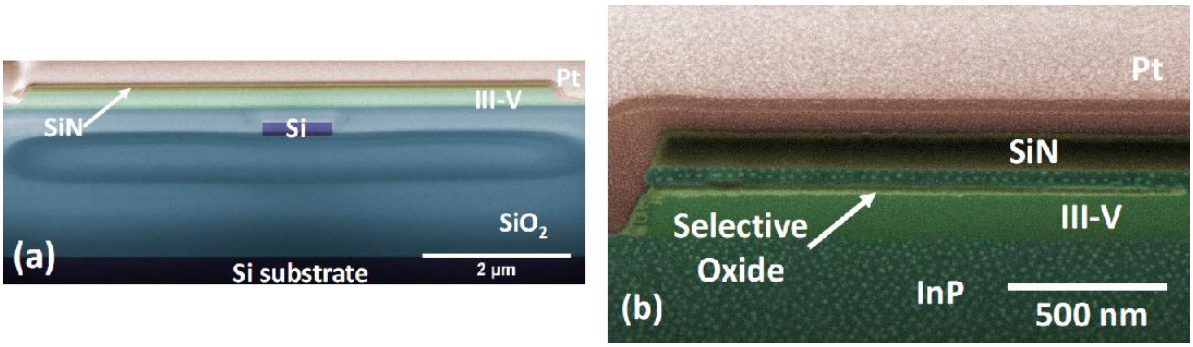


*Figure 5. False-colored SEM cross-sections of a) final laser device (Si waveguide and III-V epitaxial layer stack are visible, halo in BOX originates from charging) and b) III-V epitaxial layer stack with selective lateral oxidation (only a single layer is oxidized).*

## 4. RESULTS

To prove the feasibility of our concept, we have characterized our devices by optical pumping. A fiber-coupled pump laser with a wavelength of 980 nm was coupled into custom-made beam shaping optics to generate a homogeneous line profile on the sample. We measured a line width of 20 µm and length of 600 µm on the sample plane with a beam profiler. The pump laser was operated in pulsed mode with a pulse duration of 100 ns and a maximum peak optical power of 400 mW on the sample. Although the materials of the barriers and the SCH are supposed to absorb the pump laser radiation well, efficient optical pumping is still challenging due to the short absorption length of the thin III-V-layer stack.

Prior to their characterization, the chips were diced and the emitted output light was collected via butt-coupling into a lensed single-mode fiber. The average coupling loss from chip to fiber of -15 dB was subtracted from the power measurement. To normalize the peak pump power, we multiplied the active area of the device by the power density of the pump laser profile. Fig. 6a shows the laser output power versus pump power at room temperature, in which a clear threshold is observed. As expected, the slope efficiency and the laser threshold decrease with higher mirror reflectivity.

A laser output spectrum was acquired with an optical spectrum analyzer (resolution bandwidth 80 pm) and is shown in Fig. 6b. Several longitudinal modes are observed, and the extracted free spectral range (FSR) of 231 pm agrees with the calculated FSR of the cavity. To rule out that the cavity is formed by the III-V facets (Fig. 6b inset), laser spectra of ring lasers were measured (not shown). The gain section of such ring lasers is the same as

the one of the previously mentioned DBR lasers. Compared to the DRB laser, the ring cavity defined on Si is much larger and has hence a clearly distinguishable FSR with respect to the FSR of a cavity that is possibly formed by the III-V facets. The measured FSR of such laser spectra clearly scales with the ring dimension, proving that the cavity is formed on the Si layer.

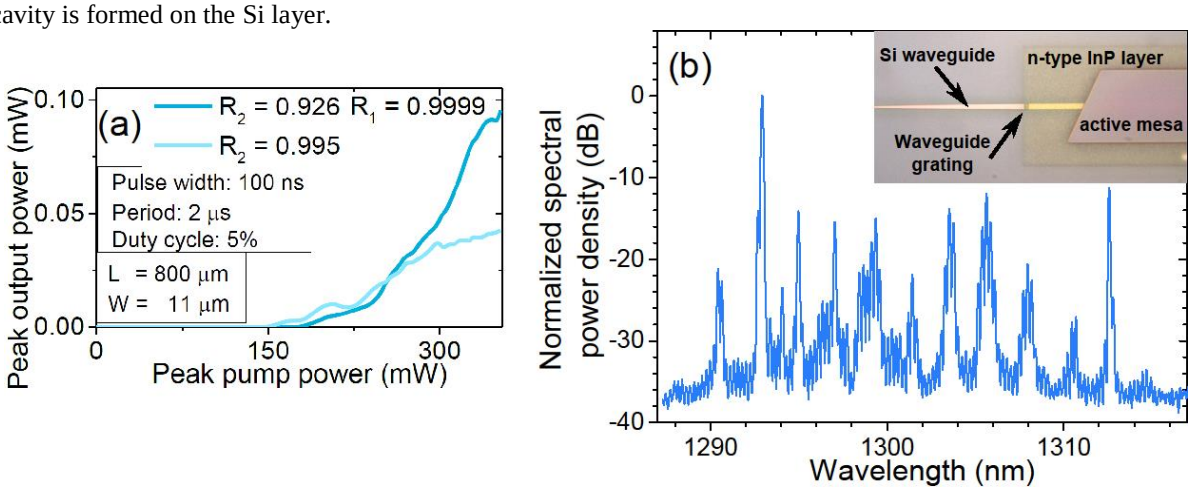


*Figure 6. a) Room temperature L-I curve of two optically pumped lasers showing output power dependence of mirror reflectivity $R_2$. A threshold power density of 1.7 kW cm$^{-2}$ is measured for the higher reflectivity device. b) Room temperature optical spectrum of laser device. Inset: Top-view photograph of laser device (the Si waveguide is tapered down to the bus waveguide width of 500 nm on the left).*

## 5. CONCLUSIONS

We have shown a concept to embed active optical devices in CMOS SiPh chips, in which SiPh, (Bi)CMOS and lasers share the same BEOL. Adiabatic couplers for low-loss optical coupling between the III-V and Si waveguide have been designed. Epitaxial layer optimization, low-resistive ohmic contacts, optimized dry etching and current blocking layer formation have been shown. Finally, optically-pumped lasers with feedback in Si were demonstrated. The next step is to realize electrically-pumped lasers based on this concept.

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