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Low-resistive, CMOS-compatible ohmic contact schemes to moderately doped n-InP

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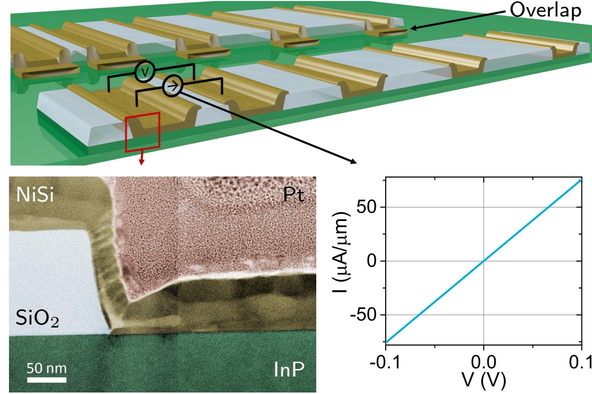
Abstract

III-V laser integration on Si is seen as a promising path to overcome the current interconnect bottleneck in computing. Therefore, III-V lasers need to be integrated with a CMOS-compatible process flow as well as that parasitic elements of the lasers need to be minimized while preventing trade-offs to the lasing action (i.e. doping level in the $10^{18}\,\mathrm{cm}^{-3}$). One such parasitic element is the n-type ohmic contact on moderately-doped n-InP. A detailed study of Au-free contacts on n-InP including structural analysis has not yet been performed. To fill this gap, we will comprehensively report on various metal contacts on n-InP that reach a record-low median specific contact resistivity of $6\times10^{-8}\,\Omega\cdot\mathrm{cm}^2$ and on contacts that show very shallow alloying behavior while still offering a specific contact resistivity in the very low $10^{-7}\,\Omega\cdot\mathrm{cm}^2$ range.

Keywords

InP, NiSi, ohmic contacts, CMOS-compatible



1 Introduction

Passive and active photonic devices are well-established in telecommunication and data communication applications. Since the distance for which optical communication is used is decreasing further, integration of photonics on the chip-level is already foreseen.[1] While discrete photonic circuits are mainly realized in InP technology, for the chip-level integration, Si photonics has a tremendous advantage due to the low cost and high throughput obtained in CMOS fabs.[2,3] Although Si and its oxide SiO_2 offer very attractive physical properties for light transmission, Si with its indirect bandgap is not a suitable material for light sources. Hence, direct bandgap semiconductors such as used in InP-related technology need to be employed. Using heterogeneous integration of III-V material on silicon-on-insulator (SOI) via bonding or direct growth can hence have a large impact for the realization of on-chip laser source.[4,5] Laser sources and other active devices such as photo-detectors have already been integrated successfully on SOI platforms.[6–9] Traditionally, III-V materials and devices have been fabricated with dedicated non-CMOS-compatible technology. One such example are ohmic contacts of electronic and optoelectronic devices. Beside the common use of lift-off processes, also the use of non-CMOS-fab compatible metals such as Au has been very common.[6,10,11] Beside Au being not tolerated in a CMOS fab, it typically leads to spiking behavior during alloying.[12–14] For structures with the n-type layer on top of the multi-quantum-well (MQW),[15] this may deteriorate the lasing function due to free-carrier absorption or formation of non-recombination centers. Yet, Au-free InP contacts have been reported only

sparsely. Beside typical Au-containing reports, a detailed electrical study with proper contact behavior has only been performed by Jain *et al.*[16] A structural analysis of such contacts is yet missing and furthermore, a fully CMOS-compatible flow for the fabrication of ohmic contacts has not yet been applied. Hence, in this paper, we will report contacts with a fully CMOS-compatible process flow. The thin contacts used are further suitable for integration in extremely thin lasers stacks that could be implemented between the front-end-of-the-line (FEOL) and the back-end-of-the-line (BEOL) of a CMOS process flow. We will show record values for the specific contact resistance. The contacts are furthermore characterized by means of cross-sectional scanning electron microscopy (SEM), scanning transmission electron microscopy (STEM) and energy dispersive X-ray (EDX) spectroscopy. Very shallow contact formation will be presented. This paves the way for a tight III-V laser integration on Si.

2 Experimental

On 2-in. semi-insulating InP (InP:Fe) wafers, metal-organic chemical vapor deposition (MOCVD) was performed to deposit 50 nm of n-doped InP (InP:Sn) with a doping concentration of $5\times10^{18}\,\mathrm{cm}^{-3}$. The growth rate was determined using high-resolution X-ray diffraction (HRXRD) on a dummy wafer that was prepared in a previous run including a marker layer. The doping concentration was verified by Hall measurements. To avoid any metal contamination on the semiconductor surface, we used a process that incorporates first a passivation layer, then a via opening and finally the metal deposition and patterning. Before the passivation layers, the wafers were cleaned in diluted H_3PO_4 and rinsed in DI water. Beside cleaning, diluted H_3PO_4 is also supposed to remove the native oxide. The wafers were then loaded into a thermal atomic layer deposition (ALD) tool. At 250 °C, about 3 nm of Al_2O_3 was deposited on the wafers. This layer was utilized as both surface passivation and etch-stop. The wafers were then transferred to a plasma-enhanced chemical

vapor deposition (PECVD) tool to deposit 200 nm of SiO_2. This layer acted as final passivation. Mesa isolation was performed by optical lithography, removal of the SiO_2 using a CHF_3-based reactive-ion etch (RIE) process, subsequent removal of the Al_2O_3 by diluted HF (dHF) and final dry-etch of the n-InP in an inductively-coupled plasma reaction-ion etch (ICP-RIE) chamber using CH_4/H_2 as reactive gas. To ensure proper isolation, the samples were well over-etched. Subsequently, openings for the ohmic contacts were fabricated by means of optical lithography and dry-etching of SiO_2 using a CHF_3-based RIE process. The process stopped at the Al_2O_3 layer. At this step of fabrication, the wafers were diced into $12\times12\,mm^2$ pieces. Immediately prior to the metal deposition, the Al_2O_3 was removed using dHF. Metal deposition was then performed by DC-sputtering. For the Ni-alloy samples, rapid thermal annealing (RTA) was performed directly after the first metal deposition. The temperature in the RTA was assessed by a thermocouple connected to a Si wafer on which the samples were placed. Subsequently, the unalloyed Ni was removed selectively to the Ni-alloy using a wet etch solution. Finally, W plugs were sputtered to contact the Ni-alloy. For all other samples, the metal layers were patterned by means of ion-beam etching (IBE) and RIE. Finally, except for the Ni/W samples, an RTA was performed under forming-gas atmosphere with 5 % H_2 content.

Transfer length method (TLM) (as indicated in the abstract illustration) and circular TLM (CTLM)[1] characterization was performed on a semi-automatic probe station using an Agilent B1500A Semiconductor Device Parameter Analyzer. For the sake of higher accuracy, the TLM contacts were overlapping the mesa (*cf.* with the abstract illustration). The TLM device dimensions are 100 μm and 50 μm for contact width and contact length, respectively, and 5, 10, 15, 20 and 25 μm for the various contact separations. The CTLM device dimensions are 50 μm inner radius and 5, 7.5, 10, 12.5 and 15 μm for the contact separations. Samples for cross-sectional high-resolution scanning electron microscopy (HRSEM) were prepared and imaged with a dual beam FEI HELIOS NanoLab 450S focused ion beam (FIB). Prior to the

[1]CTLM had to be used for the Ni/W samples since mesa-isolated regions reacted with Ni to form a leakage path.

cross-sectional cut obtained by employing Ga ions, few hundreds of nm of electron beam (e-beam) and ion beam Pt have been deposited to protect our layers. Using the same procedure, also samples for high-resolution scanning transmission electron microscopy (HRSTEM) and energy dispersive X-ray spectroscopy (EDX) were obtained. High-angle annular dark-field (HAADF) images have then been acquired with a double aberration-corrected JEOL ARM 200F microscope operated at 200 kV. EDX maps have been performed using a liquid-nitrogen-free silicon drift detector (SDD) and an image correction has been applied after each scanned line.

3 Results and Discussion

First, the lower limit of accurate extraction values for the TLM method is calculated. For a contact length L_c much larger than the transfer length L_T (which holds in all our cases), the lower limit is given as[17]

$$\rho_c \geq 0.2 \cdot R_{sh} \cdot t^2 \tag{1}$$

in which ρ_c, R_{sh} and t correspond to the specific contact resistivity, the sheet resistance of the semiconductor and the thickness of the semiconductor, respectively. With

$$R_{sh} = \frac{1}{e \cdot n \cdot t \cdot \mu_n} \tag{2}$$

in which e, n and μ_n correspond to the elementary charge, the electron concentration and the electron mobility, respectively, Eq. 1 becomes to

$$\rho_c \geq 0.2 \frac{t}{e \cdot n \cdot \mu_n} \tag{3}$$

Apparently, a thin layer allows for an accurate extraction of ρ_c for lower values. Using the values extracted from a reference sample subjected to Hall measurements [$t = 50\,\text{nm}$, $n = 5 \times 10^{18}\,\text{cm}^{-3}$ and $\mu_n = 1100\,\text{cm}^2/(\text{V}\cdot\text{s})$], we obtain the requirement $\rho_c \geq 1.2 \times 10^{-9}\,\Omega\cdot\text{cm}^2$.

As we will show, this holds for all samples.

Leakage current in TLM structures can deteriorate the extraction accuracy. We therefore monitored the current between contacts that reside only on the etched area. Such measurements yielded typically three orders of magnitude lower current than those between contacts on top of the mesa. The accuracy of the present investigation is hence mainly limited by the variation in contact separation. This variation originates from the optical lithography processing and it is compensated for by manual measurement of the separation gaps.

3.1 W vs. Mo/W vs. Ni/Si

As a first set of experiments, a comparison between three different metal stacks is performed. To this end, W, Mo/W and Ni/Si-based ohmic contacts are compared. All stacks have a nominal thickness of 75 nm. For the Mo/W stack, this is shared to 5 and 70 nm, whereas for the Ni/Si stack it is shared to 25 nm and 50 nm. The experiment was created in a design of experiments (DOE) manner using JMP software.[18] Beside the difference in metal stack, various process variations were performed for wet treatment (no additional treatment, or treatment in diluted H_3PO_4), annealing temperature (350 °C to 450 °C) and annealing time (20 s to 180 s). The mean ($\overline{\rho_c}$) data for 24 different samples with each 16 test sites obtained by TLM measurements is shown as a 3D plot with error bars for standard deviation (σ) in Figure 1. Apparently, the choice of metal stack has a much higher influence on ρ_c than the other parameters. The values for the Ni/Si stack are roughly one order of magnitude lower than the ones for the other two stacks. The lowest median value of about $1.5\times10^{-6}\,\Omega\cdot\text{cm}^2$ ($\overline{\rho_c}\pm\sigma = 1.7\times10^{-6}\,\Omega\cdot\text{cm}^2\pm0.8\times10^{-6}\,\Omega\cdot\text{cm}^2$) is achieved for the Ni/Si sample with a 20 s anneal at 400 °C and with prior wet clean. However, from the evaluation of the full DOE, all parameters except for the metal stack were calculated as being not significant. From a contour plot (*cf.* with the supplemental material Figure S2) of the Ni/Si-based samples, it is concluded that a low annealing temperature with longer annealing times yields the lowest values for ρ_c. In addition, a clear influence of annealing temperature on time and *vice versa*

is observed. In general, this first DOE allowed us to conclude that a Ni-based stack is more likely to lead to a low ρ_c.

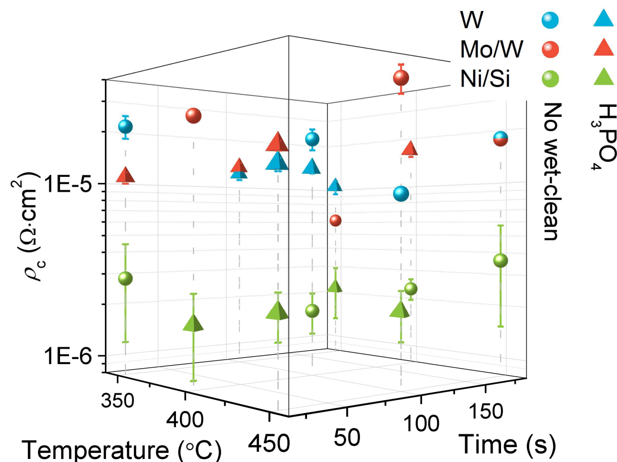


Figure 1: Ohmic contact resistance for a DOE that compares different metal schemes, annealing temperatures, times and a wet clean. The largest influence on ρ_c is apparently the metal scheme. W and Mo/W contacts yield almost similar values for ρ_c, whereas Ni/Si contacts have values that are roughly one order of magnitude lower.

3.2 Ni/W samples

Based on these conclusions, we fabricated TLM samples with Ni/W stacks. These were fabricated as described in Section 2. Again, an experiment was designed with different parameters. The initial Ni thickness was varied between 3 and 10 nm, the annealing temperature between 250 °C and 400 °C and the annealing time between 60 s to 300 s. The results of 11 samples are plotted in Figure 2. For all samples, ohmic contact behavior is obtained. In comparison to the experiments before, a larger variation in the results is observed. Median values for ρ_c vary between $2.3\times10^{-7}\,\Omega\cdot cm^2$ and $4.1\times10^{-6}\,\Omega\cdot cm^2$. In comparison to the earlier discussed experiment, several samples show reduced ρ_c.

For an in-depth analysis of this experiment, more samples would be needed. Yet, an influence on Ni layer thickness together with the annealing temperature seems to exist, such that with larger Ni layer thicknesses and higher annealing temperatures, improved values for ρ_c can be expected. Sample B5 is examined via cross-sectional SEM. Additionally, sample

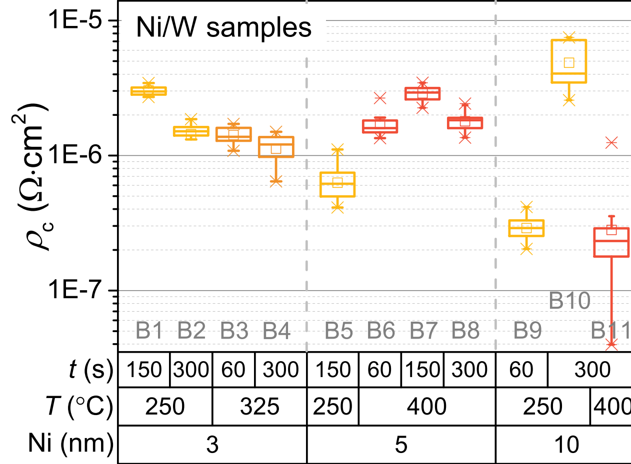


Figure 2: Box plot of ohmic contact resistance for Ni/W samples with different Ni thicknesses, annealed at various temperatures and for various times. Samples are grouped and a warmer color corresponds to a higher temperature. Lowest values for ρ_c are obtained for the thickest Ni layer.

B9 with a median ρ_c of $2.9 \times 10^{-7}\,\Omega{\cdot}\text{cm}^2$ (10 nm, 250 °C for 60 s) was used for both SEM and TEM cross-sections as will be discussed further below.

3.3 Ni/Si-based samples

In a next step, different stacks based on alternating layers of Ni and Si are analyzed.

Prior to the ohmic contact evaluation, 4-point IV measurements of dummy samples (annealed Ni and Si layers on SiO_2) were performed to optimize the contact stack sheet resistance $R_{\text{sh,pad}}$. This experiment involved variations in Si:Ni thickness ratios. For the 75 nm thick layers, values between 2.5 Ω/sq. (optimized) and 9.0 Ω/sq. (non-optimized) were obtained. The optimized values were obtained for a Ni:Si thickness ratio of approx. 1:1. The stacking order had only a minor influence on $R_{\text{sh,pad}}$.

Of particular interest for this series is whether a difference in contact resistivity is observed between stacks with either Ni or Si in intimate contact to the n-InP. Therefore, 3 nm thin layers of either Ni or Si or both were deposited below the thicker contact layers (that are now approx. of equahellol thickness). For all samples, the total stack thickness was still kept at 75 nm.

The mean results of TLM measurements for 24 samples based on four different metal stacks are shown in contour plots in Figure 3. The schematics on top of the plots indicate the metal layer arrangement for each individual stack. The plots are all scaled in the same range. The median values for ρ_c vary between $8.0\times10^{-8}\,\Omega\cdot\text{cm}^2$ and $1.8\times10^{-5}\,\Omega\cdot\text{cm}^2$ (respective mean values: $9.8\times10^{-8}\,\Omega\cdot\text{cm}^2$ and $1.9\times10^{-5}\,\Omega\cdot\text{cm}^2$). For the sample with Ni/Si/Ni contact (Figure 3a) values around $1\times10^{-6}\,\Omega\cdot\text{cm}^2$ are obtained. The same observation holds for the sample with Si/Ni/Si contact [Figure 3 b)]. For the sample with a Si/Ni/Si/Ni contact, values are higher by one order of magnitude (Figure 3c). Apparently, for the sample with the Ni/Si/Ni/Si contact (Figure 3c), this is reversed. Only for this stack, a sample with ρ_c below $1\times10^{-7}\,\Omega\cdot\text{cm}^2$ is obtained.

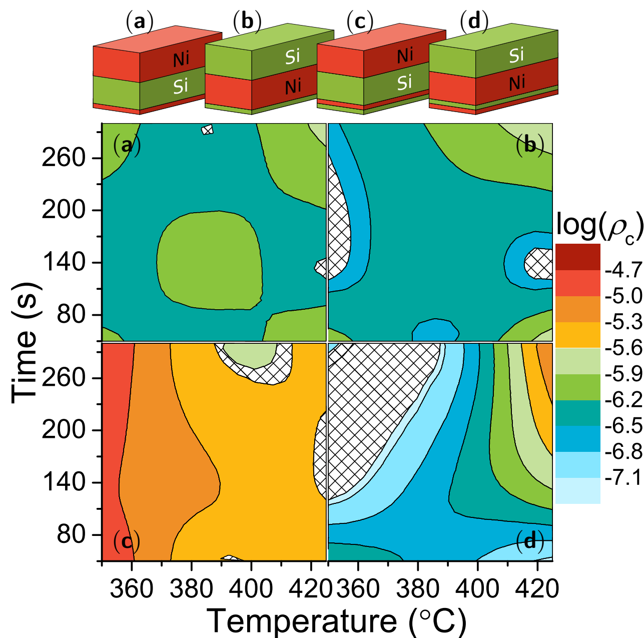


Figure 3: Smoothed contour plots of the logarithmic ρ_c vs. annealing temperature and annealing time for four different Ni/Si contact schemes. The ohmic contact schemes are illustrated on the top. The thin layer(s) have a nominal thickness of 3 nm, and the total height is 75 nm for all stacks. Clearly, the highest ρ_c is obtained for structure c), whereas the lowest ρ_c is yielded for structure d).

These results show several effects. Using the refined annealing process parameters, we can clearly see an influence of these onto ρ_c. Furthermore, it appears that to achieve proper ohmic contacts, Ni has to be either in direct contact with n-InP or needs to be available in

larger amounts directly above the first Si layer. The results indicate that for three stacks (a,b,d), a similar dependence of ρ_c on annealing parameters is observed. Optimal annealing conditions are either at lower temperatures for longer durations or at higher temperatures for shorter times. It appears that at low temperatures and short times, the ohmic contact formation is not fully performed, whereas for higher temperatures and longer durations, the contact already degrades.

To analyze this further, a final set of 8 samples was prepared. To this end, the metal stacks as depicted in Figure 3b,d were used in combination with a two-step anneal. A first annealing step was performed either at 240 °C or 275 °C for 30 to 100 s, after which a second step at 350 °C was performed for 50 s and 300 s, respectively. The resulting data is plotted in Figure 4 and for each sample, 13 to 16 TLM structures were assessed. A length correction for the Ni encroachment was performed for the samples with the first annealing step at 275 °C (Ni encroachment discussed later).

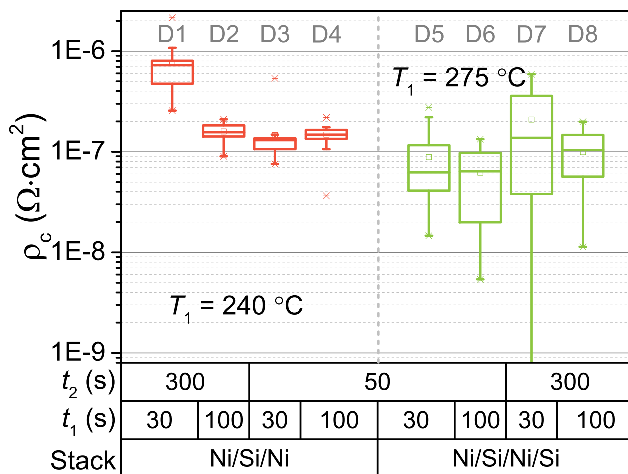


Figure 4: Ohmic contact resistance for optimized metal and annealing schemes. Two sets with either Ni/Si/Ni (left four) or Ni/Si/Ni/Si (right four) stack were annealed with different times. The second anneal step was performed for all samples at $T_2 = 350\,°\mathrm{C}$. Other anneal parameters (t_1 and t_2 being the durations in the first and second annealing step, respectively, and T_1 the respective temperature in the first step) as indicated in the Figure. The plots shows clearly different behavior for the two metal stacks and also some slight trends with temperature. Sample D6 shows record-low ρ_c.

For all samples, a ρ_c below $1{\times}10^{-6}\,\Omega{\cdot}\mathrm{cm}^2$ is obtained. Except for one samples, almost

all measured structures show a ρ_c of even below $2{\times}10^{-7}\,\Omega{\cdot}cm^2$. The colors indicate the used metal stack (red - three layers, green - four layers). The higher ρ_c for the sample D1 is linked to its higher R_{sh} of $363 \pm 136\,\Omega$/sq. compared to mean values and standard deviations of 211-245 Ω/sq. and 3-12 Ω/sq., respectively, for the remaining samples. These mean values of R_{sh} match the Hall results of the reference sample mentioned in Section 2. The sample group annealed at 275 °C shows slight lower values for ρ_c. This comes at a slightly increased standard deviation σ. This difference in σ, however, appears in this semi-logarithmic plot larger than it actually is. Beside the difference related to the metal layer stack, a trend towards higher values of ρ_c is visible for the longer time in the second annealing step and towards higher values for shorter annealing times in the first annealing step (at least for samples D5-D8). Overall, the lowest values for ρ_c are achieved for samples D6 with a median value of $6.4{\times}10^{-8}\,\Omega{\cdot}cm^2$. This reflects the lowest value ever reported for ohmic contacts on moderately-doped n-InP ($\overline{\rho_c} \pm \sigma = 6.2{\times}10^{-8}\,\Omega{\cdot}cm^2 \pm 4.1{\times}10^{-8}\,\Omega{\cdot}cm^2$).

4 Structural analysis

To corroborate a better understanding of the electrical results, additional cross-sectional SEM, STEM and EDX results of selected samples are discussed. False-colored cross-sectional SEM images are shown for four different samples in Figure 5. Samples B5 and B9 were discussed in Section 3.2 and Figure 2 and samples D3 and D6 in Section 3.3 and Figure 4. The area of interest is composed of the metal-semiconductor interface as well as the area in which metal, semiconductor and SiO_2 converge (*cf.* with the illustration in the abstract).

All images show the two Pt layers originating from the samples preparation. In the actual devices, these are not present. Figures 5a,b show images of the samples with Ni/W stack (B5 and B9). For both samples, a wavy surface below the ohmic contact is apparent. In addition, an interfacial layer that is most likely the result of the alloying of Ni on InP is visible for both samples. Owing to the larger initial Ni layer thickness for sample B9, the

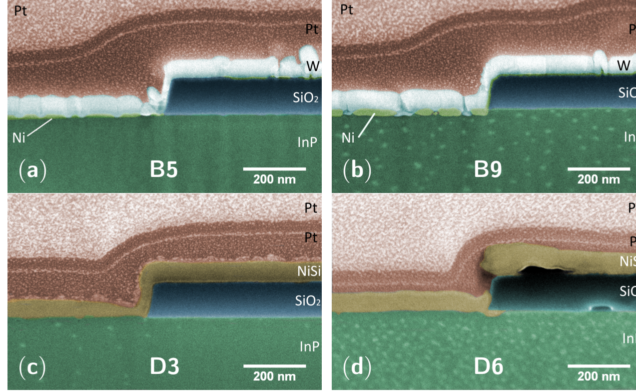


Figure 5: Cross-sectional SEM images of two samples with Ni/W contact [a: B5 and b: B9] and two with Ni/Si-based contact [c: D3 and d: D6]. All images are in false colors to enhance the readability of the micrographs. B5 features a Ni thickness of 5 nm, B9 of 10 nm. For both samples, an interfacial layer between W and InP is visible, more apparently for B9, for which the alloyed portion is approx. 25 nm. For sample D3, a three layer Ni/Si/Ni stack was used and also here, a slight contrast difference is visible at the metal/n-InP interface. All layers appear to be very smooth for this sample. For sample D6, a distinct nose of an alloyed portion is visible below the SiO_2. For all samples, a bright interface between SiO_2 and InP indicates the presence of the thin ALD-Al_2O_3 oxide layer.

interfacial layer is more pronounced for this sample. With the visible recess into the InP, it appears that InP is consumed during the anneal. For sample B9, the layer thickness of the alloyed region is approx. 25 nm. For sample B5, this effect is less pronounced. Furthermore, the alloying leaves gaps in between the Ni-dominated regions. However, as we have seen from the first experimental series discussed for Figure 1, in which W samples have shown a rather high ρ_c, the low values for ρ_c have to be originating from the Ni-InP interface. No Ni-dominated region is migrating below the SiO_2.

For samples D3 and D6 (Figure 5c,d), a different appearance of the interfaces is observed. For sample D3, a very smooth metal-semiconductor interface is apparent. No visible consumption of InP as well as proper alloying of Ni and Si is visible. These findings hold for all samples D1-D4 (*cf.* with the supplemental material Figure S5). In contrast, for sample D6, the NiSi shows a discontinuity at the sidewall of the SiO_2 layer. Again, no visible consumption of InP is appearing and the NiSi layer seems to be properly alloyed. Very remarkable, the NiSi is penetrating between the Al_2O_3 and InP. This effect has been similarly reported

for the silicidation process for which Ni is alloyed with a Si substrate layer[19,20] as well as for Ni on $In_{0.53}Ga_{0.47}As$.[21]

Based on these findings, TEM cross-sections were prepared and investigated for samples B9, D3 and D6. For all samples, additionally, EDX measurements were performed at selected spots.

The results for sample B9 are plotted in Figure 6. The colors used for enhancing the visibility are the same as used for the cross-sectional SEM images. We hence omitted to label the layers. Figure 6d shows an overview of the investigated region in which SiO_2, Ni, W and InP converge. A thick Ni-rich layer is sandwiched between W and InP. The consumption of InP is also very visible. One of the gaps in the Ni-rich region that have been observed already in Figure 5 is now clearly visible in the STEM image. For this sample, the Al_2O_3-InP interface (Figure 6a) appears slightly rough. We correlate this to the roughness provided by the W layer that deteriorates somewhat the TEM sample quality. This well-known "theater curtain" effect originates from the columnar structure of the W layer in combination with the FIB preparation.[22] The EDX color maps in Figure 6b,c show clearly air gaps, but also that Ni is intermixing with P, but not with In. We assume that In segregrated on top of the NiP layer which allowed us to remove it with the Ni etchant. The Ni-W interface that is depicted in Figure 6e shows a smooth interface. This is supported by the HR-EDX color plot in Figure 6f, in which the separation between Ni and W is clearly shown. The EDX signal count plot in Figure 6g shows, despite the lack of an annealing step, an intermixed region between Ni and W of roughly 2 nm. Additionally, P is still present on the top of the Ni-rich region. We refer the slightly increased In count on top of the Ni-rich region to the increased noise level that is provided by the W layer. Figure 6h shows a zoom-in on the interface between Ni-rich region and InP. Despite the apparent alloying, the interface appears to be very smooth and the lattice of InP is intact. The HR-EDX color plot in Figure 6i proves again a strong presence of P in the Ni-region. This is manifested further by the corresponding EDX signal count plot in Figure 6j that shows even an increased presence

of P in Ni as compared to the first few nm of InP. Since we also see a clear drop of In in the Ni-rich region, we therefore conclude that the Ni-rich region is most likely the binary alloy of NiP and that In segregated on top of this layer. The alloying between Ni and InP has been discussed in previous studies for initial Ni layer thickness of 300-500 nm,[23] 40-50 nm[24,25] (as cited in Ref. 23), 30 nm[26] and 20 nm.[27] The latter study was, however, performed including a surface-damage inducing Ar^+ sputter step. After an initial alloying of Ni and InP to an amorphous Ni_xInP with subsequent segregation of the single phases, a binary phase of NiP is forming for temperatures in the range of 250 °C.[23] While this is consistent with our results, Ghegin *et al.* did not observe this formation at 250 °C but only at higher temperatures of 300 and 340 °C.[27] A final formation of monoclinic Ni_2InP is also discussed in Ref. 23 to occur at an annealing temperature of 280 °C for 300 s. Looking back at Figure 2, we can identify samples B6-B8 and B11 to meet this condition and we may speculate that the transition from NiP to Ni_2InP does not modify ρ_c by large.

HAADF images of sample D3 are plotted in Figure 7. Figure 7d shows an overview of the analyzed areas with details depicted in Figure 7a-c. Several conclusions can be drawn from these images. First and as expected, we can see in Figure 7a that the interface between Al_2O_3 and InP is atomically flat with height variations in the order of one atomic layer. Second, the NiSi to InP interface shows very much the same surface roughness. A slight recess into the InP layer is visible in Figures 7b,c. This recess is either related to a slight InP consumption that could occur during the thermal anneal or during the removal of natively-oxidised InP during the HF dip prior to the metallization. For the NiSi layer, the color contrast indicates a rather inhomogeneous layer composition. This can most likely be related to Si- and Ni-rich regions in the respective Si and Ni layers that were originally deposited.

EDX analysis has also been performed on this sample. In Figure 7e, a dark-field zoom-in on the section discussed beforehand is visible. In this image, the area in which the EDX spectrum was taken is displayed. As can be seen from the two maps (Figures 7f,g), a sharp interface between SiO_2 and NiSi without intermixing is present. Furthermore, within the

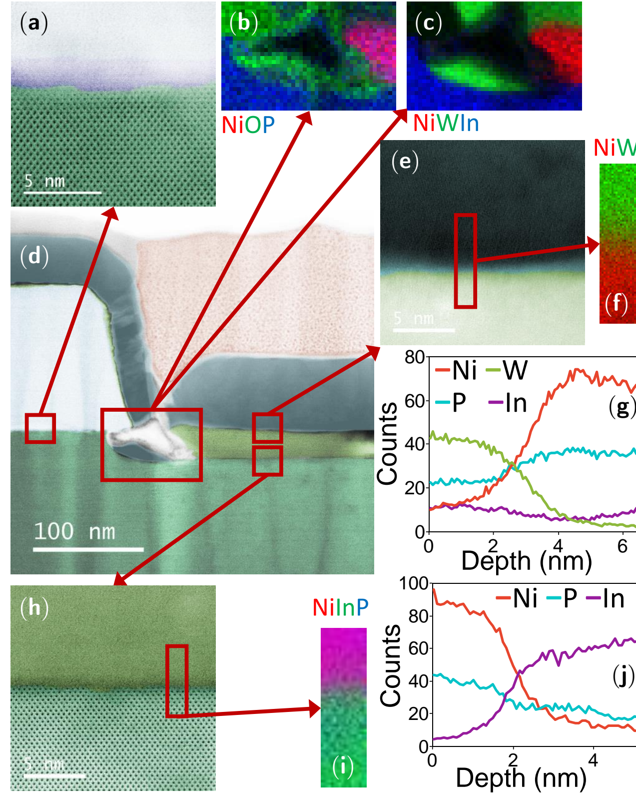


Figure 6: HAADF images of sample B9. False colored images are colored as in Figure 5. (a) Zoom-in at the Al_2O_3-InP interface. Visible roughness is related to TEM sample roughness originating from the W layer during FIB preparation ("theater curtain" effect). (b), (c) EDX color plots of area in which W reached the InP surface. (d) Overview of analysed area. (e) Close-up of Ni/W interface with (f) HR-EDX color map and (g) EDX signal count plot showing a smooth surface very little intermixing between Ni and W. (h) Zoom-in on the Ni-InP interface showing a smooth surface, yet with slight intermixing that is more detailed shown in (i) the EDX color map and (j) the EDX signal count plot that both reveal intermixing between Ni and InP in about 1 nm. Apparently, P is present in the Ni layer.

resolution of the image, the interface between NiSi and InP appears to be sharp without intermixing as well. As assumed beforehand, Figures 7f,g indicate that the NiSi layer is most likely not completely intermixed. Figure 7h shows a zoom-in on the NiSi-InP interface with the respective EDX color maps depicted in Figures 7i,j and their corresponding EDX signal count plot in Figure 7k. Clearly visible is an atomically sharp interface. From the counts, a region of less than 1 nm shows intermixing between NiSi and InP. Yet, this abrupt interface gives proper ohmic contact behavior. Metal stacks prepared like the one for this sample are hence a way to form ohmic contacts even on laser stacks for which very shallow alloyed

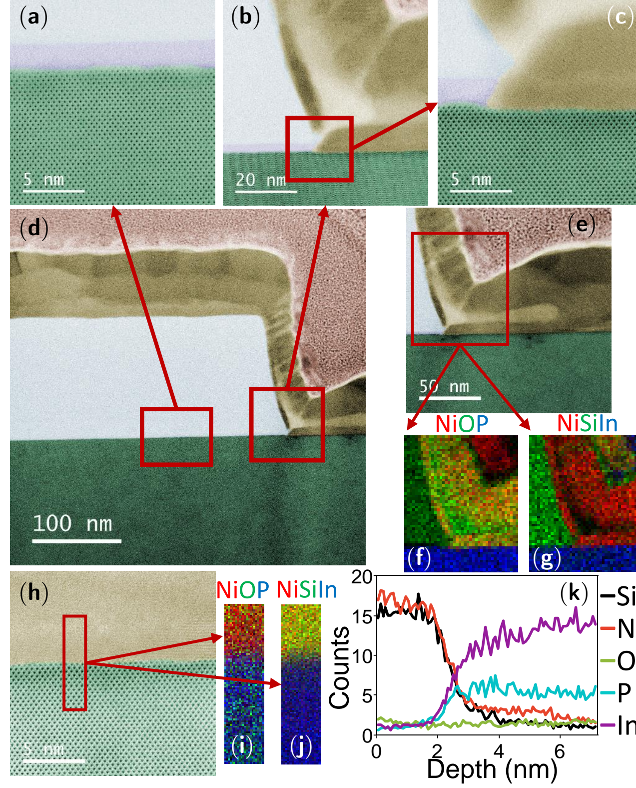


Figure 7: HAADF images of sample D3. False colored images are colored as in Figure 5. (a)-(c) Zoom-ins of cross-section in (d) showing close-ups of the very smooth Al_2O_3-InP and NiSi-InP interfaces and the area where NiSi, InP and SiO_2 converge. (e) Another zoom-in in which the site for the EDX spectra is indicated. (f), (g) EDX spectra showing clear separation between NiSi, InP and SiO_2. (h) Another zoom-in at the NiSi-InP interface in which site for HR-EDX spectra is indicated. (i), (j) HR-EDX spectra showing little intermixing of NiSi and InP and (k) signal count plot confirms intermixing in between less than 1 nm.

regions are mandatory.

HAADF images of sample D6 are presented in Figure 8. A cross-sectional view on the region that was discussed for the other samples is shown in Figure 8a. Clearly visible are air gaps below and above the SiO_2 as well as in the area in which the NiSi layer is interrupted. Furthermore, the pronounced nose is visible and its length and depth are about 70 nm and 25 nm. The bright-field zoom in Figure 8b shows the nose in detail. From these two images, the higher interface roughness as compared to sample D3 is also visible. EDX maps obtained from the area indicated in Figure 8b are shown in Figure 8c,d. Despite the nose, still, a clear distinction between NiSi and InP is obtained. However, a closer look on Figure 8e and its

respective EDX color maps Figure 8f,g reveals that the intermixed region for this sample is approx. 2 nm wide. The plot in Figure 8h illustrates this further. Hence, for this stack, larger intermixing is obtained than for the three layer stack.

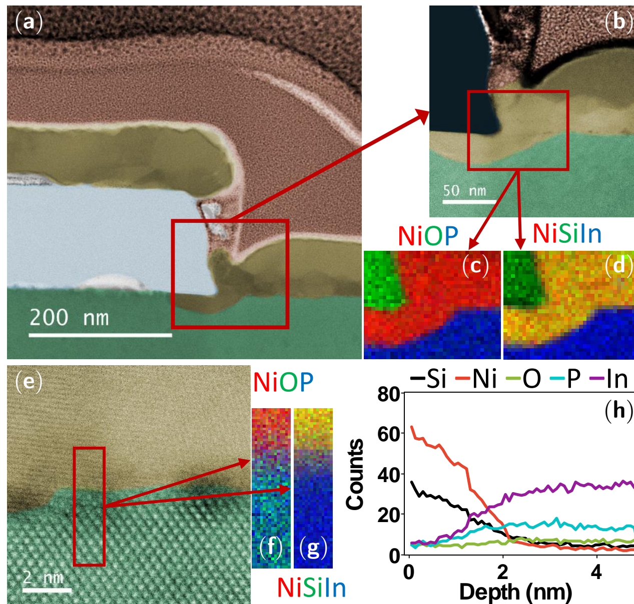


Figure 8: HAADF images of sample D6. False colored images are colored as in Figure 5. (a) Cross-sections showing InP, NiSi layer and SiO_2 (and Pt) with the gap in NiSi as observed beforehand. The nose of the Ni is also visible. (b) Bright-field zoom-in of (a) in which the site for EDX spectra is indicated. (c), (d) Three-colored EDX maps showing clear separation between NiSi, InP and SiO_2. (e) Dark-field zoom-in of the metal-semiconductor interface. Site for HR-EDX spectra is indicated. (f), (g) HR-EDX spectra showing only minor intermixing of NiSi and InP. (h) Plot of signal count showing intermixing of InP and NiSi in between 2 nm.

5 Conclusion

In summary, various metal schemes for ohmic contact fabrication on n-InP have been analyzed electrically and structurally. While W and Mo/W have been found to result in rather high values of ρ_c, Ni/Si has been identified as a suitable metal stack. In addition, Ni/W samples prepared in a two-step approach in which Ni is alloyed and W acts as plug to the actual contact have shown proper ohmic behavior with ρ_c values down to $2\times10^{-7}\,\Omega\cdot\text{cm}^2$. In a refined approach, ohmic contacts with three and four alternating Ni and Si layers have been

investigated. With this approach, ρ_c has been reduced to below $1\times10^{-7}\,\Omega\cdot\text{cm}^2$. Finally, by employing a two-step annealing procedure, a record-low median ρ_c of $6.4\times10^{-8}\,\Omega\cdot\text{cm}^2$ has been achieved. Structural analysis of selected Ni/W and Ni/Si samples has revealed that Ni alloys with InP and the alloyed portion strongly depends on the Ni thickness. Encroaching NiSi below the passivation layer has been identified for certain samples. With properly designed metal stacks, the intermixing region between NiSi and InP can be limited to 1 nm, making such stacks ideal candidates for highly-scaled integrated III-V lasers for which deep alloying needs to be prevented.

Supporting Information Available

The following files are available free of charge.

- SuppInfo.pdf: Box-plots with individual process parameters for Figures 1 and 3. Smoothed contour plot for the data of the Ni/Si samples discussed in Figure 1. Unsmoothed contour plot for Figure 3. Cross-sectional SEM images in addition to Figure 5.

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Supporting information for: Low-resistive, CMOS-compatible ohmic contacts schemes to moderately doped n-InP

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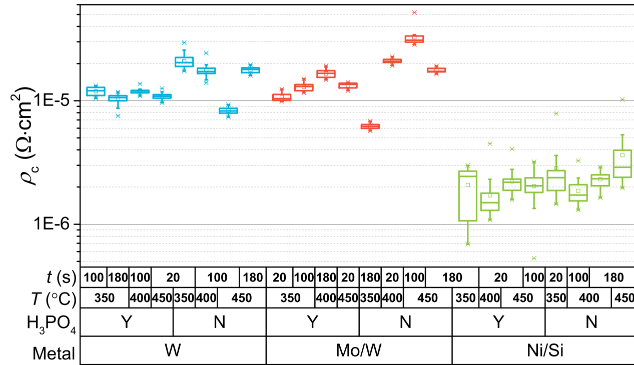

Figure S1: Box plot of Figure 1. Ohmic contact resistance for a DOE that compares different metal schemes, annealing temperatures, times and a wet clean.

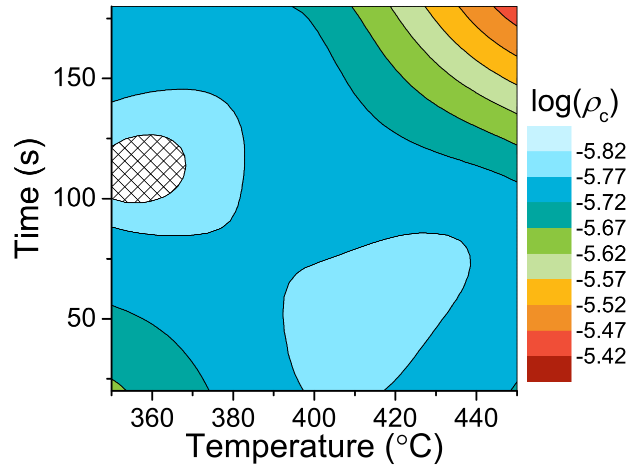

Figure S2: Smoothed contour plot for the Ni/Si samples presented in Figure 1. Logarithmic of specific contact resistance is plotted vs. annealing temperature and time. Wet clean is assumed to have no impact for this plot. Longer times at lower annealing temperatures or shorter times at higher annealing temperatures seem to be best for low ρ_c. Strong dependence between those two parameters is visible.

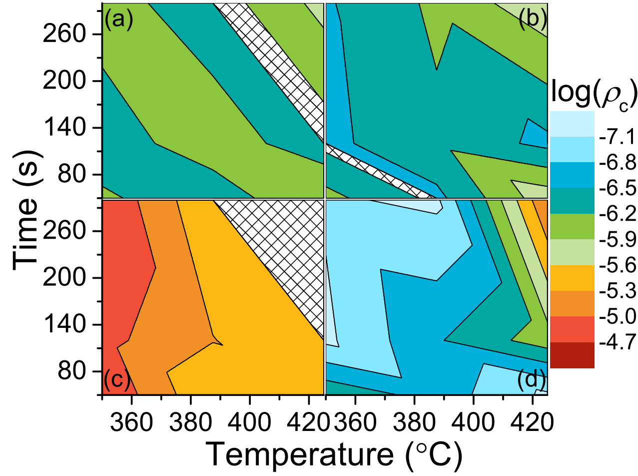

Figure S3: Unsmoothed version of contour plots of Figure 3. The logarithmic ρ_c is plotted vs. annealing temperature and annealing time for four different Ni/Si contact schemes. The ohmic contact schemes are illustrated on the top of Figure 3. The thin layer(s) have a nominal thickness of 3 nm, and the total height is 75 nm for all stacks.

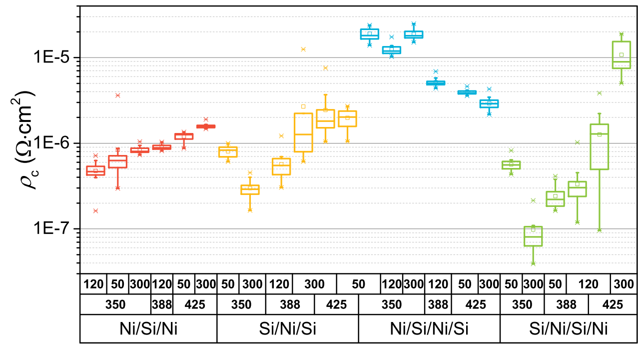

Figure S4: Box plot for four different Ni/Si contact schemes as used in Figure 3. The ohmic contact schemes are illustrated on the top of Figure 3. The thin layer(s) have a nominal thickness of 3 nm, and the total height is 75 nm for all stacks.

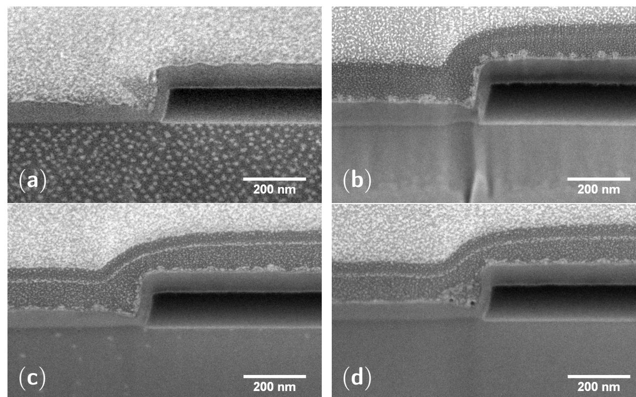

Figure S5: Cross-sectional SEM images of samples (a) D1, (b) D2, (c) D3 and (d) D4. For all samples, smooth layers and a clear transition between metal and semiconductor is apparent.

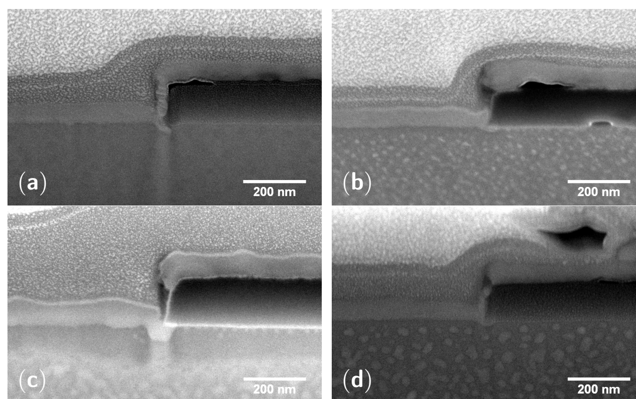

Figure S6: Cross-sectional SEM images of samples (a) D5, (b) D6, (c) D7 and (d) D8. For all samples, the nose as described in the original manuscript is visible.