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Research Report

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Y. Baumgartner, B. Mayer, M. Sousa, D. Caimi, K. Moselund, L. Czornomaz

IBM Research – Zurich
8803 Rüschlikon
Switzerland

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Monolithic Integration of InAlAs/InGaAs Quantum-Well on InP-OI Micro-substrates on Si for Infrared Light Sources

Y. Baumgartner[a], B. Mayer[a], M. Sousa[a], D. Caimi[a], K. Moselund[a], L. Czornomaz[a].
[a] IBM Research GmbH, Säumerstrasse 4, CH-8803 Rüschlikon, Switzerland.

Abstract - ***We demonstrate for the first time that InAlAs/InGaAs QW can be selectively grown on micron-sized InP-OI substrates, obtained by selective epitaxy in empty oxide cavities on Si. The concept, material and optical characterizations are presented, paving the way towards integrated light sources for infrared applications.***

I. Introduction

Using optical interconnects with Silicon Photonics (SiPh) is expected to be the ultimate solution to boost the cost-efficiency and bandwidth of data centres [1]. However on-chip light sources coupled to SiPh are missing owing to the difficulty to integrate III-V gain materials on Si. Selective epitaxy of III-V compounds on large Si wafers is the most competitive approach to integrate such light sources, assuming that the crystalline quality of the III-V can be further improved [2].

Selective epitaxy in oxide cavities was previously used to demonstrate III-V/SiGe CMOS circuits, III-V nanowires and III-V heterojunction Tunnel FETs on Si [3,4,5,6]. Recently this concept was extended to integrate GaAs virtual substrates on SOI wafers for integrated light sources [7]. Here we further develop this concept and demonstrate the integration of InAlAs/InGaAs quantum-well (QW) on local InP micro-substrates on SOI. Our results show that III-V gain material can be used for III-V/Si lasers.

II. Concept

The large lattice mismatch of III-V compounds with Si and the change of polarity at the substrate interface restrict the use of III-V materials for integrated devices on Si, due to a high density of dislocations, antiphase domains and stacking faults in the III-V layer. Recently one dimensional defect filtering via aspect ratio trapping was used to obtain hybrid optically-pumped distributed feedback lasers on Si [8].

In the present work we further improve the material quality by integrating micron-sized InP islands on Si wafers using selective epitaxy in empty SiO_2 cavities. This growth technique typically restricts most defects in the first nanometres of the III-V layer [9], thanks to an efficient defect filtering in many directions. Empty SiO_2 cavities are obtained using CMOS-compatible processes and materials, as shown in Fig. 1. The cavities contain 1) a small crystalline Si seed, 2) an arbitrarily defined geometry which shapes the growing III-V crystal, and 3) openings to allow the metalorganic precursors to enter the cavity. Micron-sized InP substrates are grown by metal-organic chemical vapor deposition (MOCVD) within the cavities. After stripping the top oxide of the cavities, the surface of InP islands is used for the overgrowth of III-V heterostructures. We chose as a model system to grow a lattice-matched InAlAs/InGaAs stack containing 3 QW.

III. Results and discussion

Transmission Electron Microscopy (TEM) performed after the growth of InP within the cavities are shown on Fig. 2. Such InP-on-Insulator (InP-OI) micro-substrates can be used for the integration of other III-V materials on Si. SEM images of Fig. 3 show the cavity before (a) and after (b) the growth of InP. Fig. 3(c) illustrates an overgrown InAlAs/InGaAs QW stack on InP. The surface morphology and roughness indicates that the layer might contain some crystalline defects, originating either from strain relaxation in the targeted $In_{0.52}AlAs/In_{0.53}GaAs$ stack or from the InP-OI micro-substrates. As compared with regular growth on InP wafer, selective epitaxy of ternaries is challenging owing to varying loading factor across the wafer and fluctuating diffusion length of the group-III atoms on the surrounding SiO_2. EDX line-scans of Fig. 4(a) reveal the presence of the InGaAs QW and InAlAs barriers and a sharp interface with the InP-OI micro-substrate. PL at room-temperature was observed, with a central wavelength at 1090 nm (Fig. 4(b)). Improved process conditions for the QW growth – or the integration of more complex III-V quaternary heterostructures on the InP-OI micro-substrates - will allow providing gain at higher wavelengths.

IV. Conclusions

Using selective epitaxy in empty SiO_2 cavities, we demonstrate the monolithic integration of InP-OI micro-substrates on Si, which can be used to overgrow other III-V stacks. We show a room-temperature PL signal from an overgrown InAlAs/InGaAs heterostructure, paving the way for cost-efficient and CMOS-compatible laser sources for infrared applications.

V. Acknowledgements

Fruitful discussions with Prof. Jérôme Faist and support by the BRNC OpTeam are acknowledged. This project has received funding from the EU-H2020 research and innovation programme under grant No 688003, 688172 and 688544.

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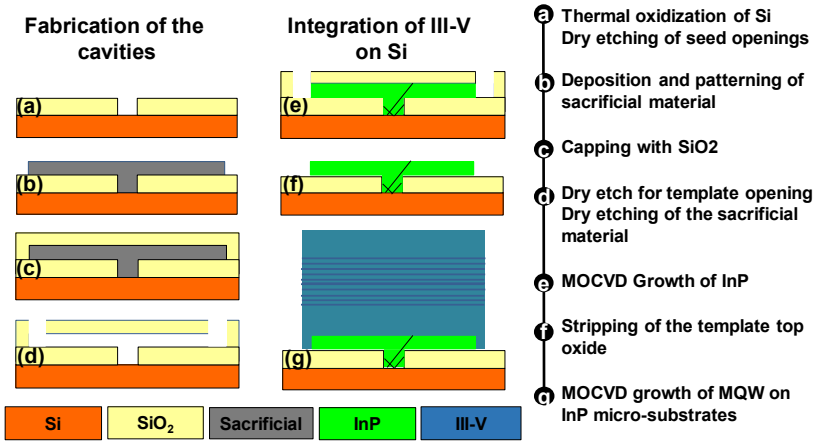

Fig. 1: Schematic and Process flow used to obtain $In_{0.52}AlAs$/ $In_{0.53}GaAs$ QW structures on InP-OI micro-substrates.

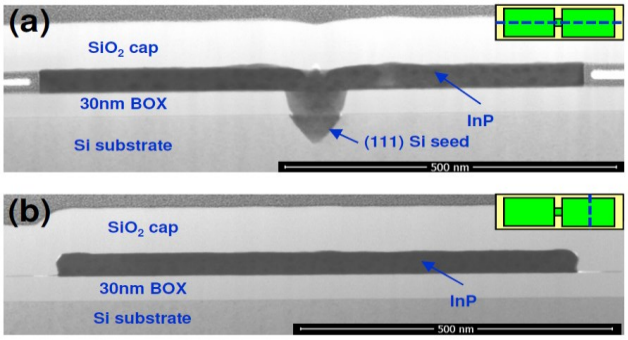

Fig. 2: TEM cross section of InP micro-substrates on Si (a) along and (b) perpendicular to the growth direction [9].

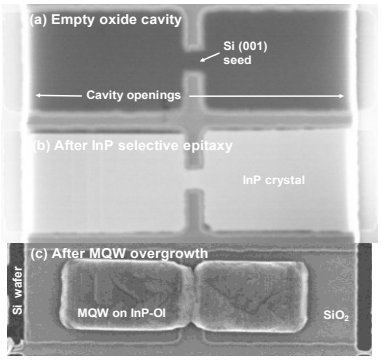

Fig. 3: Top views of a SiO_2 cavity (a) before and (b) after the growth of InP and (c) after oxide cap removal and over-growth of InAlAs/InGaAs QW.

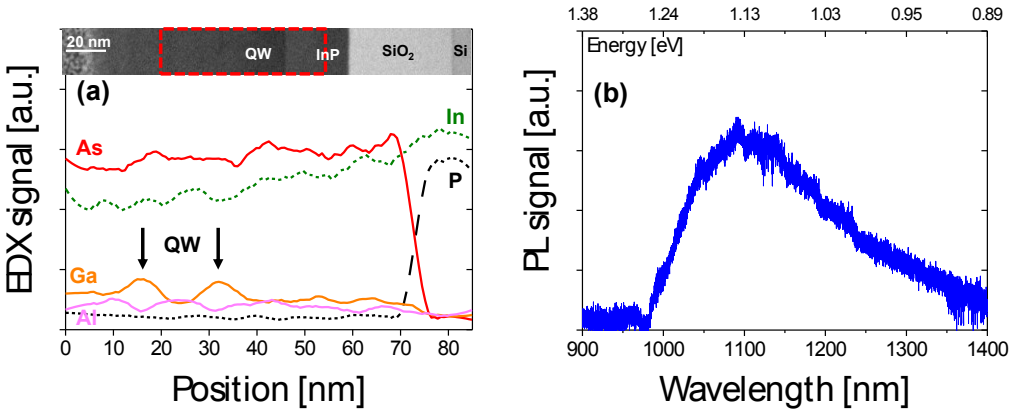

Fig. 4: (a) EDX line-scan across an InAlAs/InGaAs QW structures grown on an InP-OI micro-substrate. Inset: TEM image of the QW stack - analyzed area in red. (b) PL signal from one overgrown QW structure acquired at room temperature.