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Research Report

Micro-cavity III-V Lasers Monolithically Grown on Silicon

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We will present our recent work on III-V micro-cavity lasers monolithically grown on silicon substrates. The III-V material is directly grown using Template-Assisted-Selective-Epitaxy (TASE) within oxide cavities patterned using conventional lithographic techniques on top of the silicon substrate. This allows for the local integration of single-crystal III-V active gain material. Two variations of this technique will be discussed; the direct growth of disc lasers and the two-step approach via a virtual substrate. Room temperature single-mode optically pumped lasing is achieved in GaAs micro-cavity lasers, and devices show a remarkably low shift of the lasing threshold (T_0=170K) with temperature. Dependence on cavity geometry and pump power will be discussed.

Introduction

Silicon is the material of choice for the electronics industry, and this technology has been optimized to perfection throughout the past half century. However, as we move beyond conventional silicon CMOS there is a rising interest in integrating other materials on the Si substrate. In particular, co-integrated III-V materials are of great interest as active gain material for on-chip silicon photonics. Silicon is an excellent choice of material as waveguide, but its indirect bandgap makes it unsuitable for efficient light emission.

We have developed a method for monolithic III-V on Si integration, where we grow the III-V material within lithographically defined oxide cavities [1-4]. This provides us with a high degree of control and versatility, while eliminating some of the constraints associated with either buffer layers or traditional selective area growth of nanowires (NWs). This method has been employed to demonstrate various electronic devices ranging from high performance InGaAs nFET [4], complementary III-V heterostructure TFETs [5] to ballistic transport in one-dimensional InAs NWs [6]. Recently, we have also expanded this technology to optically active devices, enabling monolithically integrated μ-cavity GaAs lasers showing lasing at room temperature [7] and providing the potential for more complex photonic structures by developing this technology as a virtual substrate approach [8-9].

Here, I will primarily cover the fabrication method in its various embodiments, with focus on photonic applications, where somewhat larger volumes of III-V material are required compared to the electronic applications. The requirements specific to photonic structures will be discussed and the most recent results in this domain will be shown.

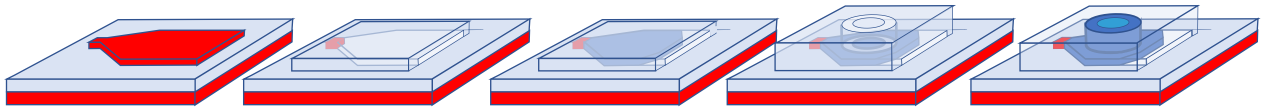
Template-Assisted Selective Epitaxy (TASE)

The two implementations of TASE used for nanophotonic devices in a planar orientation are illustrated in Fig. 1. The virtual substrate approach is illustrated in Fig 1.A. this is a two-step growth approach starting from an SOI substrate. First a lateral growth is used to create a virtual III-V substrate (thickness about 50nm) on top of the BOX layer of the SOI. Subsequent template fabrication steps allow for a second confined growth in the vertical direction of about 2-300nm thickness, whereby an optical cavity is created. The advantage of this approach is that in principle it allows for the integration of homo- or heterojunctions in the vertical direction.

Fig. 1.B shows the Direct Cavity growth approach, whereby mushroom-shaped III-V nanolasers are monolithically integrated on top of a conventional Si(001) or Si(111) substrate. This simplifies the growth as it only requires a single growth step. Furthermore, the top surface of the micro-disc is completely flat as it conforms to the template oxide, favoring a high-Q cavity. As a drawback, the control of the cavity geometry might require more complex processing.

In both cases the key is to limit the size of small Si seed area either at one extremity of the hollow template or via a small opening to the underlying substrate, and letting the template oxide guide the shape of the grown material. The template is epitaxially filled using metal-organic chemical vapor deposition (MOCVD). The growth starts from the Si seed, which assures a single nucleation point. Since the resulting large crystal is expanded from one nucleation point, typical defects found in planar mismatched heteroepitaxy are absent. Misfit dislocations which relax the strain between the materials are present and confined to the Si/III-V interface. The presence of the template also prevents the lateral overgrowth often associated with NW growth.

A. Virtual substrate approach



B. Direct cavity growth

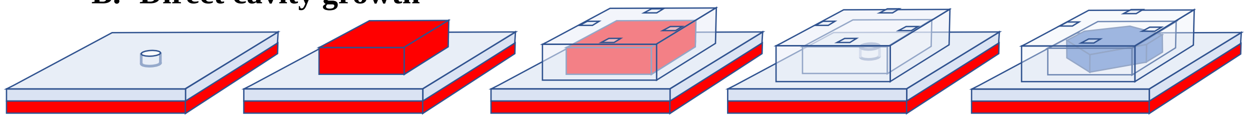


Figure 1 Schematics illustrating the concept of TASE in two different implementations. A virtual substrate approach, where first a thin III-V layer is grown horizontally from a small Si-seed. This is followed by a second templated growth step in the vertical direction which defines the optical cavity. B: Direct cavity growth, where a conventional Si substrate is covered by an oxide layer which simultaneously serves as selective epitaxy mask and dielectric isolation of the optical mode. A hole is made in the oxide, to expose the underlying Si which acts as nucleation seed. A sacrificial material is used to construct a hollow oxide cavity which is then gradually filled with III-V material growing out from the seed.

Materials, heterojunctions and devices

We have explored TASE growth of the In(Ga)As and In(Ga)Sb families extensively for the application for various electronic devices [10]. Here the high performance observed in electrical devices as well as high electron mobilities measured (5400 cm^2/Vs measured for InAs doped to

$5x10^{17}$cm-3 [3]) is a testament to the quality of the grown III-V material. Also the local integration of multiple III-V materials on a single Si substrate was shown in [11]

For optical applications, however, the challenges are somewhat different. Firstly, to scale all geometries up while controlling small feature size for the nucleation seed is non-trivial, for example photonics requires thicker dielectric layers for optical isolation which leads to increased topography as compared to electronics. At the same time the size of the nucleation area must be kept small, in the 100nm range or less. Also, stacking faults which are often linked to selective epitaxial growth is less important for conventional electronic devices, whereas they might be detrimental for optical devices.

Compared to high performance FETs, optical devices need to be larger in dimensions. This places new requirements on the epitaxy steps in the templates, which must be optimized for fast growth rates, high selectivity, and economic use of reagents.

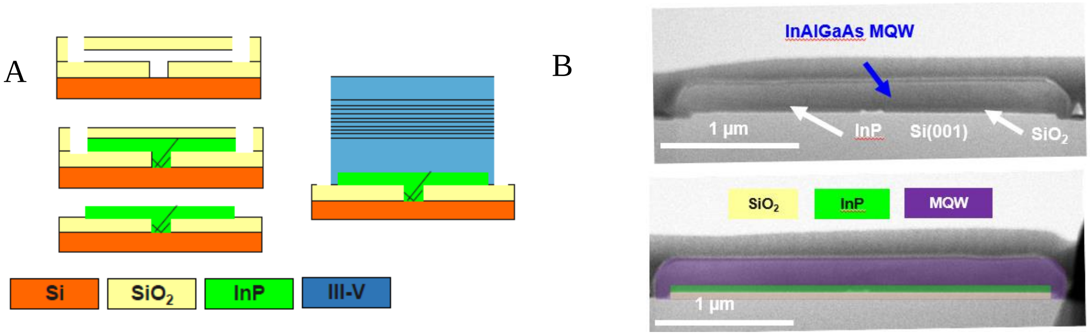


Figure 2 A) Schematic of the TASE virtual substrate approach applied to the growth of vertical quantum wells on top of a silicon substrate. B) Focused ion beam TEM cross-section of the quantum well structure showing the different material regions, from [9].

Micro-cavity GaAs lasers monolithically grown on silicon

Recently we have demonstrated GaAs microcavity lasers grown monolithically on Si, using both the virtual substrate and direct cavity growth approaches illustrated in Fig. 1. We chose GaAs as model system to circumvent composition matching needed in a ternary system.. Using both approaches we demonstrated lasers operating at room temperature based on pulsed optical pumping. Simulated Q-factors for the micro-cavities are around 1600. Cross-sections and spectra of both types of devices are shown in Fig. 3 and Fig. 4 respectively.

The Input-Output characteristics depicted in figure 3 for a direct cavity laser of roughly 3µm diameter exhibit the characteristic S-shape, with thresholds of about 12 pJ/pulse. A study of the variation of threshold as a function of device diameter shows an improvement for smaller diameters of around 1µm. In some structures the nucleation would happen elsewhere than the Si seed, resulting in non-epitaxial growth and crystal defects, suppressing lasing in these devices. While the PL emission follows the Varshni shift as a function of temperature, the lasing wavelength of these devices is remarkably temperature stable.

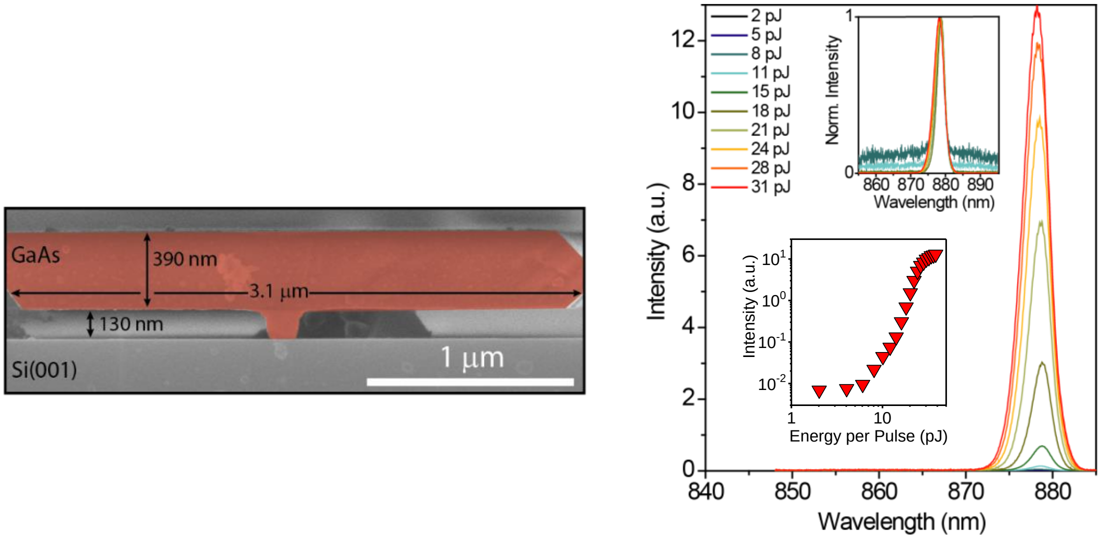


Figure 3 A) Cross sectional TEM (false colored) of a direct-cavity grown micro-cavity laser. B) lasing characteristics of a 3um wide GaAs μ-disc laser shown in (A) adapted from ref [7].

A cross-section TEM and the lasing characteristic for a virtual substrate GaAs micro-cavity laser is shown in Figure 4. Unlike the case for the direct-growth lasers the emission here is multimode. We speculate that this is due to the less defined cavity as in this case the top of the GaAs is not smooth as it is not confined by the template as in the case of the GaAs sample. We also here observe the characteristic S-curve with a very similar threshold to the direct cavity grown sample.

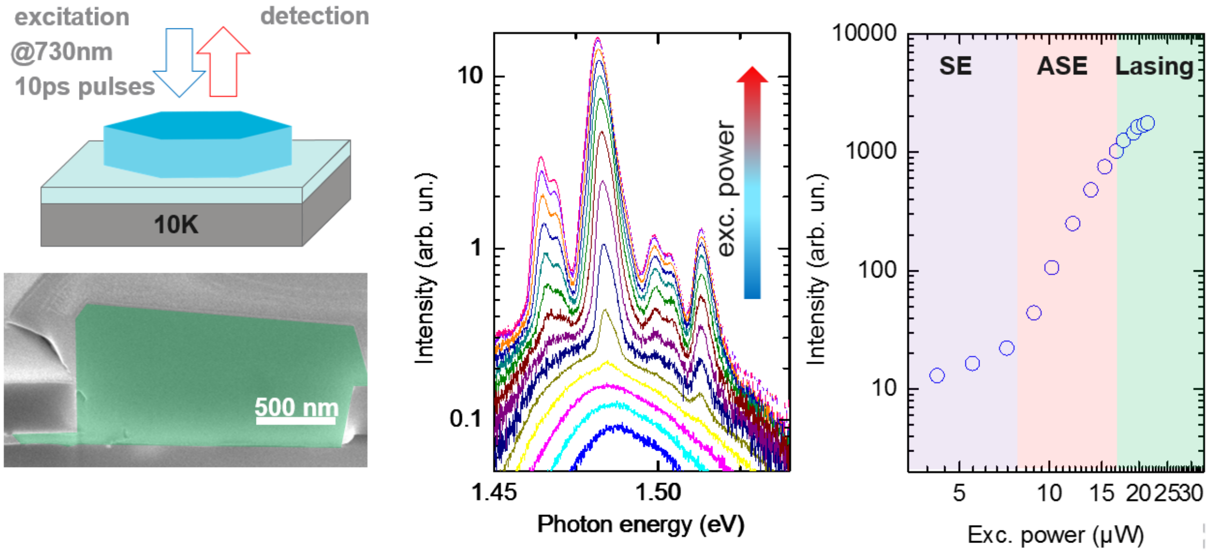


Figure 4 A) Cross sectional TEM (false colored) of a virtual substrate micro-cavity laser, the schematic above illustrates the characterization scheme. B) power series showing the multimode lasing characteristics and (C) input-output light characteristics for the device shown in (A), adapted from ref [8].

Conclusion

Monolithic III-V integration using TASE is a versatile integration method, suited for the seamless integration of high-quality III-V nanostructures on Si photonic platforms. As shown in Fig. 5 which portrays the timeline of our device and material focus, the platform was originally developed for electronics, and is now evolving towards active photonic devices. We have presented our work on optical emitters based on directly grown GaAs, and shown optically pumped pulsed room-temperature lasing from the cavities which are on the size of μm. Direct coupling of the III-V devices with Si waveguides will greatly facilitate PIC application.

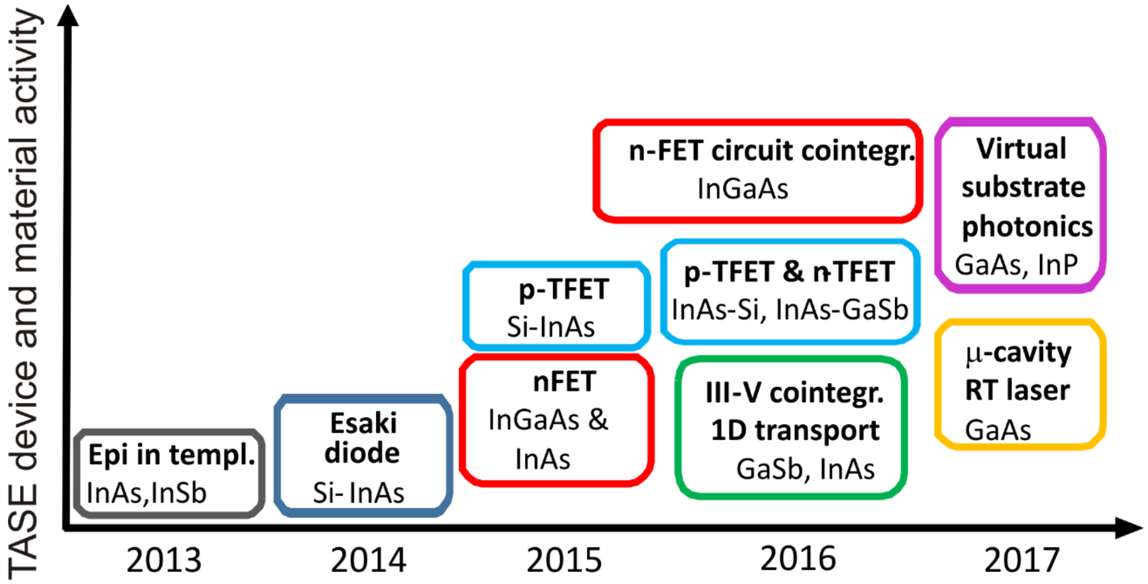


Figure 5 Evolution of TASE-based work, spanning growth, materials and device activities all with focus towards CMOS compatibility.

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References

[1] Kanungo, P. D. et al. "*Selective area growth of III–V nanowires and their heterostructures on silicon in a nanotube template: towards monolithic integration of nano-devices*", Nanotechnology, vol. 24, 225304, (2013).

[2] Borg, M. et al., "*Vertical III-V Nanowire Device Integration on Si(100)*", Nano Lett., vol.14, pp. 1914–1920, (2014).

[3] Schmid, H. et al., "*Template-assisted selective epitaxy of III-V nanoscale devices for co-planar heterogeneous integration with Si*", Appl. Phys. Lett., vol. 106, 233101, (2015).

[4] Czornomaz, L. et al., "*Confined Epitaxial Lateral Overgrowth (CELO): A novel concept for scalable integration of CMOS-compatible InGaAs-on-insulator MOSFETs on large-area Si substrates*", VLSI Symp., T172-T173, (2015)

[5] Cutaia, D. et al. "*Complementary III-V Heterojunction Lateral NW Tunnel FET Technology on Si",* Symp. on VLSI Technology, pp. 403-407, (2016).

[6] Gooth, J. et al, "*Ballistic one-dimensional transport in InAs nanowires monolithically integrated on silicon* ", Applied Physics Letters, vol. 110, 083105, (2017).

[7] Wirths, S. et al. "*Room Temperature Lasing from Monolithically Integrated GaAs Microdisks on Si*", CLEO Europe, (2017).

[8] Mayer, B. et al. "*Monolithically Integrated III-V Gain Material on Virtual Substrates on Si Using Template-Assisted Selective Epitaxy*", CLEO Europe, (2017).

[9] Baumgartner, Y. et al., “*Monolithic Integration of InAlAs/InGaAs Quantum-Well on InP-OI Micro-substrates on Si for Infrared Light Sources*”, To be presented at Group IV Photonics (GFP), 2017 IEEE 14th International Conference on. IEEE, (2017).

[10] Schmid, H. et al. “*Monolithic integration of multiple III-V semiconductors on Si for MOSFETs and TFETs*”, Proc. IEDM, (2016)

[11] Borg, M. et al., “*High-Mobility in GaSb Nanostructures Cointegrated with InAs on Si*”, ACS Nano, 11, 2554-2560, (2017).